3.3 V Zero Delay Buffer

Features

- Zero input-output propagation delay, adjustable by capacitive load on FBK input
- Multiple configurations
- Multiple low-skew outputs
- 10 MHz to 133 MHz operating range
- 90 ps typical peak cycle-to-cycle jitter at 15 pF, 66 MHz
- Space-saving 8-pin 150-mil small outline integrated circuit (SOIC) package
- 3.3 V operation
- Industrial temperature available

Functional Description

The CY2304 is a 3.3 V zero delay buffer designed to distribute high-speed clocks in PC, workstation, datacom, telecom, and other high performance applications.

The part has an on-chip phase-locked loop (PLL) that locks to an input clock presented on the REF pin. The PLL feedback is required to be driven into the FBK pin, and can be obtained from one of the outputs. The input-to-output skew is guaranteed to be less than 250 ps, and output-to-output skew is guaranteed to be less than 200 ps.

The CY2304 has two banks of two outputs each.

The CY2304 PLL enters a power down state when there are no rising edges on the REF input. In this mode, all outputs are three-stated and the PLL is turned off, resulting in less than 25 µA of current draw.

Multiple CY2304 devices can accept the same input clock and distribute it in a system. In this case, the skew between the outputs of two devices is guaranteed to be less than 500 ps.

The CY2304 is available in two different configurations, as shown in Table 1. The CY2304–1 is the base part, where the output frequencies equal the reference if there is no counter in the feedback path.

The CY2304–2 allows the user to obtain Ref and 1/2x or 2x frequencies on each output bank. The exact configuration and output frequencies depends on which output drives the feedback pin.

Logic Block Diagram

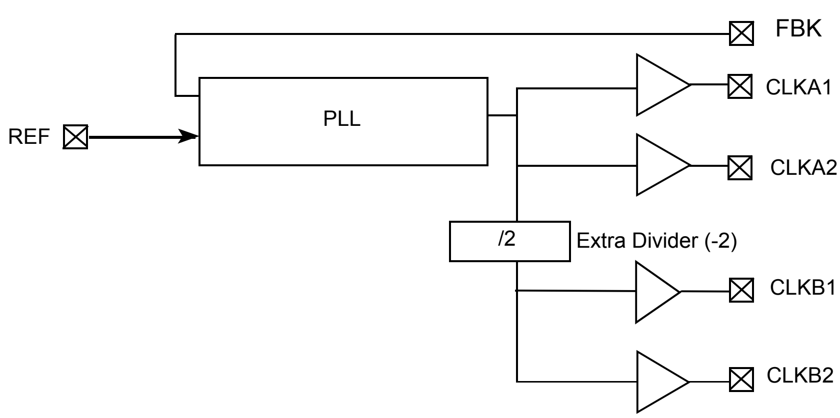


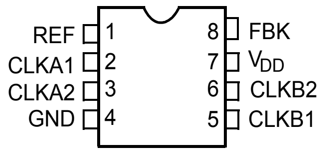
Table 1. Available Configurations

Device	FBK from	Bank A Frequency	Bank B Frequency
CY2304-1	Bank A or B	Reference	Reference
CY2304-2	Bank A	Reference	Reference/2
CY2304-2	Bank B	2 × Reference	Reference

Contents

Pin Configurations

Figure 1. 8-pin SOIC pinout



Pin Definitions

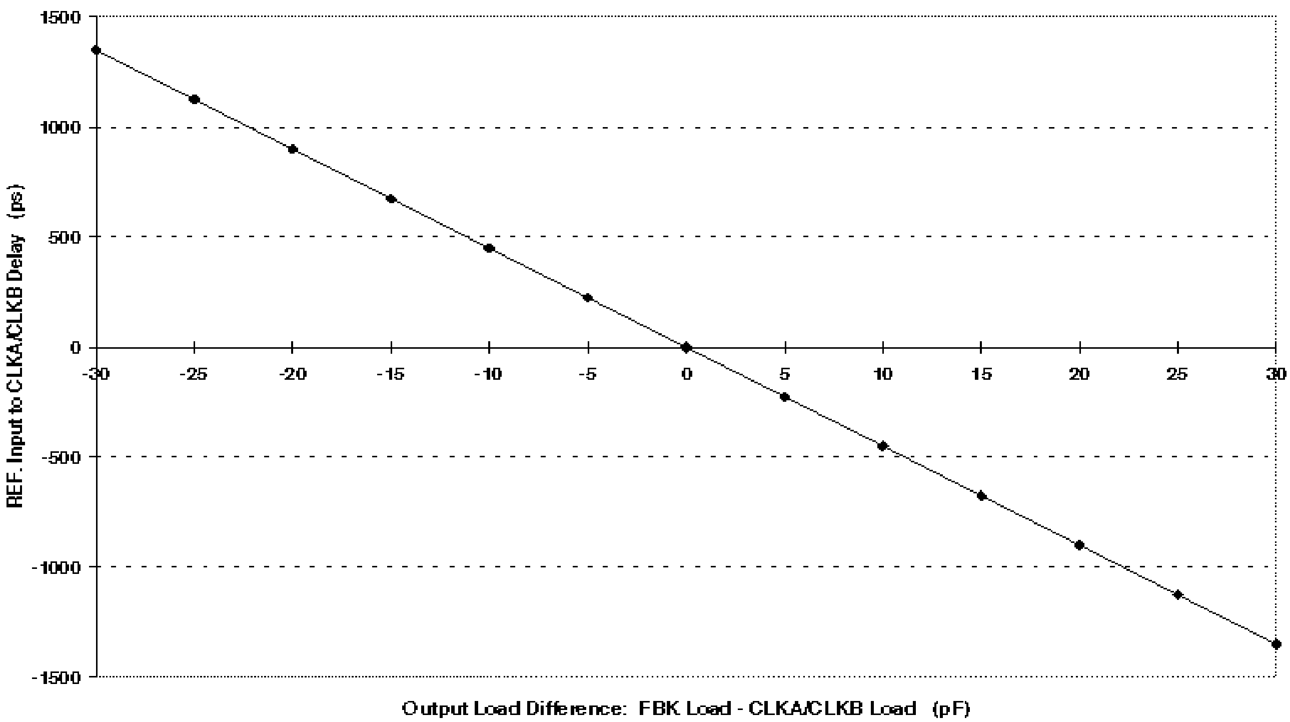
8-pin SOIC

Pin	Signal	Description
1	REF [1]	Input reference frequency, 5 V tolerant input
2	CLKA1 [2]	Clock output, Bank A
3	CLKA2 [2]	Clock output, Bank A
4	GND	Ground
5	CLKB1 [2]	Clock output, Bank B
6	CLKB2 [2]	Clock output, Bank B
7	V_{DD}	3.3 V supply
8	FBK	PLL feedback input

Notes
1. Weak pull-down.
2. Weak pull-down on all outputs.

Zero Delay and Skew Control

Figure 2. REF. Input to CLKA/CLKB Delay vs. Difference in Loading Between FBK Pin and CLKA/CLKB Pins



To close the feedback loop of the CY2304, the FBK pin can be driven from any of the four available output pins. The output driving the FBK pin is driving a total load of 7 pF, with any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input-output delay. This is shown in Figure 2.

For applications requiring zero input-output delay, all outputs including the one providing feedback must be equally loaded. If input-output delay adjustments are required, use the graph shown in Figure 2 to calculate loading differences between the feedback output and remaining outputs.

For zero output-output skew, be sure to load outputs equally. For further information on using CY2304, refer to the application note AN1234 “CY2308: Zero Delay Buffer”.

Maximum Ratings

Supply voltage to ground potential .... –0.5 V to +7.0 V

DC input voltage (except Ref) .... –0.5 V to V_{DD} + 0.5 V

DC input voltage REF .... –0.5 V to 7 V

Storage temperature .... –65 °C to +150 °C

Junction temperature .... 150 °C

Static discharge voltage
(per MIL-STD-883, Method 3015) .... > 2000 V

Operating Conditions

For CY2304SXC Commercial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage	3.0	3.6	V
T_A	Operating temperature (ambient temperature)	0	70	°C
C_L	Load capacitance (below 100 MHz)	–	30	pF
	Load capacitance (from 100 MHz to 133 MHz)	–	15	pF
C_{IN}	Input capacitance [3]	–	7	pF
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics

For CY2304SXC Commercial Temperature Devices

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW voltage		–	0.8	V
V_{IH}	Input HIGH voltage		2.0	–	V
I_{IL}	Input LOW current	V_{IN} = 0 V	–	50.0	µA
I_{IH}	Input HIGH current	V_{IN} = V_{DD}	–	100.0	µA
V_{OL}	Output LOW voltage [4]	I_{OL} = 8 mA (-1, -2)	–	0.4	V
V_{OH}	Output HIGH voltage [4]	I_{OH} = –8 mA (-1, -2)	2.4	–	V
I_{DD} (PD mode)	Power-down supply current	REF = 0 MHz	–	12.0	µA
I_{DD}	Supply current	Unloaded outputs, 100 MHz REF, Select inputs at V_{DD} or GND	–	45.0	mA
		Unloaded outputs, 66 MHz REF (-1, -2)	–	32.0	mA
		Unloaded outputs, 33 MHz REF (-1, -2)	–	18.0	mA

Notes
3. Applies to both REF clock and FBK.
4. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics

For CY2304SXC Commercial Temperature Devices

Parameter [5]	Name	Test Conditions	Min	Typ	Max	Unit
t_1	Output frequency	30 pF load, all devices	10	–	100	MHz
t_1	Output frequency	15 pF load, -1, -2 devices	10	–	133.3	MHz
t_{DC}	Duty cycle [6] = $t_2 \div t_1$ (-1, -2)	Measured at 1.4 V, F_{OUT} = 66.66 MHz, 30-pF load	40.0	50.0	60.0	%
t_{DC}	Duty cycle [6] = $t_2 \div t_1$ (-2)	Measured at 1.4 V, F_{OUT} = 83.0 MHz, 15-pF load	40.0	50.0	60.0	%
t_{DC}	Duty cycle [6] = $t_2 \div t_1$ (-1, -2)	Measured at 1.4 V, F_{OUT} < 50 MHz, 15-pF load	45.0	50.0	55.0	%
t_3	Rise time[6] (-1, -2)	Measured between 0.8 V and 2.0 V, 30-pF load	–	–	2.20	ns
t_3	Rise time [6] (-1, -2)	Measured between 0.8 V and 2.0 V, 15-pF load	–	–	1.50	ns
t_4	Fall time [6] (-1, -2)	Measured between 0.8 V and 2.0 V, 30-pF load	–	–	2.20	ns
t_4	Fall time [6] (-1, -2)	Measured between 0.8 V and 2.0 V, 15 pF load	–	–	1.50	ns
t_5	Output-to-output skew on same Bank (-1, -2) [6]	All outputs equally loaded	–	–	200	ps
	Output bank A to output bank B skew (-1)	All outputs equally loaded	–	–	200	ps
	Output bank A to output bank B skew (-2)	All outputs equally loaded	–	–	400	ps
t_6	Skew, REF rising edge to FBK rising edge [6]	Measured at $V_{DD}/2$	–	0	±250	ps
t_7	Device-to-device skew [6]	Measured at $V_{DD}/2$ on the FBK pins of devices	–	0	500	ps
t_J	Cycle-to-cycle jitter [6] (-1)	Measured at 66.67 MHz, loaded outputs, 15-pF load	–	90	175	ps
		Measured at 66.67 MHz, loaded outputs, 30-pF load	–	–	200	ps
		Measured at 133.3 MHz, loaded outputs, 15-pF load	–	–	100	ps
t_J	Cycle-to-cycle jitter [6] (-2)	Measured at 66.67 MHz, loaded outputs 30-pF load	–	–	400	ps
		Measured at 66.67 MHz, loaded outputs 15-pF load	–	–	375	ps
t_{LOCK}	PLL lock time [6]	Stable power supply, valid clocks presented on REF and FBK pins	–	–	1.0	ms

Notes
5. All parameters are specified with loaded output.
6. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Operating Conditions

For CY2304SXI Industrial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage	3.0	3.6	V
T_A	Operating temperature (ambient temperature)	–40	85	°C
C_L	Load capacitance (below 100 MHz)	–	30	pF
	Load capacitance (from 100 MHz to 133 MHz)	–	15	pF
C_{IN}	Input capacitance	–	7	pF

Electrical Characteristics

For CY2304SXI Industrial Temperature Devices

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW voltage		–	0.8	V
V_{IH}	Input HIGH voltage		2.0	–	V
I_{IL}	Input LOW current	V_{IN} = 0 V	–	50.0	μA
I_{IH}	Input HIGH current	V_{IN} = V_{DD}	–	100.0	μA
V_{OL}	Output LOW voltage [7]	I_{OL} = 8 mA (-1, -2)	–	0.4	V
V_{OH}	Output HIGH voltage [7]	I_{OH} = –8 mA (-1, -2)	2.4	–	V
I_{DD} (PD mode)	Power-down supply current	REF = 0 MHz	–	25.0	μA
I_{DD}	Supply current	Unloaded outputs, 100 MHz, Select inputs at V_{DD} or GND	–	45.0	mA
		Unloaded outputs, 66 MHz REF (-1, -2)	–	35.0	mA
		Unloaded outputs, 33 MHz REF (-1, -2)	–	20.0	mA

Note

7. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics

for CY2304SXI Industrial Temperature Devices

Parameter [8]	Name	Test Conditions	Min	Typ	Max	Unit
t_1	Output frequency	30-pF load, All devices	10	–	100	MHz
t_1	Output frequency	15-pF load, All devices	10	–	133.3	MHz
t_{DC}	Duty cycle [9] = $t_2 \div t_1$ (-1, -2)	Measured at 1.4 V, F_{OUT} = 66.66 MHz, 30-pF load	40.0	50.0	60.0	%
t_{DC}	Duty cycle [9] = $t_2 \div t_1$ (-2)	Measured at 1.4 V, F_{OUT} = 83.0 MHz, 15-pF load	40.0	50.0	60.0	%
t_{DC}	Duty cycle [9] = $t_2 \div t_1$ (-1, -2)	Measured at 1.4 V, F_{OUT} < 50 MHz, 15-pF load	45.0	50.0	55.0	%
t_3	Rise time [9] (-1, -2)	Measured between 0.8 V and 2.0 V, 30-pF load	–	–	2.50	ns
t_3	Rise time [9] (-1, -2)	Measured between 0.8 V and 2.0 V, 15-pF load	–	–	1.50	ns
t_4	Fall time [9] (-1, -2)	Measured between 0.8 V and 2.0 V, 30-pF load	–	–	2.50	ns
t_4	Fall time [9] (-1, -2)	Measured between 0.8 V and 2.0 V, 15-pF load	–	–	1.50	ns
t_5	Output-to-output skew on same bank (-1, -2) [9]	All outputs equally loaded	–	–	200	ps
	Output bank A to output bank B skew (-1)	All outputs equally loaded	–	–	200	ps
	Output bank A to output bank B skew (-2)	All outputs equally loaded	–	–	400	ps
t_6	Skew, REF rising edge to FBK rising edge [9]	Measured at $V_{DD}/2$	–	0	±250	ps
t_7	Device-to-device skew [9]	Measured at $V_{DD}/2$ on the FBK pins of devices	–	0	500	ps
t_J	Cycle-to-cycle jitter [9] (-1)	Measured at 66.67 MHz, loaded outputs, 15-pF load	–	–	180	ps
		Measured at 66.67 MHz, loaded outputs, 30-pF load	–	–	200	ps
		Measured at 133.3 MHz, loaded outputs, 15-pF load	–	–	100	ps
t_J	Cycle-to-cycle jitter [9] (-2)	Measured at 66.67 MHz, loaded outputs, 30-pF load	–	–	400	ps
		Measured at 66.67 MHz, loaded outputs, 15-pF load	–	–	380	ps
t_{LOCK}	PLL lock time [9]	Stable power supply, valid clocks presented on REF and FBK pins	–	–	1.0	ms

Notes
8. All parameters are specified with loaded output.
9. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Waveforms

Figure 3. Duty Cycle Timing

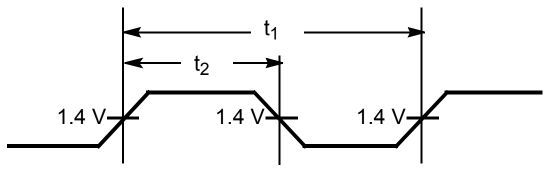


Figure 4. All Outputs Rise/Fall Time

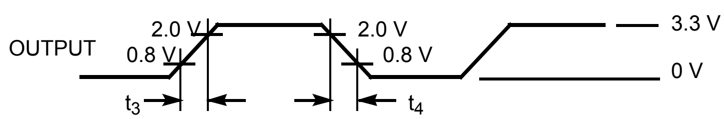


Figure 5. Output-Output Skew

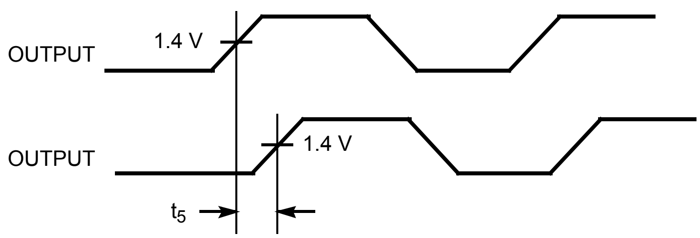


Figure 6. Input-Output Skew

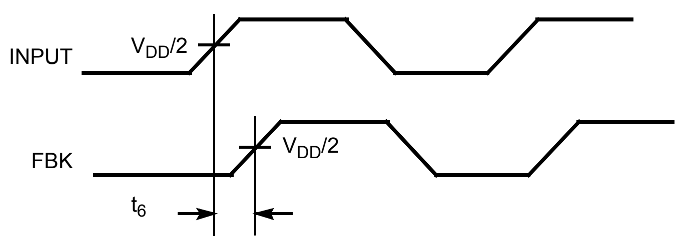


Figure 7. Device-Device Skew

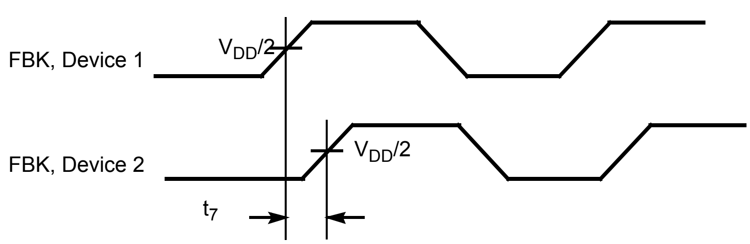
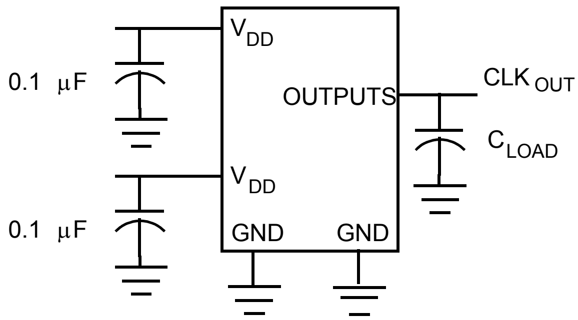


Figure 8. Test Circuit # 1

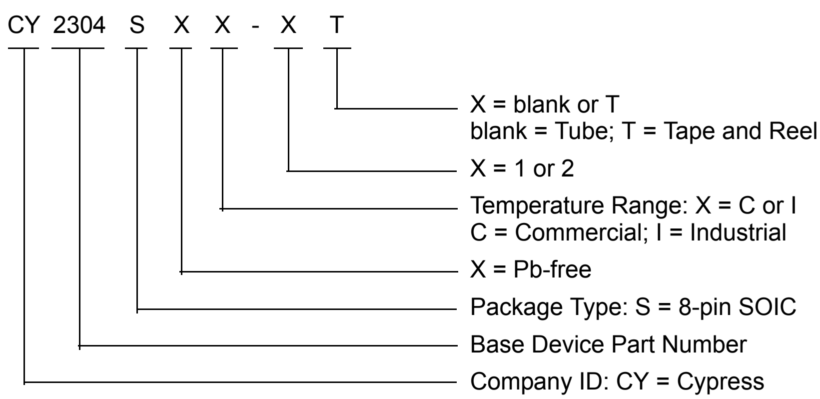


Test circuit for all parameters

Ordering Information

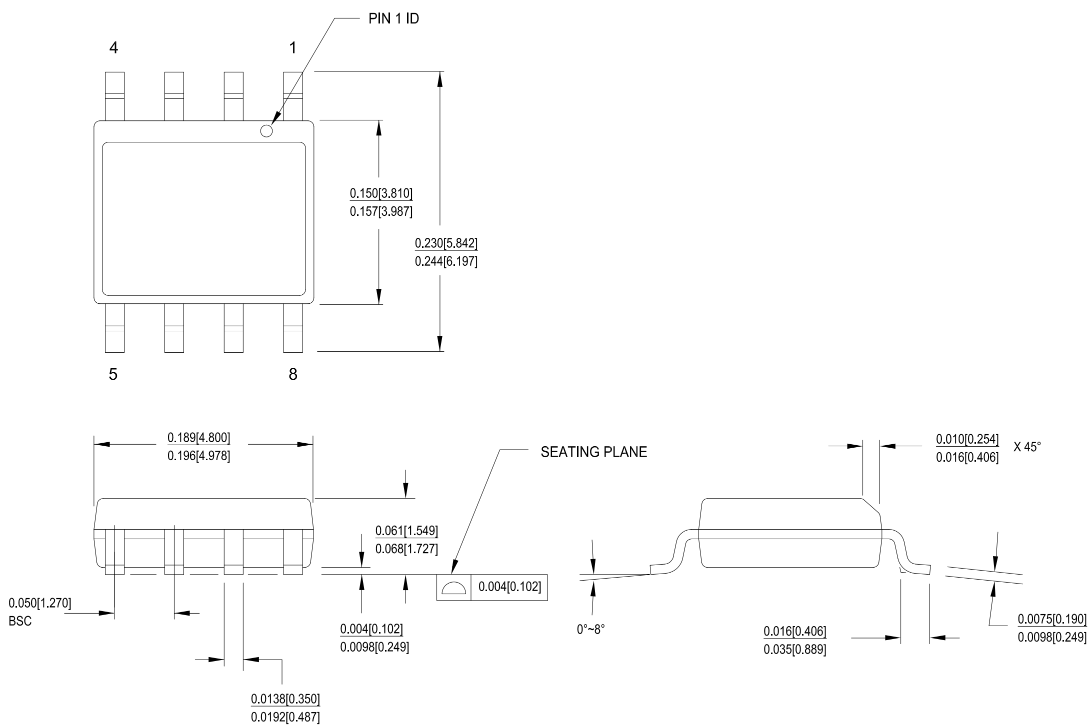
Ordering Code	Package Type	Operating Range
Pb-free		
CY2304SXC-1	8-pin SOIC (150 Mils)	Commercial
CY2304SXC-1T	8-pin SOIC (150 Mils) – Tape and Reel	Commercial
CY2304SXI-1	8-pin SOIC (150 Mils)	Industrial
CY2304SXI-1T	8-pin SOIC (150 Mils) – Tape and Reel	Industrial
CY2304SXC-2	8-pin SOIC (150 Mils)	Commercial
CY2304SXC-2T	8-pin SOIC (150 Mils) – Tape and Reel	Commercial
CY2304SXI-2	8-pin SOIC (150 Mils)	Industrial
CY2304SXI-2T	8-pin SOIC (150 Mils) – Tape and Reel	Industrial

Ordering Code Definitions



Package Diagram

Figure 9. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066



51-85066 *F

Acronyms

Acronym	Description
PLL	Phase Locked Loop
SOIC	Small Outline Integrated Circuit

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
ns	nanosecond
pF	picofarad
ps	picosecond
V	volt

Appendix: Silicon Errata for the Zero Delay Clock Buffers, CY2304

This section describes the errors, workaround solution and silicon design fixes for Cypress zero delay clock buffers belonging to the families CY2304. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Table 2. Part Numbers Affected

Part Number	Device Variants
CY2304SXC-1	All Variants
CY2304SXC-1T	All Variants
CY2304SXC-2	All Variants
CY2304SXC-2T	All Variants
CY2304SXI-1	All Variants
CY2304SXI-1T	All Variants
CY2304SXI-2	All Variants
CY2304SXI-2T	All Variants

CY2304 Errata Summary

Items	Part Number	Fix Status
Start up lock time issue [CY2304]	All	Silicon fixed. New silicon available from WW 10 of 2013

CY2303 Qualification Status of fixed silicon

Product Status: In production

Qualification report last updated on 11/27/2012

http://www.cypress.com/?rID=72595

1. Start up lock time issue

- **Problem Definition**

  Output of CY2304 fails to locks within 1 ms upon power up (as per datasheet spec)

- **Parameters Affected**

  PLL lock time

- **Trigger Condition(s)**

  Start up

- **Scope of Impact**

  It can impact the performance of system and its throughput

- **Workaround**

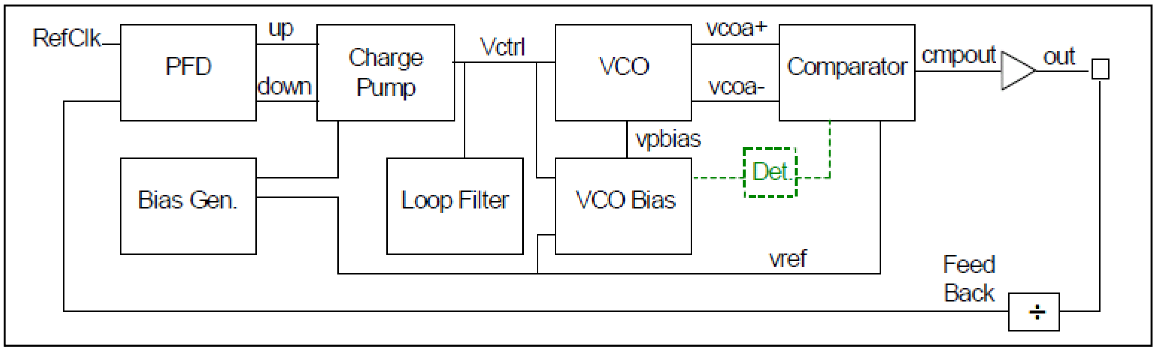
  Apply reference input (RefClk) before power up (V_{DD}). If RefClk is applied after power up, noise gets coupled on the output and propagates back to the PLL causing it to take higher time to acquire lock. If reference input is present during power up, noise will not propagate to the PLL and device will start up normally without problems.

- **Fix Status**

  This issue is due to design marginality. Two minor design modifications have been made to address this problem.

  a. Addition of VCO bias detector block as shown in the following figure keeps comparator power down till VCO bias is present and thereby eliminating the propagation of noise to feedback.

  b. Bias generator enhancement for successful initialization.


RefClk
PFD
up
down
Charge Pump
Vctrl
VCO
vcoa+
vcoa-
Comparator
cmpout
out
vpbias
Det.
Bias Gen.
Loop Filter
VCO Bias
vref
Feed Back
÷

Document History Page

Document Title: CY2304, 3.3 V Zero Delay Buffer Document Number: 38-07247				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110512	SZV	12/11/01	Change from Spec number: 38-01010 to 38-07247
*A	112294	CKN	03/04/02	On Pin Configuration Diagram (p.1), swapped CLKA2 and CLKA1
*B	113934	CKN	05/01/02	Added Operating Conditions for CY2304SI-X Industrial Temperature Devices, p. 4
*C	121851	RBI	12/14/02	Power up requirements added to Operating Conditions Information
*D	308436	RGL	01/26/05	Added Lead-free Devices
*E	2542331	AESA	09/18/08	Updated template. Added Note “Not recommended for new designs.” Removed part number CY2304SI-2 and CY2304SI-2T. Changed Lead-Free to Pb-Free. Changed IDD (PD mode) from 12.0 to 25.0 μA. Deleted Duty Cycle parameters for F_{OUT} < 50.0 MHz for commercial and industrial devices.
*F	2673353	KVM / PYRS	03/13/09	Reverted IDD (PD mode) and Duty Cycle parameters back to the values in revision *D: Changed IDD (PD mode) from 25 to 12 μA for commercial devices. Added Duty Cycle parameters for F_{OUT} < 50.0 MHz for commercial and industrial devices.
*G	2906571	KVM	04/07/10	Removed parts CY2304SC-1, CY2304SC-1T,CY2304SC-2,CY2304SC-2T,CY2304SI-1,CY2304SI-1T from the ordering information table. Updated Package Diagram.
*H	3072674	BASH	10/27/2010	Corrected part number in all table titles (pages 3 to 5) from CY2304SC-X and CY2304SI-X to CY2304SXC and CY2304SXI. Removed “except t_8” from Figure 7
*I	3162681	BASH	02/04/2011	Updated in new template.
*J	3204827	CXQ	03/24/2011	Added duty cycle spec for 83.0 MHz output condition.
*K	4018186	CINM	06/10/2013	Updated Package Diagram: spec 51-85066 – Changed revision from *D to *F. Added Appendix: Silicon Errata for the Zero Delay Clock Buffers, CY2304.

Sales, Solutions, and Legal Information

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