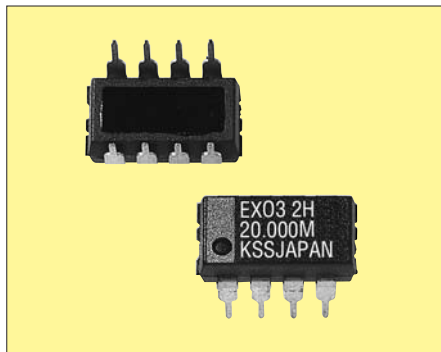


CMOS/ 5.0V



Ph Free

RoHS Compliant

### Features

- Since it has a frequency dividing function, it is able to obtain a frequency division of  $1/2 - 1/2^8$  ( $1/256$ )
- The symmetry of frequency divided output is within  $50 \pm 2\%$
- The oscillation start time has the fast starting characteristic of being 1.5m sec. or less
- The pin arrangement is DIP 8PIN
- Supply voltage  $V_{CC}=5.0V$

### Applications

- Amusement

### How to Order

**KCEXO3-** 20.0000 C 5 1 B 00  
 ① ② ③ ④ ⑤ ⑥ ⑦

- ① Type
- ② Output Frequency
- ③ Output Type (CMOS)
- ④ Supply Voltage (5.0V)
- ⑤ Frequency Tolerance
- ⑥ Symmetry/ Enable Function (40/ 60%, Stand-by)
- ⑦ Customer Special Model Suffix (STD Specification is "00")

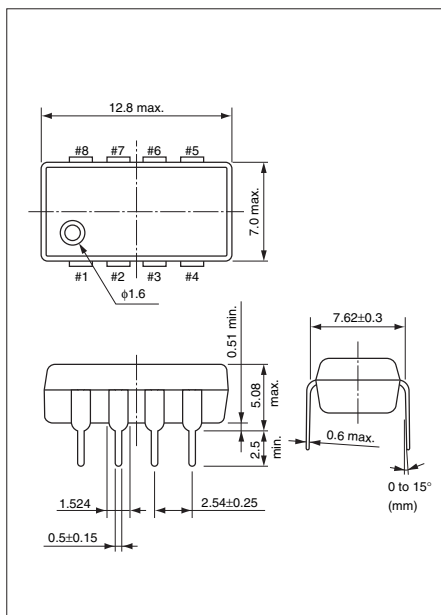
### Specifications

Item	Symbol	Conditions	Specifications		Units
			Min.	Max.	
Output Frequency Range	F <sub>o</sub>		11.0592	24.576	MHz
Frequency Tolerance (Overall)	F <sub>tol</sub>		-100	+100	$\times 10^{-6}$
Storage Temperature Range	T <sub>stg</sub>		-40	+85	°C
Operating Temperature Range	T <sub>use</sub>		-10	+70	°C
Supply Voltage	V <sub>CC</sub>		4.5	5.5	V
Current Consumption	I <sub>CC</sub>		—	20	mA
Symmetry	SYM	@50% V <sub>CC</sub>	40	60	%
Rise/ Fall Time	tr/ tf		—	15	nS
Low Level Output Voltage	V <sub>OL</sub>		—	10% V <sub>CC</sub>	V
High Level Output Voltage	V <sub>OH</sub>		90% V <sub>CC</sub>	—	V
Output Load	CL		—	50	pF
Start-up Time	t <sub>str</sub>		—	1.5	mS

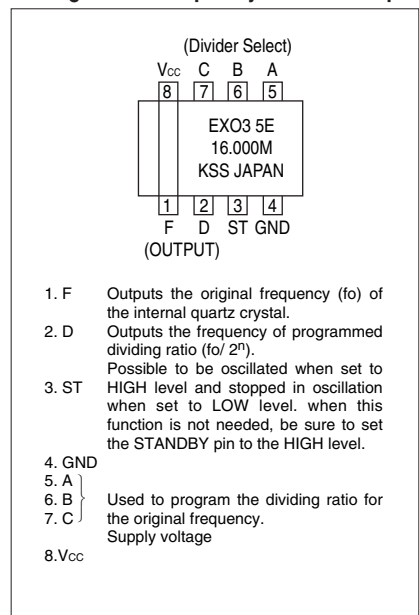
Note: All electrical characteristics are defined at the maximum load and operating temperature range.  
 Please contact us for inquiries about operating temperature range, available frequencies and other conditions.

### Dimensions

(Unit: mm)



### Settings of the frequency division output



### Pin connection

Input			Output	
Select	ST		F Original Frequency	D Divided Wave form
C	B	A	fo clock	fo · 1/2 clock
L	L	L	fo clock	fo · 1/2 <sup>2</sup> clock
L	H	L	fo clock	fo · 1/2 <sup>3</sup> clock
L	H	H	fo clock	fo · 1/2 <sup>4</sup> clock
H	L	L	fo clock	fo · 1/2 <sup>5</sup> clock
H	L	H	fo clock	fo · 1/2 <sup>6</sup> clock
H	H	L	fo clock	fo · 1/2 <sup>7</sup> clock
H	H	H	fo clock	fo · 1/2 <sup>8</sup> clock
—	—	L	L	L