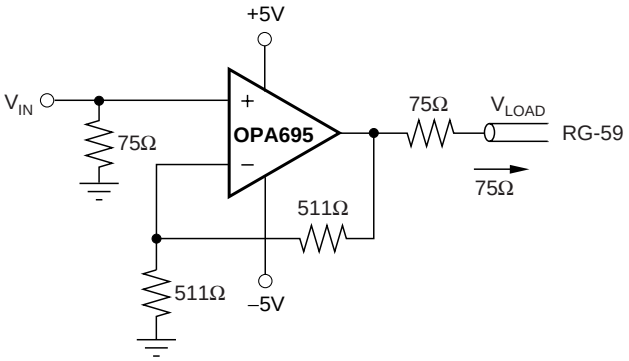
Ultra-Wideband, Current-Feedback OPERATIONAL AMPLIFIER With Disable

FEATURES

- GAIN = +2 BANDWIDTH (1400MHz)
- GAIN = +8 BANDWIDTH (450MHz)
- OUTPUT VOLTAGE SWING: ±4.2V
- ULTRA-HIGH SLEW RATE: 4300V/µs
- 3RD-ORDER INTERCEPT: > 40dBm (f < 50MHz)
- LOW POWER: 129mW
- LOW DISABLED POWER: 0.5mW
- PACKAGES: SO-8, MSOP-8, SOT23-6

APPLICATIONS

- VERY WIDEBAND ADC DRIVERS
- LOW-COST PRECISION IF AMPLIFIERS
- BROADBAND VIDEO LINE DRIVERS
- PORTABLE INSTRUMENTS
- ACTIVE FILTERS
- ARB WAVEFORM OUTPUT DRIVERS
- OPA685 PERFORMANCE UPGRADES



Gain 2V/V Video Line Driver

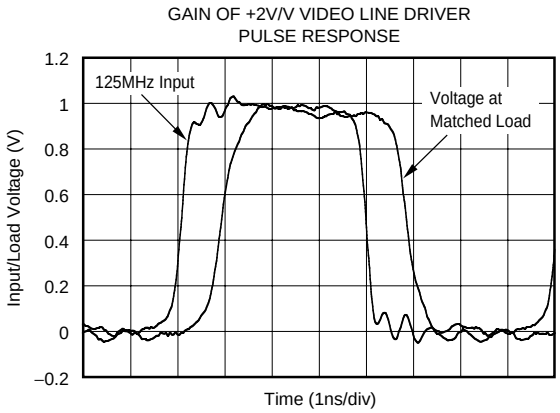
DESCRIPTION

The OPA695 is a very high bandwidth, current-feedback op amp that combines an exceptional 4300V/µs slew rate and a low input voltage noise to deliver a precision, low-cost, high dynamic range Intermediate Frequency (IF) amplifier. Optimized for high gain operation, the OPA695 is ideally suited to buffering Surface Acoustic Wave (SAW) filters in an IF strip or delivering high output power at low distortion for cable-modem upstream line drivers. At lower gains, a higher bandwidth of 1400MHz is achievable, making the OPA695 an excellent video line driver for supporting high-resolution RGB applications.

The OPA695 low 12.9mA supply current is precisely trimmed at +25°C. This trim, along with a low temperature drift, gives low system power over temperature. System power may be further reduced using the optional disable control pin. Leaving this pin open, or holding it HIGH, gives normal operation. If pulled LOW, the OPA695 supply current drops to less than 170µA. This power-saving feature, along with exceptional single +5V operation and ultra-small SOT23-6 packaging, make the OPA695 ideal for portable applications.

OPA695 RELATED PRODUCTS

SINGLES	DUALS
OPA694	OPA2694
OPA691	OPA2691
OPA692	THS3202
OPA693	—



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	±6.5V_{DC}
Internal Power Dissipation	See Thermal Analysis
Differential Input Voltage	±1.2V
Input Common-Mode Voltage Range	±V_S
Storage Temperature Range: D, DBV	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+150°C
ESD Rating	
Human Body Model (HBM)(2)	1500V
Charge Device Model (CDM)	1000V
Machine Model (MM)	100V

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

(2) Pin 2 on SO-8 package and pin 4 on SOT23-6 package > 500V HBM.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

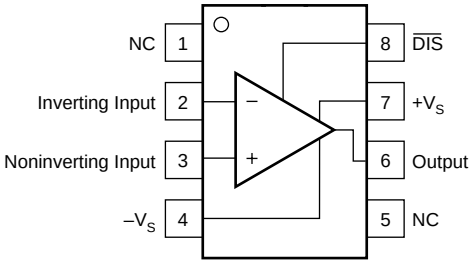
PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA695	SO-8	D	–40°C to +85°C	OPA695	OPA695ID	Rails, 100
"	"	"	"	"	OPA695IDR	Tape and Reel, 2500
OPA695	SOT23-6(2)	DBV	–40°C to +85°C	A71L	OPA695IDBVT	Tape and Reel, 250
"	"	"	"	"	OPA695IDBVR	Tape and Reel, 3000
OPA695	MSOP-8	DGK	–40°C to +85°C	695	OPA695IDGKT	Tape and Reel, 250
"	"	"	"	"	OPA695IDGKR	Tape and Reel, 2500

NOTES: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this document, or see the TI website at www.ti.com.

(2) The SOT23-6 is shipped only as a lead-free and ***green*** package. Check TI web site for lead-free availability of other packages.

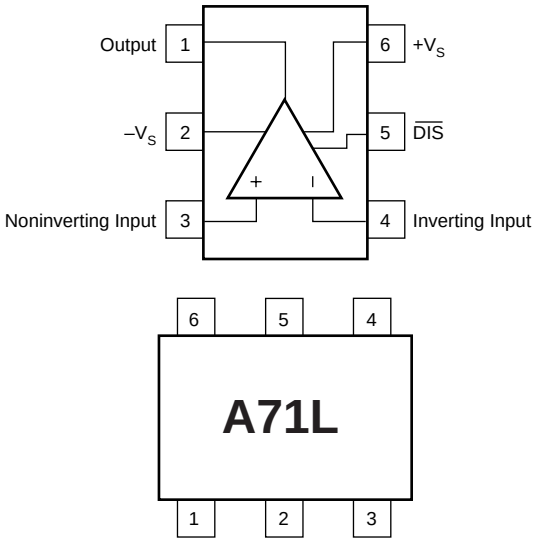
PIN CONFIGURATIONS

Top View **MSOP, SO**



NC = No Connection

Top View **SOT23**



Pin Orientation/Package Marking

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

Boldface limits are tested at **+25°C.**

$R_F = 402\Omega$, $R_L = 100\Omega$, and G = +8, (see Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA695ID, IDBV						
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	TEST LEVEL(3)
AC PERFORMANCE (see Figure 1)								
Small-Signal Bandwidth ($V_O = 0.5V_{PP}$)	G = +1, $R_F = 523\Omega$	1700				MHz	typ	C
	G = +2, $R_F = 511\Omega$	1400				MHz	typ	C
	G = +8, $R_F = 402\Omega$	450	400	380	350	MHz	min	B
	G = +16, $R_F = 249\Omega$	350				MHz	typ	C
Bandwidth for 0.2dB Gain Flatness	G = +2, $V_O = 0.5V_{PP}$, $R_F = 523\Omega$	320				MHz	min	B
Peaking at a Gain of +1	$R_F = 523\Omega$, $V_O = 0.5V_{PP}$	4.6	5.4	5.8	6.0	dB	max	B
Large-Signal Bandwidth	G = +8, $V_O = 4V_{PP}$	450				MHz	typ	C
Slew Rate	G = –8, V_O = 4V Step	4300	3700	3600	3500	V/µs	min	B
	G = +8, V_O = 4V Step	2900	2600	2500	2400	V/µs	min	B
Rise-and-Fall Time	G = +8, V_O = 0.5V Step	0.8				ns	typ	C
	G = +8, V_O = 4V Step	1.0				ns	typ	C
Settling Time to 0.02%	G = +8, V_O = 2V Step	16				ns	typ	C
0.1%	G = +8, V_O = 2V Step	10				ns	typ	C
Harmonic Distortion	G = +8, f = 10MHz, $V_O = 2V_{PP}$							
2nd-Harmonic	$R_L = 100\Omega$	–65	–62	–60	–59	dBc	max	B
	$R_L \geq 500\Omega$	–78	–76	–74	–73	dBc	max	B
3rd-Harmonic	$R_L = 100\Omega$	–86	–84	–75	–72	dBc	max	B
	$R_L \geq 500\Omega$	–86	–82	–81	–80	dBc	max	B
Input Voltage Noise	f > 1MHz	1.8	2	2.7	2.9	nV/$\sqrt{Hz}$	max	B
Noninverting Input Current Noise	f > 1MHz	18	19	21	22	pA/$\sqrt{Hz}$	max	B
Inverting Input Current Noise	f > 1MHz	22	24	26	27	pA/$\sqrt{Hz}$	max	B
Differential Gain	G = +2, NTSC, V_O = 1.4Vp, $R_L = 150\Omega$	0.04				%	typ	C
Differential Phase	G = +2, NTSC, V_O = 1.4Vp, $R_L = 150\Omega$	0.007				deg	typ	C
DC PERFORMANCE(4)								
Open-Loop Transimpedance Gain (Z_{OL})	V_O = 0V, $R_L = 100\Omega$	85	**45**	43	41	kΩ	min	A
Input Offset Voltage	V_{CM} = 0V	±0.3	**±3.0**	±3.5	±4.0	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			±10	±15	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = 0V	+13	**±30**	±37	±41	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = 0V			+150	+180	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 0V	±20	**±60**	±66	±70	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 0V			±120	±160	nA°/C	max	B
INPUT								
Common-Mode Input Range(5) (CMIR)		±3.3	**±3.1**	±3.0	±3.0	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0V	56	**51**	50	50	dB	min	A
Noninverting Input Impedance		280 || 1.2				kΩ || pF	typ	C
Inverting Input Resistance (R_I)	Open-Loop	29				Ω	typ	C
OUTPUT								
Voltage Output Swing	No Load	±4.2	**±4.0**	±3.9	±3.9	V	min	A
	100Ω Load	±3.9	**±3.7**	±3.7	±3.6	V	min	A
Current Output, Sourcing	V_O = 0	+120	**+90**	+80	+70	mA	min	A
Current Output, Sinking	V_O = 0	–120	**–90**	–80	–70	mA	min	A
Closed-Loop Output Impedance	G = +8, f = 100kHz	0.04				Ω	typ	C
DISABLE (Disabled LOW)								
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0	–100	**–170**	–186	–192	µA	typ	A
Disable Time	$V_{IN} = \pm 0.25V_{DC}$	1				µs	typ	C
Enable Time	$V_{IN} = \pm 0.25V_{DC}$	25				ns	typ	C
Off Isolation	G = +8, 10MHz	70				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn On Glitch	G = +2, $R_L = 150\Omega$, V_{IN} = 0	±100				mV	typ	C
Turn Off Glitch	G = +2, $R_L = 150\Omega$, V_{IN} = 0	±20				mV	typ	C
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0	75	**130**	143	145	µA	max	A
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage Range			**±6**	±6	±6	V	max	A
Max Quiescent Current	$V_S = \pm 5V$	12.9	**13.3**	13.7	14.1	mA	max	A
Min Quiescent Current	$V_S = \pm 5V$	12.9	**12.6**	11.8	11.0	mA	min	A
Power-Supply Rejection Ratio (–PSRR)	Input Referred	55	**51**	48	48	dB	typ	A
TEMPERATURE RANGE								
Specification: ID, IDBV		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-8		125				°C/W	typ	C
DGK MSOP-8		135				°C/W	typ	C
DBV SOT23-6		150				°C/W	typ	C

NOTES: (1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +15°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

R_F = 348Ω, R_L = 100Ω to V_S/2, and G = +8, (see Figure 3 for AC performance only), unless otherwise noted.

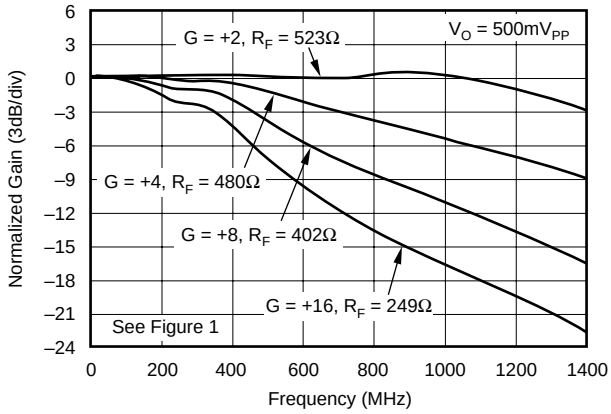
PARAMETER	CONDITIONS	OPA695ID, IDBV						TEST LEVEL(3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/MAX	
AC PERFORMANCE (see Figure 3)								
Small-Signal Bandwidth (V_O = 0.5V_{PP})	G = +1, R_F = 511Ω	1400				MHz	typ	C
	G = +2, R_F = 487Ω	960				MHz	min	C
	G = +8, R_F = 348Ω	395	380	330	300	MHz	typ	B
	G = +16, R_F = 162Ω	235				MHz	typ	C
Bandwidth for 0.2dB Gain Flatness	G = +2, V_O < 0.5V_{PP}, R_F = 487Ω	230	180	135	110	MHz	min	B
Peaking at a Gain of +1	R_F = 511Ω, V_O < 0.5V_{PP}	1.0	2.0	2.5	3.0	dB	max	B
Large-Signal Bandwidth	G = +8, V_O = 2V_{PP}	310				MHz	typ	C
Slew Rate	G = +8, 2V Step	1700	1300	1200	1100	V/µs	min	B
Rise-and-Fall Time	G = +8, V_O = 0.5V Step	1.0				ns	typ	C
	G = +8, V_O = 2V Step	1.0				ns	typ	C
Settling Time to 0.02%	G = +8, V_O = 2V Step	16				ns	typ	C
0.1%	G = +8, V_O = 2V Step	10				ns	typ	C
Harmonic Distortion	G = +8, f = 10MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω to V_S/2	–62	–58	–58	–57	dBc	max	B
	R_L ≥ 500Ω to V_S/2	–70	–66	–66	–65	dBc	max	B
3rd-Harmonic	R_L = 100Ω to V_S/2	–66	–64	–64	–63	dBc	max	B
	R_L ≥ 500Ω to V_S/2	–65	–63	–63	–62	dBc	max	B
Input Voltage Noise	f > 1MHz	1.8	2	2.7	2.9	nV/√Hz	max	B
Noninverting Input Current Noise	f > 1MHz	18	19	21	22	pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	22	24	26	27	pA/√Hz	max	B
DC PERFORMANCE(4)								
Open-Loop Transimpedance Gain (Z_{OL})	V_O = V_S/2, R_L = 100Ω to V_S/2	70	**40**	38	36	kΩ	min	A
Input Offset Voltage	V_{CM} = V_S/2	±0.3	**±3**	±3.5	±4.0	mV	max	A
Average Offset Voltage Drift	V_{CM} = V_S/2			±10	±15	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = V_S/2	±5	**±40**	±45	±50	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = V_S/2			±110	±170	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = V_S/2	±5	**±60**	±66	±70	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = V_S/2			±120	±160	nA/°C	max	B
INPUT								
Least Positive Input Voltage(5)		1.7	**1.8**	1.9	1.9	V	max	A
Most Positive Input Voltage(5)		3.3	**3.2**	3.1	3.1	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = V_S/2	54	**51**	50	50	dB	min	A
Noninverting Input Impedance		280 || 1.2				kΩ || pF	typ	C
Inverting Input Resistance (R_I)	Open-Loop	32				Ω	typ	C
OUTPUT								
Most Positive Output Voltage	No Load	4.2	**4.0**	3.9	3.8	V	min	A
	R_L = 100Ω to V_S/2	4.0	**3.9**	3.8	3.7	V	min	A
Least Positive Output Voltage	No Load	0.8	**1.0**	1.1	1.2	V	max	A
	R_L = 100Ω to V_S/2	1.0	**1.1**	1.2	1.3	V	max	A
Current Output, Sourcing	V_O = V_S/2	90	**70**	67	66	mA	min	A
Current Output, Sinking	V_O = V_S/2	–90	**–70**	–67	–66	mA	min	A
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.05				Ω	typ	C
DISABLE (Disabled LOW)								
Power Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0	–95	–160	–175	–180	µA	typ	C
Disable Time		1				µs	typ	C
Enable Time		25				ns	typ	C
Off Isolation	G = +8, 10MHz	70				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn On Glitch	G = +2, R_L = 150Ω, V_{IN} = V_S/2	±100				mV	typ	C
Turn Off Glitch	G = +2, R_L = 150Ω, V_{IN} = V_S/2	±20				mV	typ	C
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0	75	130	143	149	µA	typ	C
POWER SUPPLY								
Specified Single-Supply Operating Voltage		5				V	typ	C
Max Single-Supply Operating Voltage			**12**	12	12	V	max	A
Max Quiescent Current	V_S = +5V	11.4	**12.0**	12.5	12.9	mA	max	A
Min Quiescent Current	V_S = +5V	11.4	**10.9**	9.4	9.1	mA	min	A
Power-Supply Rejection Ratio (–PSRR)	Input Referred	56				dB	typ	C
TEMPERATURE RANGE								
Specification: ID, IDBV		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-8		125				°C/W	typ	C
DGK MSOP-8		135				°C/W	typ	C
DBV SOT23-6		150				°C/W	typ	C

NOTES: (1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limit: junction temperature = ambient +15°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

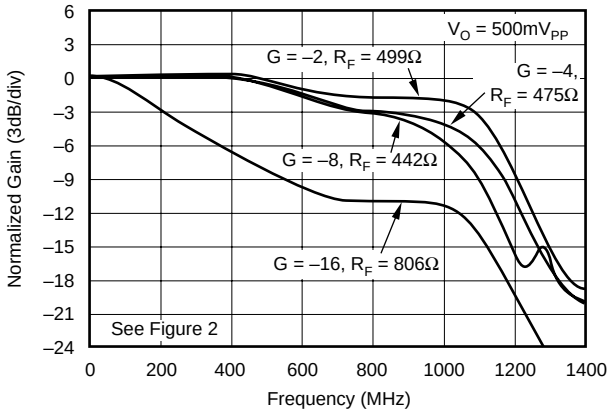
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

G = +8, R_F = 402Ω, R_L = 100Ω, unless otherwise noted.

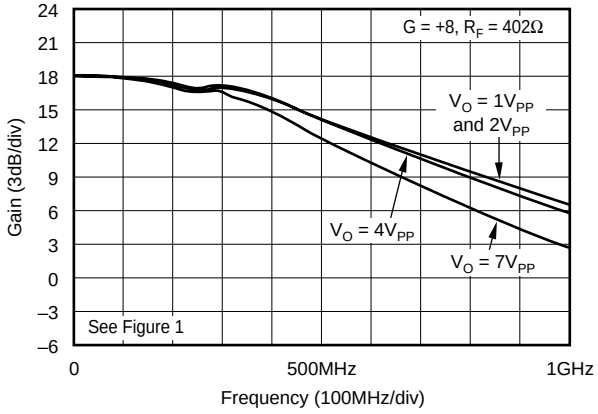
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



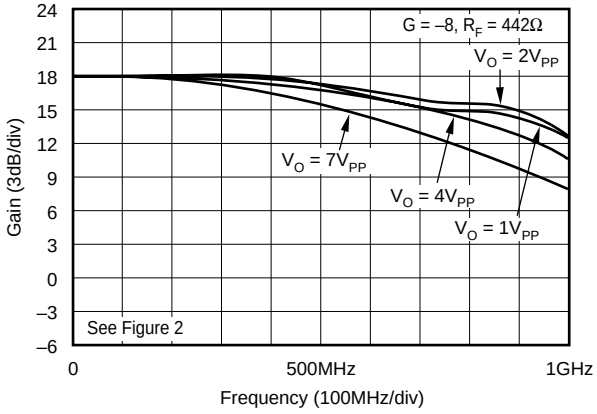
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



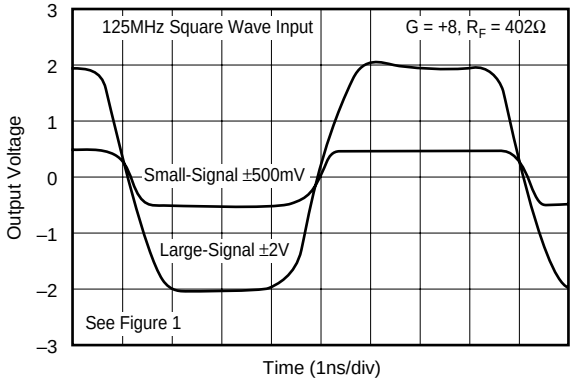
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE



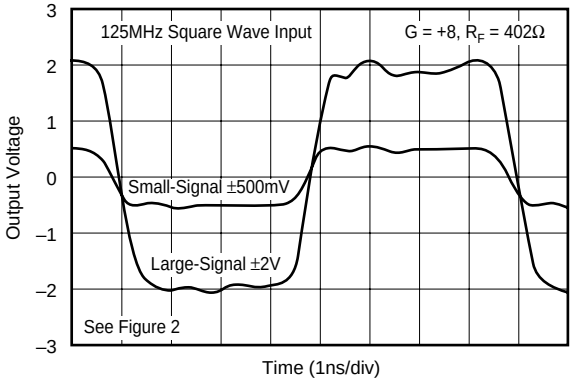
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



NONINVERTING LARGE AND SMALL-SIGNAL PULSE RESPONSE



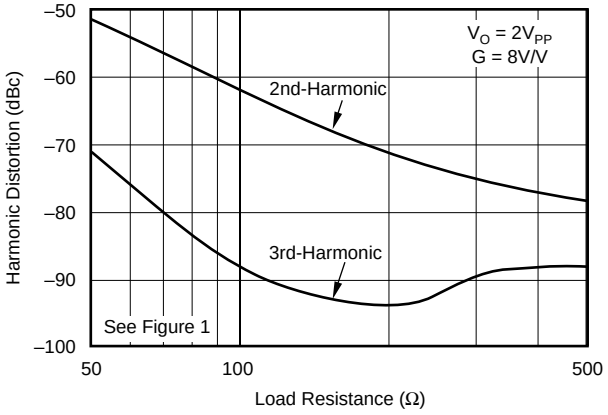
INVERTING LARGE AND SMALL-SIGNAL PULSE RESPONSE



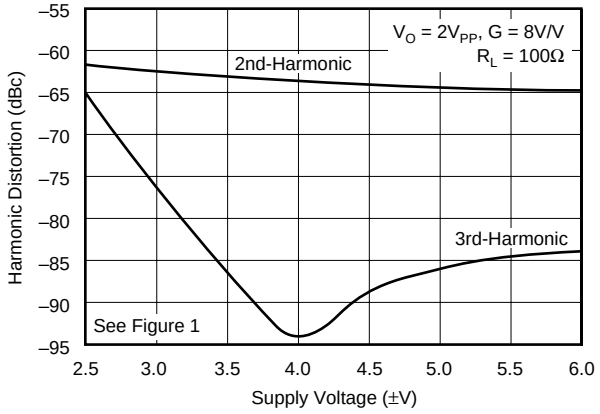
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

$G = +8$, $R_F = 402\Omega$, $R_L = 100\Omega$, unless otherwise noted.

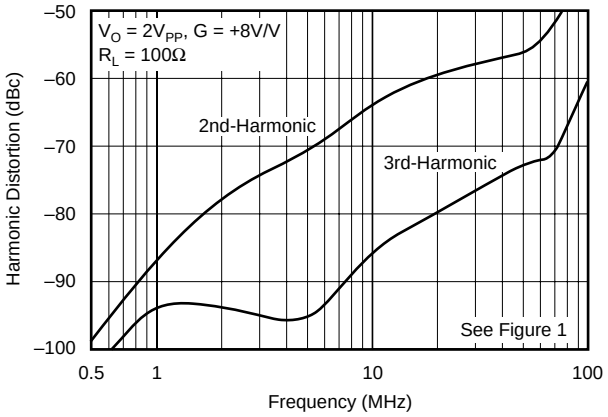
10MHz HARMONIC DISTORTION vs LOAD RESISTANCE



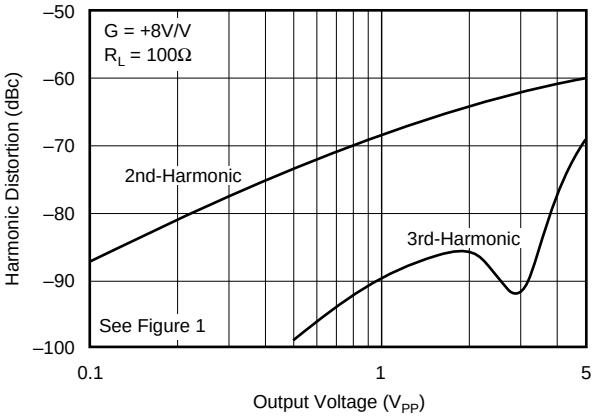
10MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE



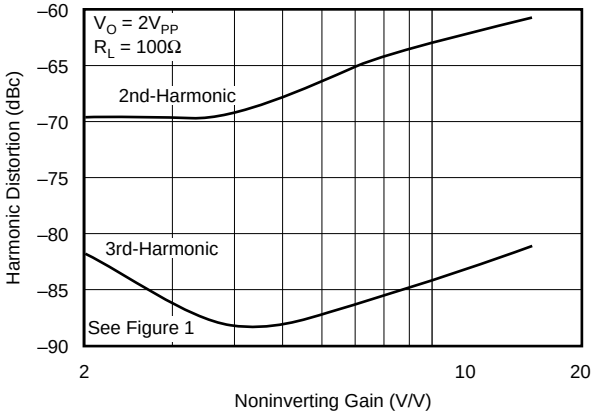
HARMONIC DISTORTION vs FREQUENCY



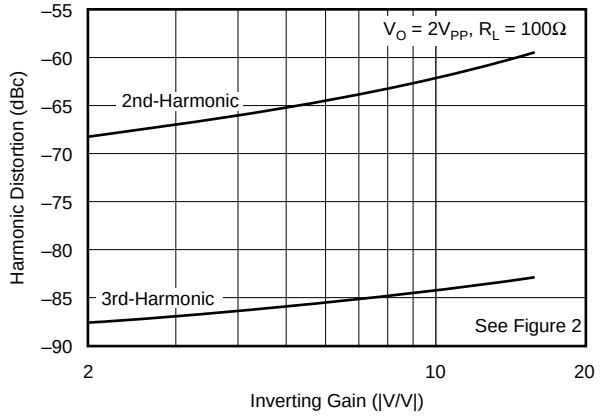
10MHz HARMONIC DISTORTION vs OUTPUT VOLTAGE



10MHz HARMONIC DISTORTION vs NONINVERTING GAIN



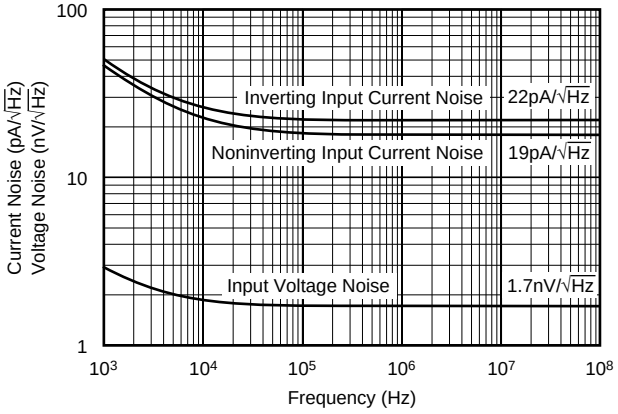
10MHz HARMONIC DISTORTION vs INVERTING GAIN



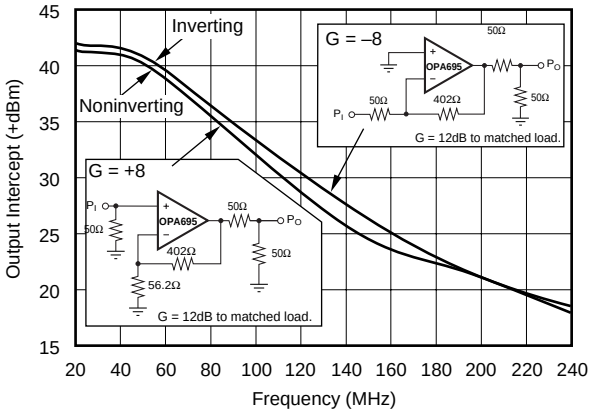
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

G = +8, R_F = 402Ω, R_L = 100Ω, unless otherwise noted.

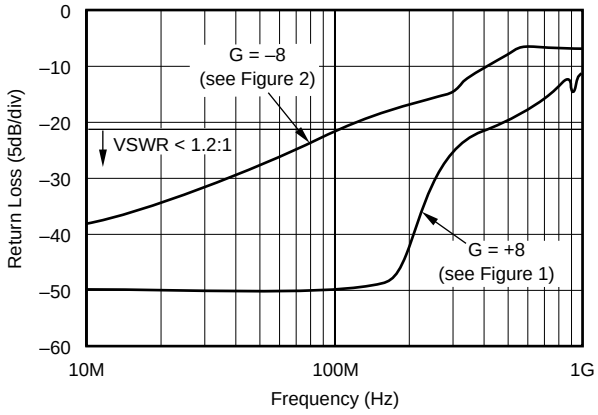
INPUT VOLTAGE AND CURRENT NOISE DENSITY



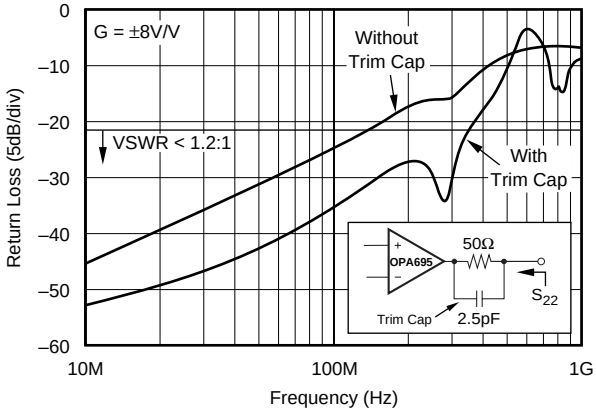
TWO-TONE, 3rd-ORDER INTERMODULATION INTERCEPT ±5V



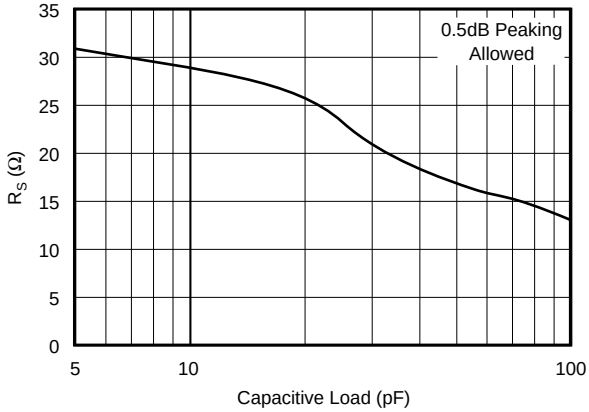
INPUT RETURN LOSS vs FREQUENCY (S_{11})



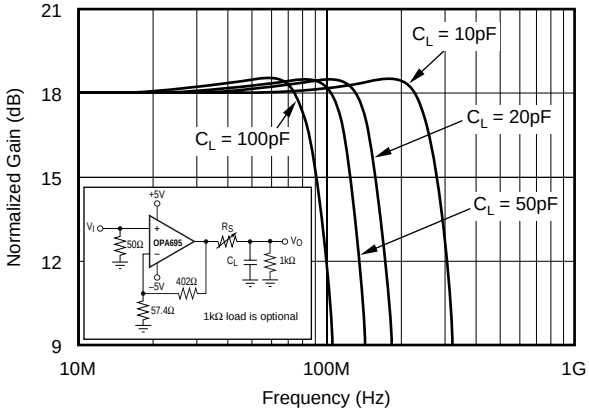
OUTPUT RETURN LOSS vs FREQUENCY (S_{22})



R_S vs CAPACITIVE LOAD



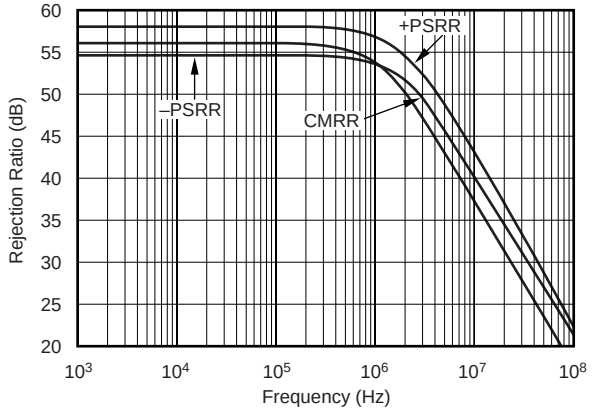
SMALL-SIGNAL FREQUENCY RESPONSE vs CAPACITIVE LOAD



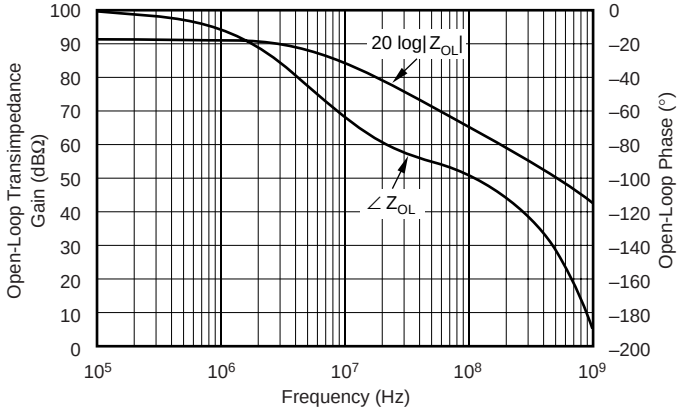
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

G = +8, R_F = 402Ω, R_L = 100Ω, unless otherwise noted.

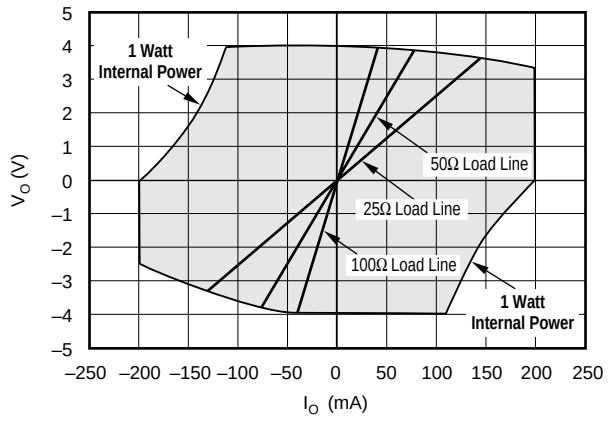
CMRR AND PSRR vs FREQUENCY



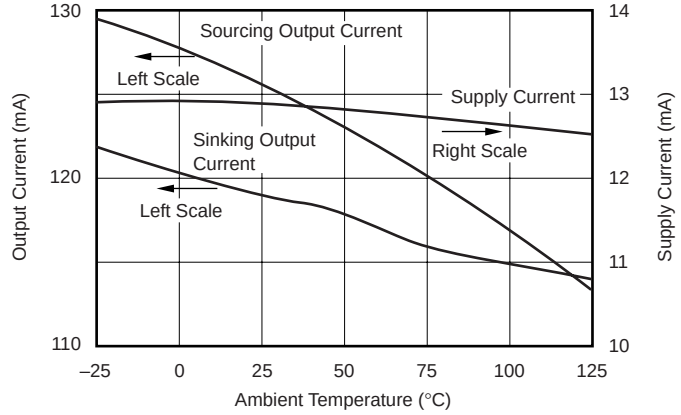
OPEN-LOOP TRANSIMPEDANCE GAIN AND PHASE



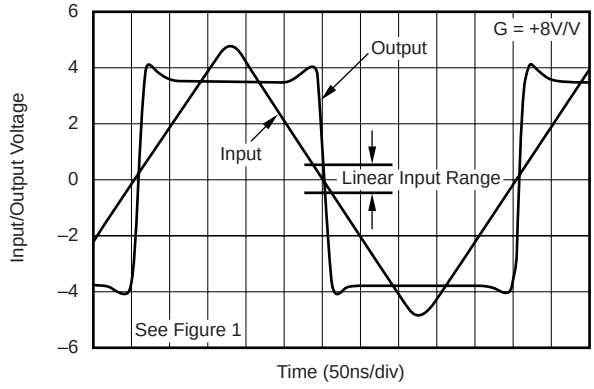
OUTPUT VOLTAGE AND CURRENT LIMITATIONS



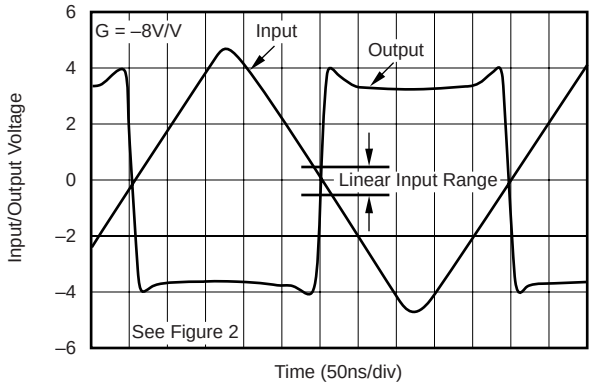
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



NONINVERTING OVERDRIVE RECOVERY



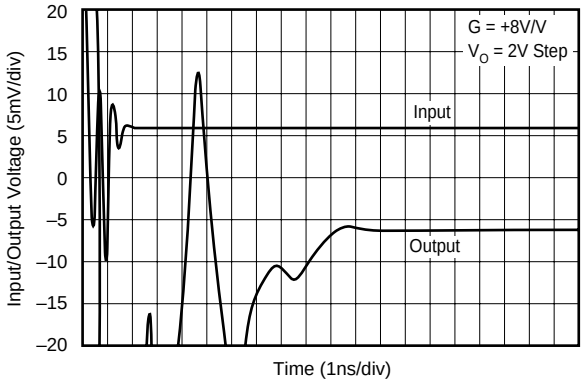
INVERTING OVERDRIVE RECOVERY



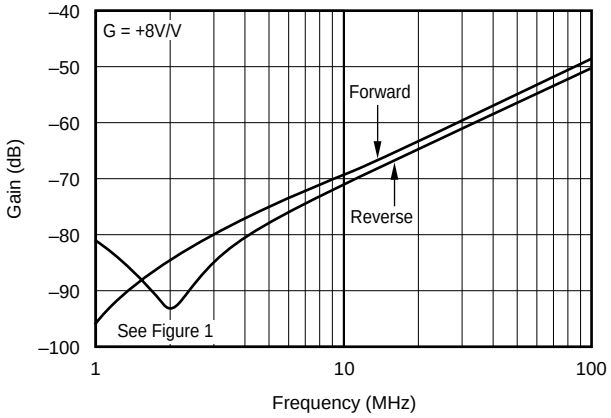
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

G = +8, R_F = 402Ω, R_L = 100Ω, unless otherwise noted.

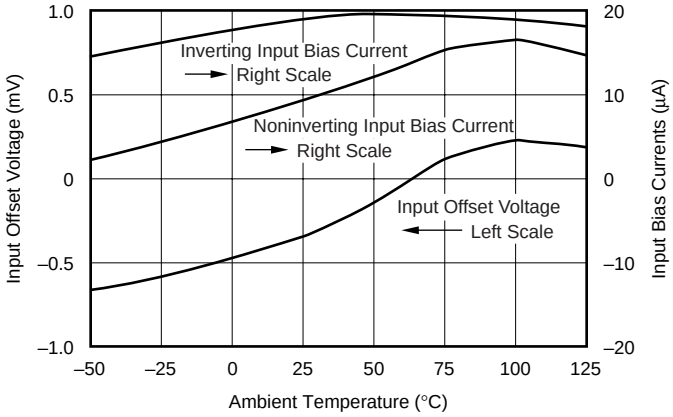
SETTLING TIME



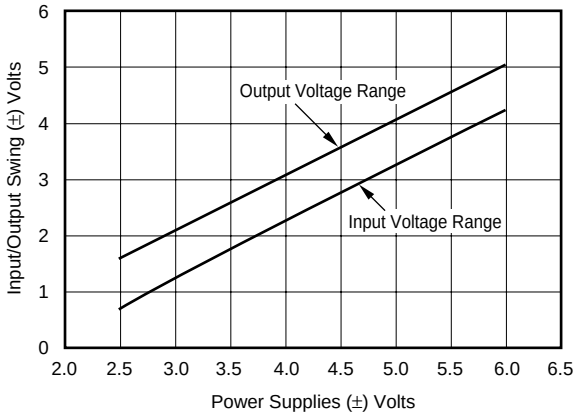
DISABLED FEEDTHROUGH vs FREQUENCY



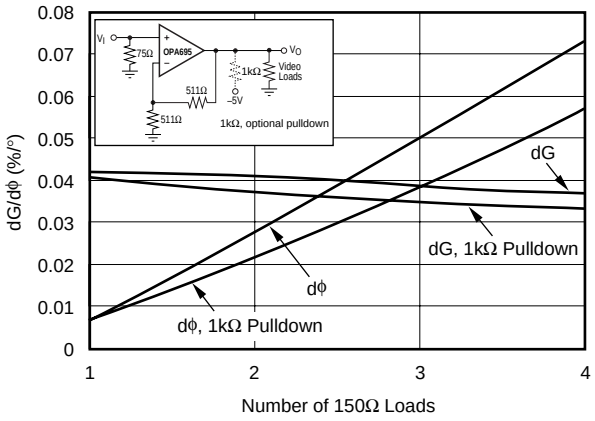
TYPICAL DC DRIFT OVER TEMPERATURE



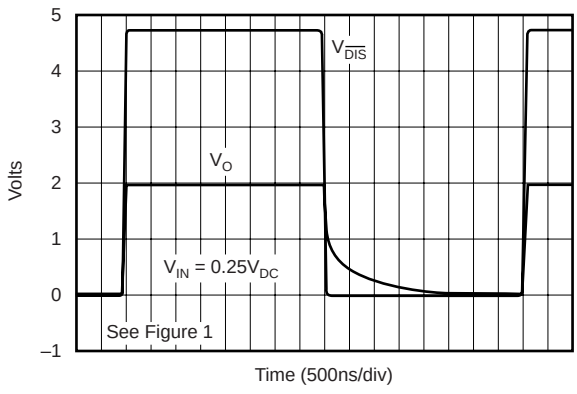
COMMON-MODE INPUT AND OUTPUT SWING vs SUPPLY VOLTAGE



COMPOSITE VIDEO dG/dϕ

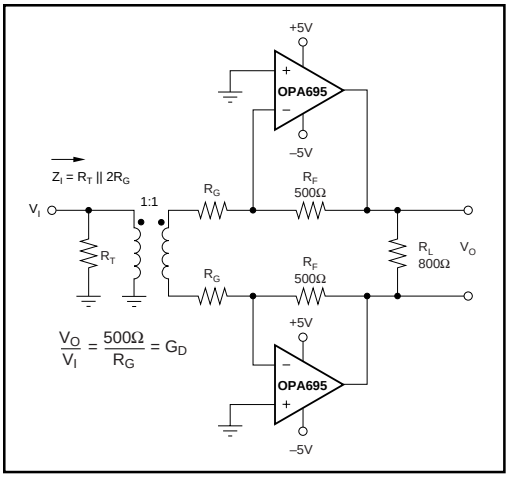


LARGE-SIGNAL DISABLE/ENABLE RESPONSE

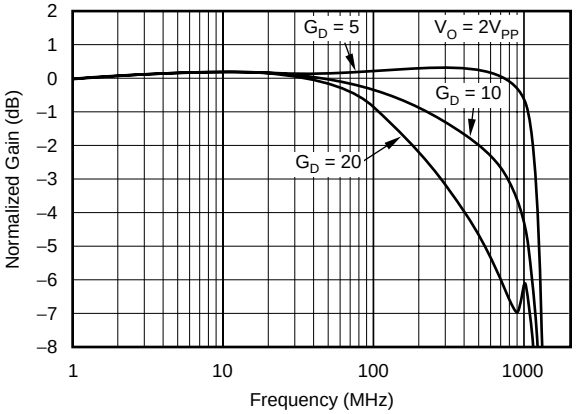


TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ Differential Operation

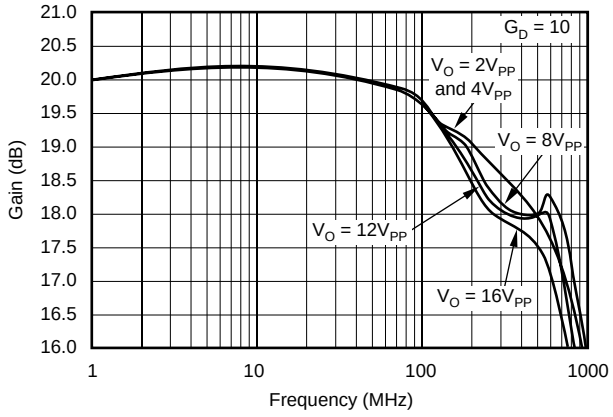
$G_D = 10$, $R_F = 500\Omega$, $R_L = 800\Omega$, unless otherwise noted.



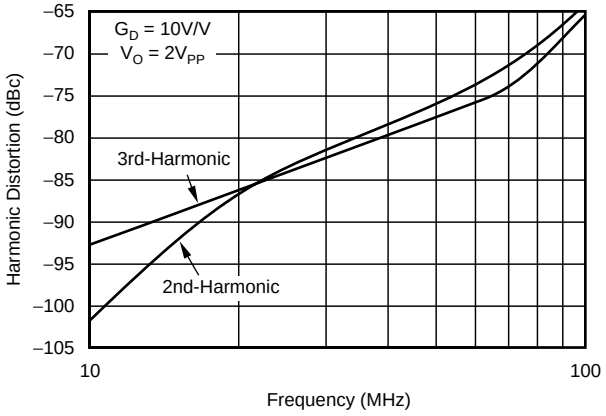
DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE



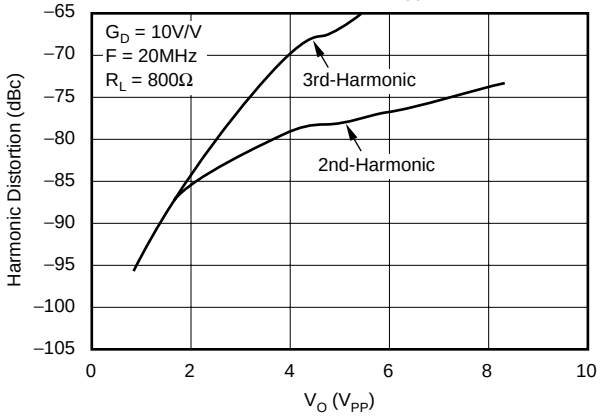
LARGE-SIGNAL BANDWIDTH



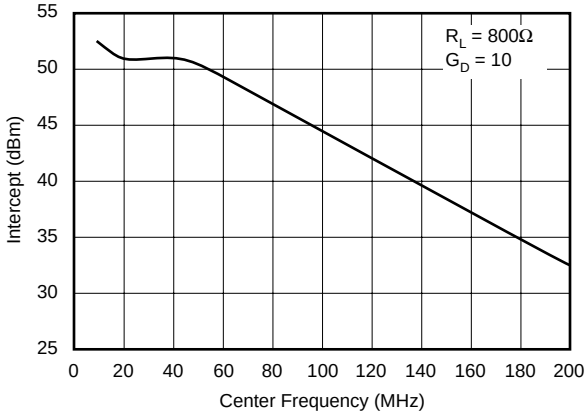
DISTORTION vs FREQUENCY



DISTORTION vs V_{OUT}



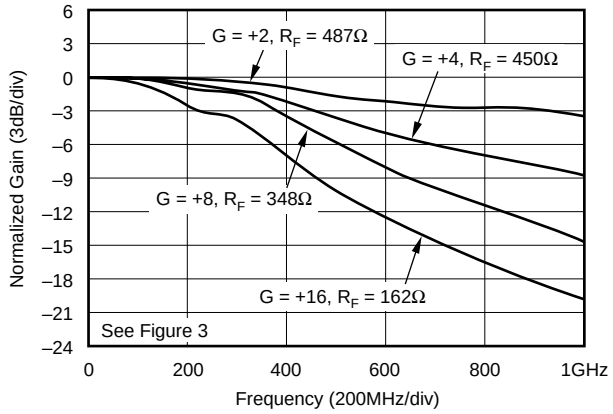
2-TONE, 3RD-ORDER INTERMODULATION INTERCEPT



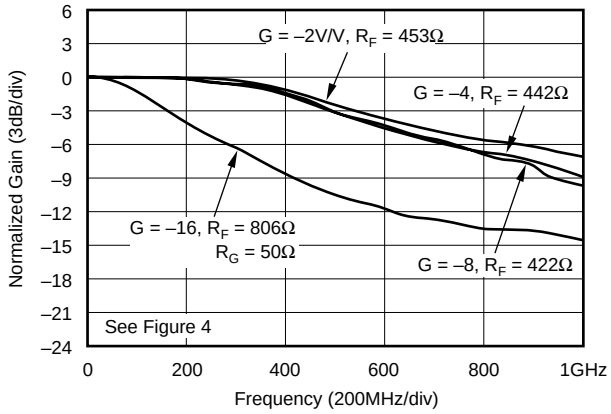
TYPICAL CHARACTERISTICS: V_S = +5V

V_S = +5V, G = +8, R_F = 348Ω, R_L = 100Ω, unless otherwise noted.

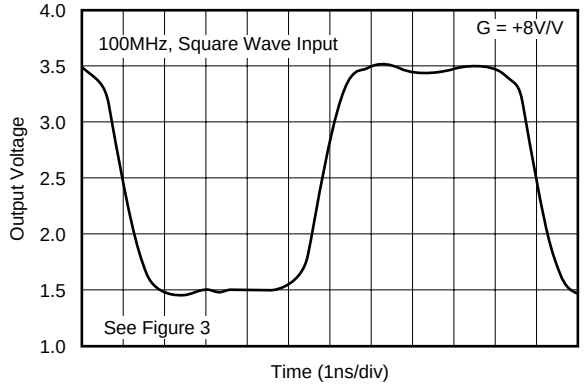
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



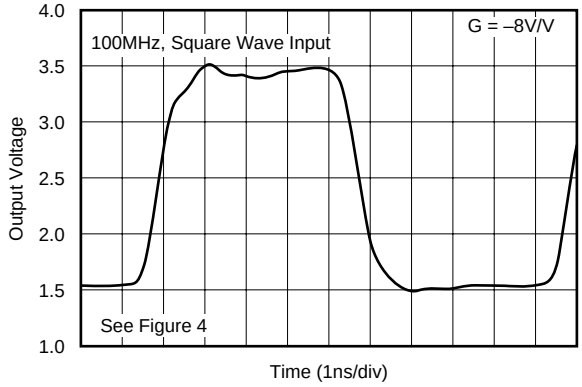
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



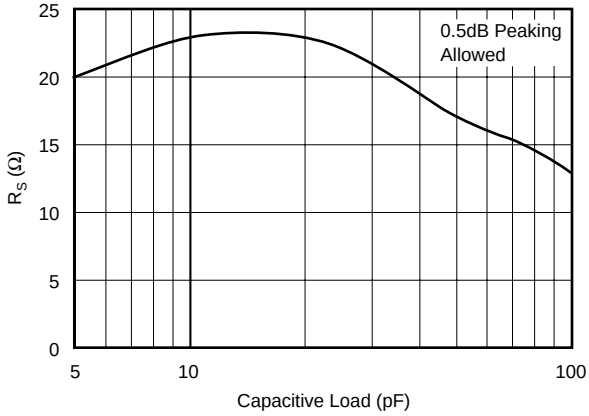
NONINVERTING PULSE RESPONSE



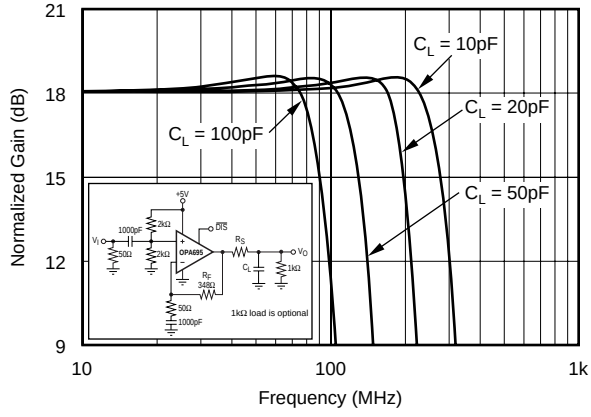
INVERTING PULSE RESPONSE



R_S vs CAPACITIVE LOAD



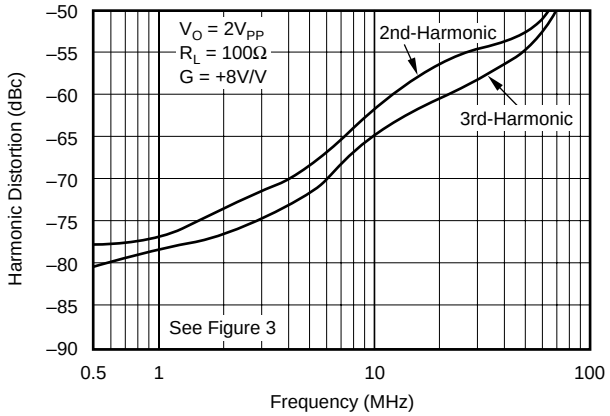
SMALL-SIGNAL FREQUENCY RESPONSE vs CAPACITIVE LOAD



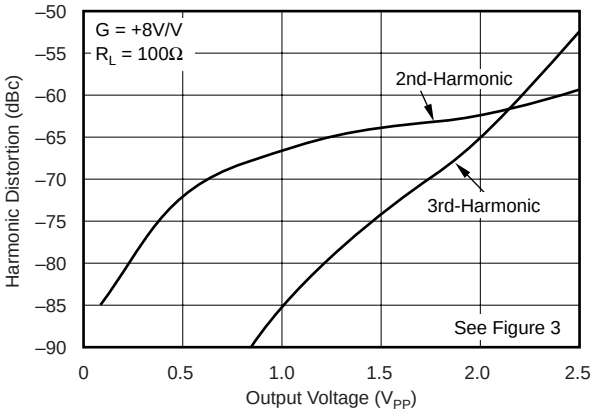
TYPICAL CHARACTERISTICS: V_S = +5V (Cont.)

V_S = +5V, G = +8, R_F = 348Ω, R_L = 100Ω, unless otherwise noted.

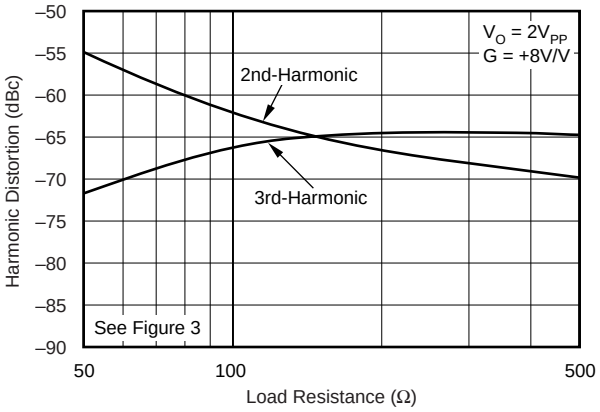
HARMONIC DISTORTION vs FREQUENCY



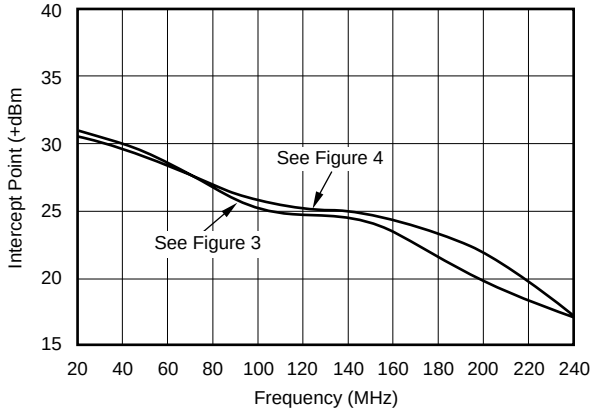
10MHz HARMONIC DISTORTION vs OUTPUT VOLTAGE



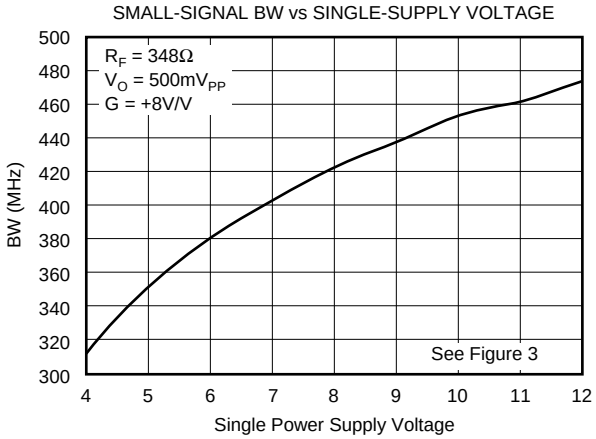
10MHz HARMONIC DISTORTION vs LOAD RESISTANCE



TWO-TONE, 3rd-ORDER INTERMODULATION INTERCEPT



SMALL-SIGNAL BW vs SINGLE-SUPPLY VOLTAGE



APPLICATIONS INFORMATION

WIDEBAND CURRENT FEEDBACK OPERATION

The OPA695 gives a new level of performance in wideband current feedback op amps. Nearly constant AC performance over a wide gain range, along with 4300V/µs slew rate, gives a lower power and cost solution for high-intercept IF amplifier requirements. While optimized at a gain of +8V/V (12dB to a matched 50Ω load) to give 450MHz bandwidth, applications from gains of 1 to 40 can be supported. **As a gain of +2 video line driver, the bandwidth extends to 1.4GHz with a slew rate to support the highest pixel rates.** At gains above 20, the signal bandwidth starts to decrease, but still exceeds 180MHz up to a gain of 40V/V (26dB to a matched 50Ω load). Single +5V supply operation is also supported with similar bandwidths but reduced output power capability. For lower speed (< 250MHz) requirements with higher output powers, consider the OPA691.

Figure 1 shows the DC-coupled, gain of +8V/V, dual power supply circuit used as the basis of the ±5V Specifications and Typical Characteristic curves. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins while load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 1, the total effective load will be 100Ω || 458Ω = 82Ω. The disable control line ($\overline{DIS}$) is typically left open to get normal amplifier operation. The disable line must be asserted low to shut off the OPA695. One optional component is included in Figure 1. In addition to the usual power supply decoupling capacitors to ground, a 0.01µF capacitor is included between the two power supply pins. In practical PC board layouts, this optional added capacitor will typically improve the 2nd-harmonic distortion performance by 3dB to 6dB for bipolar supply operation.

Figure 2 shows the DC-coupled, gain of –8V/V, dual power supply circuit used as the basis of the Inverting Typical Characteristic curves. Inverting operation offers several performance benefits. Since there is no common mode signal across the input stage, the slew rate for inverting operation is higher and the distortion performance is slightly improved. An additional input resistor, R_T, is included in Figure 2 to set the input impedance equal to 50Ω. The parallel combination of R_T and R_G set the input impedance. Both the non-inverting and inverting applications of Figures 1 and 2 will benefit from optimizing the feedback resistor (R_F) value for bandwidth (see the discussion in *Setting Resistor Values to Optimize Bandwidth*). The typical design sequence is to select the R_F value for best bandwidth, set R_G for the gain, then set R_T for the desired input impedance. As the gain increases for the inverting configuration, a point will be reached where R_G will equal 50Ω, where R_T is removed and the input match is set by R_G only. With R_G fixed to achieve an input match to 50Ω, R_F is simply increased, to increase gain. This will, however, quickly reduce the achievable bandwidth, as shown by the inverting gain of –16 frequency response in the Typical Characteristic curves. For gains > 10V/V (14dB at the matched load), noninverting operation is recommended to maintain broader bandwidth.

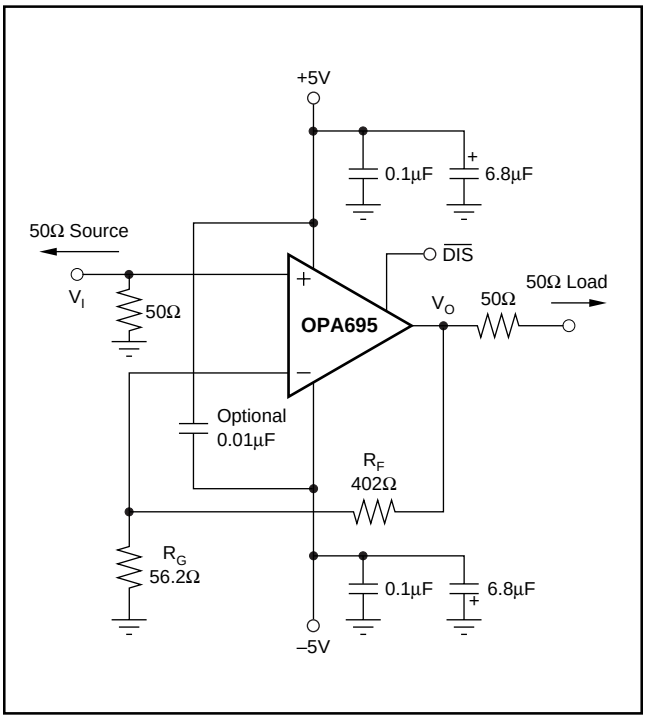


FIGURE 1. DC-Coupled, G = +8V/V, Bipolar Supply Specifications and Test Circuit.

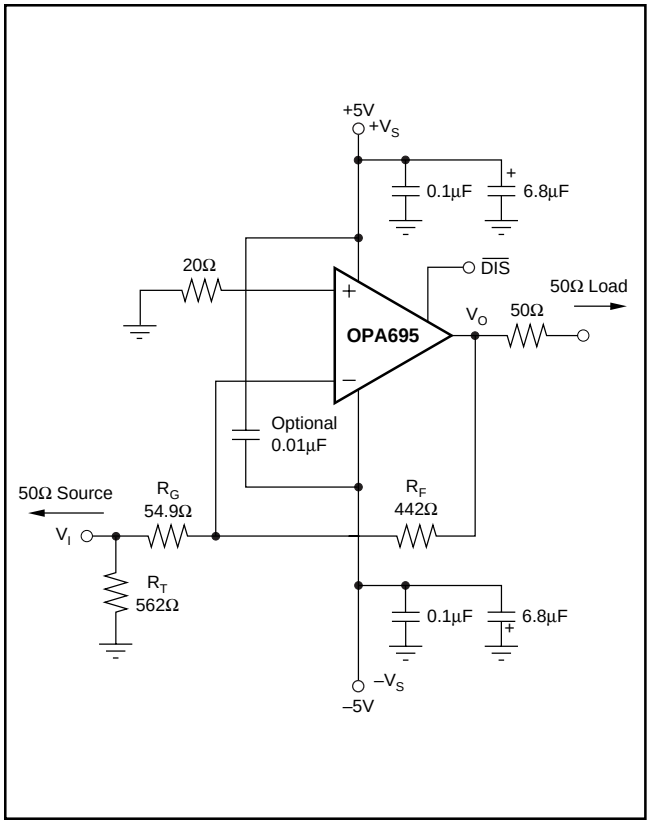


FIGURE 2. DC-Coupled, G = –8V/V, Bipolar Supply Specifications and Test Circuit.

Figure 3 shows the AC-coupled, single +5V supply, gain of +8V/V circuit configuration used as a basis for the +5V only Specifications and Typical Characteristic curves. The key requirement for broadband single-supply operation is to maintain input and output signal swings within the useable voltage ranges at both the input and the output. The circuit of Figure 3 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 806Ω resistors) to the noninverting input. The input signal is then AC-coupled into this midpoint voltage bias. The input voltage can swing to within 1.6V of either supply pin, giving a $1.8V_{PP}$ input signal range centered between the supply pins. The input impedance matching resistor (57.6Ω) used in Figure 3 is adjusted to give a 50Ω input match when the parallel combination of the biasing divider network is included. The gain resistor (R_G) is AC-coupled, giving the circuit a DC gain of +1. This puts the input DC bias voltage (2.5V) on the output as well. The feedback resistor value has been adjusted from the bipolar supply condition to re-optimize for a flat frequency response in +5V only, gain of +8 operation (see Setting Resistor Values to Optimize Bandwidth). On a single +5V supply, the output voltage can swing to within 1.0V of either supply pin while delivering more than 90mA output current giving 3V output swing into 100Ω (7dBm maximum at the matched load). The circuit of Figure 3 shows a blocking capacitor driving into a 50Ω output resistor then into a 50Ω load. Alternatively, the blocking capacitor could be removed with the load tied to a supply midpoint or to ground if the DC current required by this grounded load is acceptable.

Figure 4 shows the AC-coupled, single +5V supply, gain of –8V/V circuit configuration used as a basis for the +5V only Typical Characteristic curves. In this case, the midpoint DC bias on the noninverting input is also de-coupled with an additional 0.1µF decoupling capacitor. This reduces the source impedance at higher frequencies for the noninverting input bias current noise. This 2.5V bias on the noninverting input pin appears on the inverting input pin and, since R_G is DC blocked by the input capacitor, will also appear at the output pin. One advantage to inverting operation is that since there is no signal swing across the input stage, higher slew rates and operation to even lower supply voltages are possible. To retain a $1V_{PP}$ output capability, operation down to a 3V supply is allowed. At a +3V supply, the input common mode range is 0V. However, for the inverting configuration of a current feedback amplifier, wideband operation is retained even with the input stage saturated.

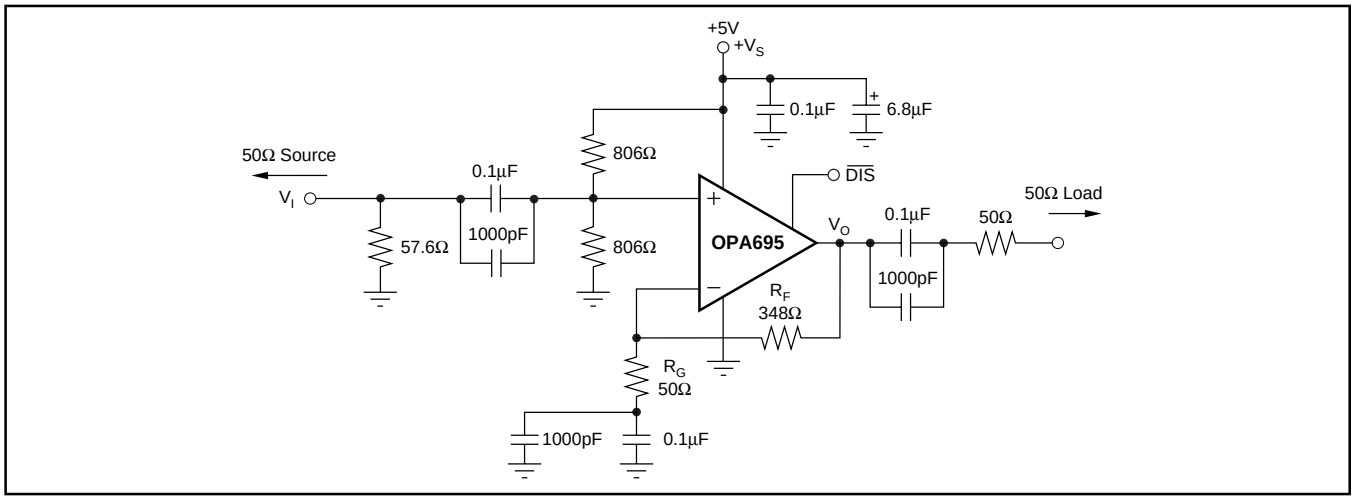


FIGURE 3. AC-Coupled, G = +8V/V, Single-Supply Specifications and Test Circuit.

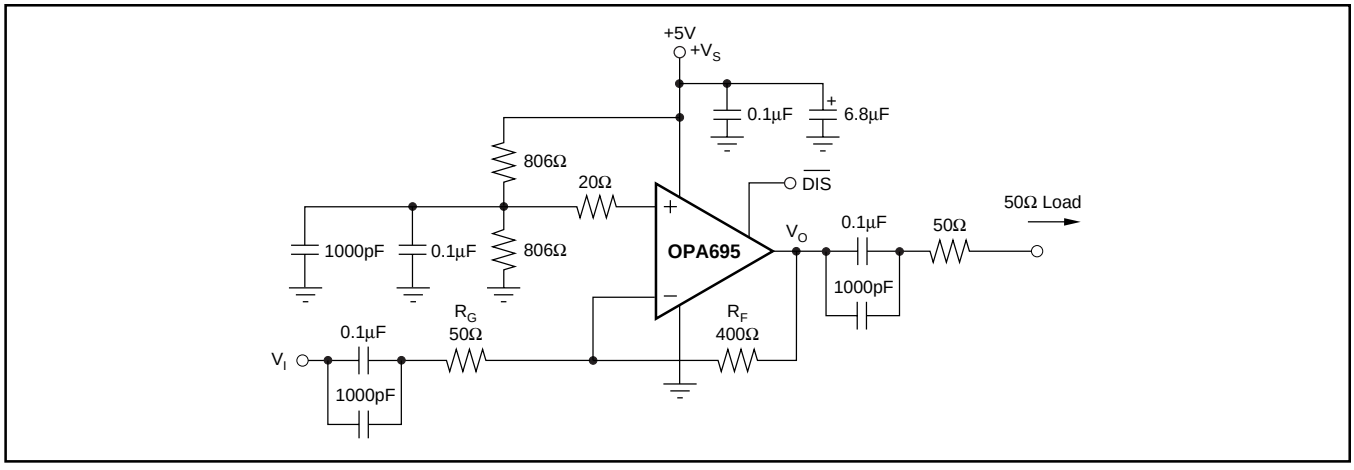


FIGURE 4. AC-Coupled, G = –8V/V, Single-Supply Specifications and Test Circuit.

The single-supply test circuits of Figures 3 and 4 show +5V operation. These same circuits can be used over a single-supply range of +5V to +12V. Operating on a single +12V supply, with the Absolute Maximum Supply voltage specification of +13V, gives adequate design margin for the typical ±5% supply tolerance.

RF SPECIFICATIONS AND APPLICATIONS

The ultra-high, full-power bandwidth and 3rd-order intercept of the OPA695 may be used to good advantage in IF amplifier applications. Additional benefits to using a wideband op amp such as the OPA695 include extremely good (and independent) I/O impedance matching as well as very high reverse isolation. A designer more accustomed to using fixed-gain RF amplifiers will get almost perfect gain accuracy, much higher I/O return loss, and 3rd-order intercept points exceeding 30dBm (up to 110MHz) using only a 13mA supply current for the OPA695. Using the considerable design freedom achieved by adjusting the external resistors, the OPA695 can replace a wide range of fixed-gain RF amplifiers with a single part. To understand (in RF amplifier terms) how to take advantage of this, consider first the 4-S parameters (this will be done using the example circuits of Figures 1 and 2 on ±5V supplies, but similar results can be obtained on a single +5V to +12V supply).

INPUT RETURN LOSS (S_{11})

Input return loss is a measure of how nearly (over frequency) the input impedance matches the source impedance. This is relatively independent of gain setting for both the noninverting and inverting configurations. The Typical Characteristic curves show the magnitude of S_{11} for the circuits of Figures 1 and 2 through 1GHz (noninverting gain of +8 and inverting gain of –8 operation, respectively). Noninverting operation does offer much better matching to higher frequencies, with the only deviation due to the parasitic input capacitance of the input pin. The noninverting input match is simply set by the resistor to ground on the noninverting input, since the amplifier itself shows a very high input impedance. Inverting operation is also very good, but rises more quickly due to loop gain roll-off effects appearing at the inverting node. The inverting mode input match is set by the parallel combination of R_G and R_T in Figure 2, since the inverting amplifier node may be considered a virtual ground. A good, fixed-gain, RF amplifier would have an input, Voltage Standing Wave Ratio (VSWR) < 1.2:1. This corresponds to an S_{11} of –21dB. The OPA695 exceeds this performance through 100MHz for the inverting mode of operation, and through 400MHz for the noninverting mode.

OUTPUT RETURN LOSS (S_{22})

Output return loss is a measure of how nearly (over frequency) the output impedance matches the load impedance. This is relatively independent of gain setting for both the noninverting and inverting configurations. The output matching impedance, to a first order, is, simply set by adding a series resistor to the low impedance output of the op amp. Since the op amp itself shows a very low output impedance that increases with frequency, an improvement in the output match can therefore be obtained by adding a small equalizing capacitor across this output resistor. The Typical Characteristic curves show the measured S_{22} with and without this 2.5pF capacitor (across the 50Ω output resistor). Again, a very good match for a fixed-gain RF amplifier would give a VSWR of 1.2:1 (S_{22} < –21dB). The Typical Characteristic curves show the measured S_{22} with and without this 2.5pF capacitor across the 50Ω output resistor. The Typical Characteristic curves show that a simple 50Ω output resistor holds better than –21dB to 140MHz, but up to 380MHz with the tuning capacitor.

FORWARD GAIN (S_{21})

In all high-speed amplifier data sheets, this is referred to as the small signal gain which is plotted over frequency. The difference between noninverting and inverting operation is that the phase of S_{21} starts out at 0° for the noninverting and –180° for the inverting. This initial phase shift for inverting mode is inconsequential to most IF strip applications. The phase of S_{21} was not shown in the Typical Characteristic curves, but is very linear with frequency and may be accurately modeled as a constant time delay through the amplifier.

The Typical Characteristic Curves for the OPA695 show S_{21} over a range of signal gains where the external resistors have been adjusted to re-optimize flatness at each gain setting. Since this is a current feedback op amp, the signal bandwidth can be held relatively constant as the desired gain setting is changed. The plot of the noninverting bandwidth versus gain shows some change in bandwidth versus gain (due to parasitic capacitive effects on the inverting node) with very little change showing up for the inverting mode of operation.

Signal gains are most often referred to as V/V in op amp data sheets. This is the voltage gain from input to output and is set by external resistor ratios. Since the output impedance is set by a physical series resistor, the voltage gain to the matched load is cut in 1/2 by this resistor divider. The log gain to the matched load for the noninverting circuit of Figure 1 is: (1)

$$G^{+} = 20\log\frac{1}{2}\left(1+\frac{R_F}{R_G}\right)\text{dB}$$

The log gain to the matched load for the inverting circuit of Figure 2 is: (2)

$$G^{-} = 20\log\frac{1}{2}\left(\frac{R_F}{R_G}\right)\text{dB}$$

The specific resistor values used in Figures 1 and 2 give both a maximally flat bandwidth and a 12dB gain to the matched load. The design tables at the end of this section summarize the required resistor values over a range of desired gains for the circuits of Figures 1 and 2.

As the desired signal gain increases, the achievable bandwidths will decrease. In the noninverting case, it decreases relatively quickly as shown in the Typical Characteristic

curves. The inverting configuration holds almost constant bandwidth (with correctly selected external resistor values) until R_G reduces to equal 50Ω, and remains at that value to satisfy the input impedance matching requirement, with further increases in gain achieved by increasing R_F in Figure 2. The bandwidth then decreases rapidly as shown by the gain of –16V/V plot in the Typical Characteristic curves.

REVERSE ISOLATION (S_{12})

Reverse isolation is a measure of how much power injected into the output pin makes it back to the source. This is rarely specified for an op amp because it is so good. Op amps are very nearly uni-directional signal devices. Below 300MHz, the noninverting configuration of Figure 1 gives much better isolation than the inverting of Figure 2. Both are well below 40dB isolation through 350MHz.

LIMITS TO DYNAMIC RANGE

The next set of considerations for RF amplifier applications are the defined limits to dynamic range. Typical fixed-gain RF amplifiers include:

- –1dB compression (a measure of maximum output power)
- Two-tone, 3rd-order, output intermodulation intercept (a measure of achievable spurious-free dynamic range)
- Noise figure (a measure of degradation in signal to noise ratio in passing through the amplifier)

–1dB COMPRESSION

The definition for –1dB compression power is that output power where the actual power is 1dB less than the input power plus the log gain. In classic RF amplifiers, this is typically 10dB less than the 3rd-order intercept. That relationship does not hold for op amps since their intercept is considerably improved by loop gain to be far more than 10dB higher than the –1dB compression. A simple estimate for –1dB compression for the OPA695 is the maximum non-slew limited output voltage swing available at the matched load converted into a power with 1dB added to satisfy the definition. For the OPA695 on ±5V supplies, its output will deliver approximately ±4.0V at the output pin or ±2.0V at the matched load. The conversion from V_{PP} to power (for a sine wave) is:

(3)

$$P_O(\text{dBm}) = 10 \log \left[\frac{\left(\frac{V_{PP}}{2\sqrt{2}} \right)^2}{0.001(50\Omega)} \right]$$

Converting this $4.0V_{PP}$ swing at the load to dBm gives 16dBm; adding 1dB to this (to satisfy the definition) gives a –1dB compression of 17dBm for the OPA695 operating on ±5V supplies. This will be a good estimate for frequencies that require less than the full slew rate of the OPA695.

The maximum frequency of operation given an available slew rate and desired peak output swing (at the output pin for a sine wave) is:

$$F_{MAX} = \frac{\text{Slew Rate}}{2\pi V_p(0.707)} \quad (4)$$

Putting in the 4600V/µs slew rate available in the inverting mode of operation and the 4.0V peak output swing at the output pin gives a maximum frequency of 259MHz. This is the maximum frequency where the –1dB compression would be 17dBm at the matched load. Higher useable bandwidths are possible at lower output powers, as shown in the Large Signal Bandwidth curves. As those graphs show, $7V_{PP}$ outputs are possible with almost perfect frequency response flatness through 100MHz for both non-inverting or inverting operation.

TWO-TONE 3rd-ORDER OUTPUT INTERMODULATION INTERCEPT (OP_3)

In narrowband IF strips, each amplifier typically feeds into a bandpass filter that attenuates most harmonic distortion terms. The most troublesome remaining distortion is the 3rd-order, two-tone intermodulations that can fall very close (in frequency) to the desired signals and cannot be filtered out. If two test frequencies are defined at $F_O + \Delta F$ and $F_O - \Delta F$, the 3rd-order intermodulation distortion products will fall at $F_O + 3\Delta F$ and $F_O - 3\Delta F$. If the two test power levels (P_T) are equal, the OPA695 will produce 3rd-order spurious terms (P_S) that are at these frequencies and at a power level below the test power levels given by:

$$P_T - P_S = 2\left(OP_3 - P_T\right) \quad (5)$$

The 3rd-order intercept plot shown in the Typical Characteristic curves shows a very high intercept at low frequencies that decreases with increasing frequency. This intercept is defined at the matched load to allow direct comparison with fixed-gain RF amplifiers. To produce a $2V_{PP}$ total two-tone envelope at the matched load, each power level must be 4dBm at the matched load ($1V_{PP}$). Using Equation 5, and the performance curve for inverting operation, at 50MHz (41.5dBm intercept) the 3rd-order spurious will be 2 • (41.5 – 4) = 75dB below these 4dBm test tones. This is an exceptionally low distortion for an amplifier that only uses 13mA supply current. Considerable improvement from this level of performance is also possible if the output drives directly into the lighter load of an ADC input (see *High SFDR Differential ADC driver* section).

This very high intercept versus quiescent power is achieved by the high loop gain of the OPA695. This loop gain does, however, decrease with frequency, giving the decreasing OP3 performance shown in the Typical Characteristics. Application as an IF amplifier through 200MHz is possible with output intercepts exceeding 21dBm at 200MHz. Intercept performance will vary slightly with gain setting decreasing at higher gains (that is, gains greater than the 8V/V, or 12dB, gain used in the Typical Characteristic curves) and increasing at lower gains.

NOISE FIGURE

All fixed-gain RF amplifiers show a very good noise figure (typically < 5dB). For broadband amplifiers, this is achieved by a low-noise input transistor and an input match set by feedback. This feedback greatly reduces the noise figure for fixed-gain RF amplifiers, but also makes the input match dependent on the load and the output match dependent on the source impedance at the input.

The noise figure for an op amp is always higher than for fixed-gain RF amplifiers due to the more complex internal circuits of an op amp (giving higher input noise voltage and current terms). Also, for simple circuits, the input match is set resistively. What is gained is an almost perfect I/O impedance match, much better load isolation, and very high 3rd-order intercepts versus quiescent power. These higher noise figures can be acceptable if the OPA695 has enough gain preceding it in the IF chain.

Op amp noise figure equations include at least six terms (see the Noise Performance section), due to the external resistors. As a point of reference, the circuit of Figure 1 has an input noise figure of 14dB while the inverting configuration of Figure 2 has an input noise figure of 11dB. At higher gains, it is typical for the inverting noise figure to be slightly better than for an equivalent gain, noninverting configuration. One easy way to improve the noise figure for the noninverting configuration of the OPA695 is to include a step-up, 1:2 turns ratio transformer at the input. This configuration is shown in Figure 5.

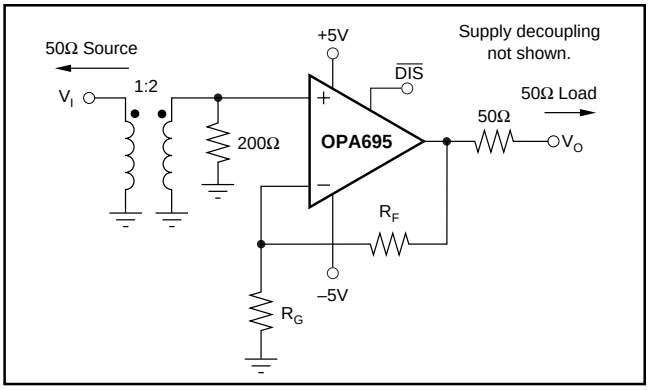


FIGURE 5. IF Amplifier with Improved Noise Figure.

The transformer provides a noiseless voltage gain at the expense of higher source impedance for the OPA695 noninverting input current noise. The input impedance is still set to 50Ω by the 200Ω resistor on the transformer secondary. A 1:2 turns ratio transformer will reflect the 200Ω to the input side as a 50Ω impedance over the bandwidth of the transformer. Using a 1:2 step-up transformer will also reduce the required amplifier gain by 1/2 for any particular desired overall gain.

Tables I - III summarize the recommended resistor values and resulting noise figures over the desired gain setting for three circuit options for the OPA695 operated as a precision IF amplifier. In each case, R_F and R_G are adjusted for both best bandwidth and to achieve the required gain.

In all cases, exact computed values for resistors are shown—in application, pick standard resistor values that are closest to those in the tables.

GAIN TO LOAD (dB)	R_F (Ω)	R_G (Ω)	NOISE FIGURE
6	478	159	17.20
7	468	134	16.55
8	458	113	15.95
9	446	96	15.40
10	433	81	14.91
11	419	68	14.47
12	402	57	14.09
13	384	48	13.76
14	363	40	13.23
15	340	33	13.23
16	314	27	13.03
17	284	21	12.86
18	252	16	12.72
19	215	12	12.60
20	174	9	12.51

TABLE I. Noninverting Wideband Op Amp (Figure 1).

GAIN TO LOAD (dB)	R_F (Ω)	R_G (Ω)	NOISE FIGURE
6	516	518	16.34
7	511	412	15.54
8	506	334	14.78
9	500	275	14.07
10	493	228	13.40
11	486	190	12.78
12	478	160	12.21
13	469	135	11.70
14	458	114	11.25
15	447	96	10.85
16	434	81	10.15
17	419	69	10.21
18	403	58	9.96
19	384	48	9.74
20	364	40	9.57

TABLE II. Noninverting with a 1:2 Input Step-Up Transformer (Figure 5).

GAIN TO LOAD (dB)	OPTIMUM R_F (Ω)	R_G (Ω)	INPUT MATCH R_T	NOISE FIGURE
6	463.27	116	87	16.94
7	454.61	101	98	16.06
8	444.91	88	114	15.16
9	434.07	77	142	14.23
10	421.95	66	199	13.24
11	408.42	57	380	12.16
12	398.11	50	Infinite	11.03
13	446.68	50	Infinite	10.92
14	501.19	50	Infinite	10.83
15	562.34	50	Infinite	10.75
16	630.96	50	Infinite	10.67
17	707.95	50	Infinite	10.61
18	794.33	50	Infinite	10.55
19	891.25	50	Infinite	10.49
20	1000.00	50	Infinite	10.45

TABLE III. Inverting Wideband RF Amplifier (Figure 2).

SAW FILTER BUFFER

One common requirement in an IF strip is to buffer the output of a mixer with enough gain to recover the insertion loss of a narrowband SAW filter. Figure 6 shows one possible configuration driving a SAW filter. Figure 7 shows the intercept at the 50Ω load. Operating in the inverting mode at a voltage gain of –8V/V, this circuit provides a 50Ω input match using the gain set resistor, has the feedback optimized for maximum bandwidth (700MHz in this case), and drives through a 50Ω output resistor into the matching network at the input of the SAW filter. If the SAW filter gives a 12dB insertion loss, a net gain of 0dB to the 50Ω load at the output of the SAW (which could be the input impedance of the next IF amplifier or mixer) will be delivered in the passband of the SAW filter. Using the OPA695 in this application will isolate the first mixer from the impedance of the SAW filter and provide very low two-tone, 3rd-order spurious levels in the SAW filter bandwidth. Inverting operation will give the broadest bandwidth up to a gain of –12V/V (15.6dB). Noninverting operation will give higher bandwidth at gain settings higher than this, but will also give a slight reduction in intercept and Noise Figure performance.

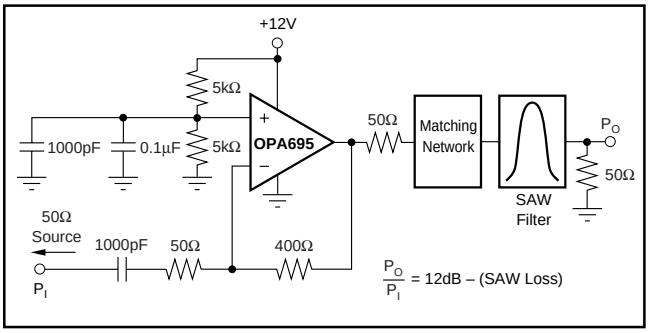


FIGURE 6. IF Amplifier Driving SAW Filter.

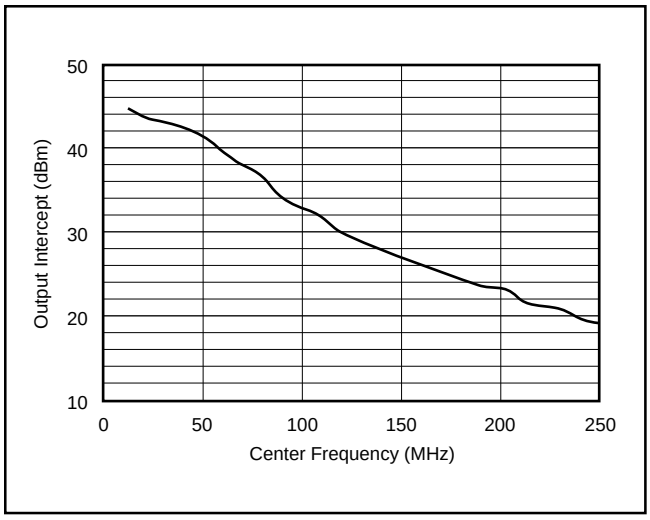


FIGURE 7. 2-Tone, 3rd-Order Intermodulation Intercept.

LO BUFFER AMPLIFIER

The OPA695 may also be used to buffer the Local Oscillator (LO) from the mixer(s). Operating at a voltage gain of +2, the OPA695 will provide almost perfect load isolation for the LO with a net gain of 0dB to the mixer. Applications through 1.4GHz LOs may be considered, but best operation would be for LOs < 1.0GHz at a gain of +2. Gain could also be easily provided by the OPA695 to drive higher power levels into the mixer. One unique option in using the OPA695 as an LO buffer is shown in Figure 8. Since the OPA695 can drive multiple output loads, two identical LO signals may be delivered to the mixers in a diversity receiver simply by tapping the output off through two series 50Ω output resistors. This circuit is set up for a voltage gain of +2V/V to the output pin for a gain of +1V/V (0dB) to the mixers, but could easily be adjusted to deliver higher gains as well.

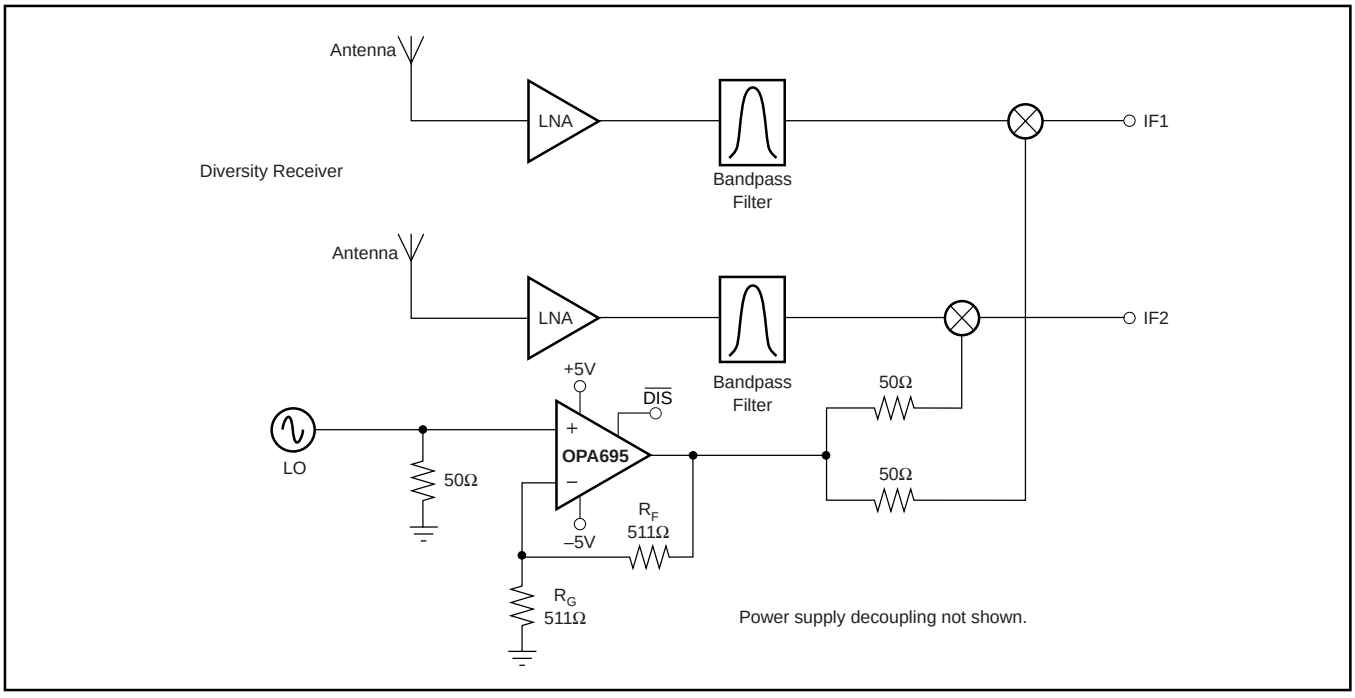


FIGURE 8. Dual Output LO Buffer.

WIDEBAND CABLE DRIVING APPLICATIONS

The high slew rate and bandwidth of the OPA695 can be used to meet the most demanding cable driving applications.

CABLE MODEM RETURN PATH DRIVER

The standard cable modem upstream driver is typically required to drive high power over a 5MHz to 65MHz bandwidth while delivering < –50dBc distortion. Highly-integrated solutions (including programmable gain stages) often fall short of this target due to high losses from the amplifier output to the line. The higher gain operating capability of the OPA695, along with its very high slew rate, provides a low-cost solution for delivering this signal with the required spurious-free dynamic range. Figure 9 shows one example of using the OPA695 as an upstream driver for a cable modem return path. In this case, the input impedance of the driver is set to 75Ω by the gain resistor (R_G). The required input level from the adjustable gain stage is significantly reduced by the 15.5dB gain provided by the OPA695. In this example, the physical 75Ω output matching resistor, along with the 3dB loss in the diplexer, will attenuate the output swing by 9dB on the line. In this example, a single +12V supply was used to achieve the lowest harmonic distortion for the $6V_{PP}$ output pin voltage through 65MHz. Measured performance for this example gave 600MHz small-signal bandwidth and < –54dBc distortion through 65MHz for a $6V_{PP}$ output pin voltage swing.

An alternative to this circuit, giving even lower distortion, is a differential driver using two OPA695s driving into an output transformer. This can be used either to double the available line power, or to improve distortion by cutting the required output swing in half for each stage. The channel disable required by the MCNS specification should be implemented by using the PGA disable feature. The MCNS disable specification requires that an output impedance match be maintained with the signal channel shut off. The disable feature of the OPA695 is intended principally for power savings and puts the output and inverting input pins into a high impedance mode. This will not maintain the required output impedance matching. Turning off the signal at the input of Figure 9, while keeping the OPA695 active, will maintain the impedance matching while putting very little noise on the line. The line noise in disable for the circuit of Figure 9 (with the PGA source turned off, but still presenting a 75Ω source impedance) will be a very low $4nV/\sqrt{Hz}$ (–157dBm/Hz) due to the low input noise of the OPA695.

RGB VIDEO LINE DRIVER

The extremely high bandwidth of the OPA695 operating at a gain of +2 will support the fastest RAMDAC outputs for applications such as auxiliary monitor driving. The front page of this data sheet shows measured performance for a $0 \rightarrow +1V$ input square wave at 125MHz. As a general rule, the required full-power bandwidth for the amplifier must be at least one-half the pixel rate. With its noninverting gain of +2, slew rate of 2900V/µs, and a $1.4V_{PP}$ output pin voltage swing for standard RGB video levels, the OPA695 will give a

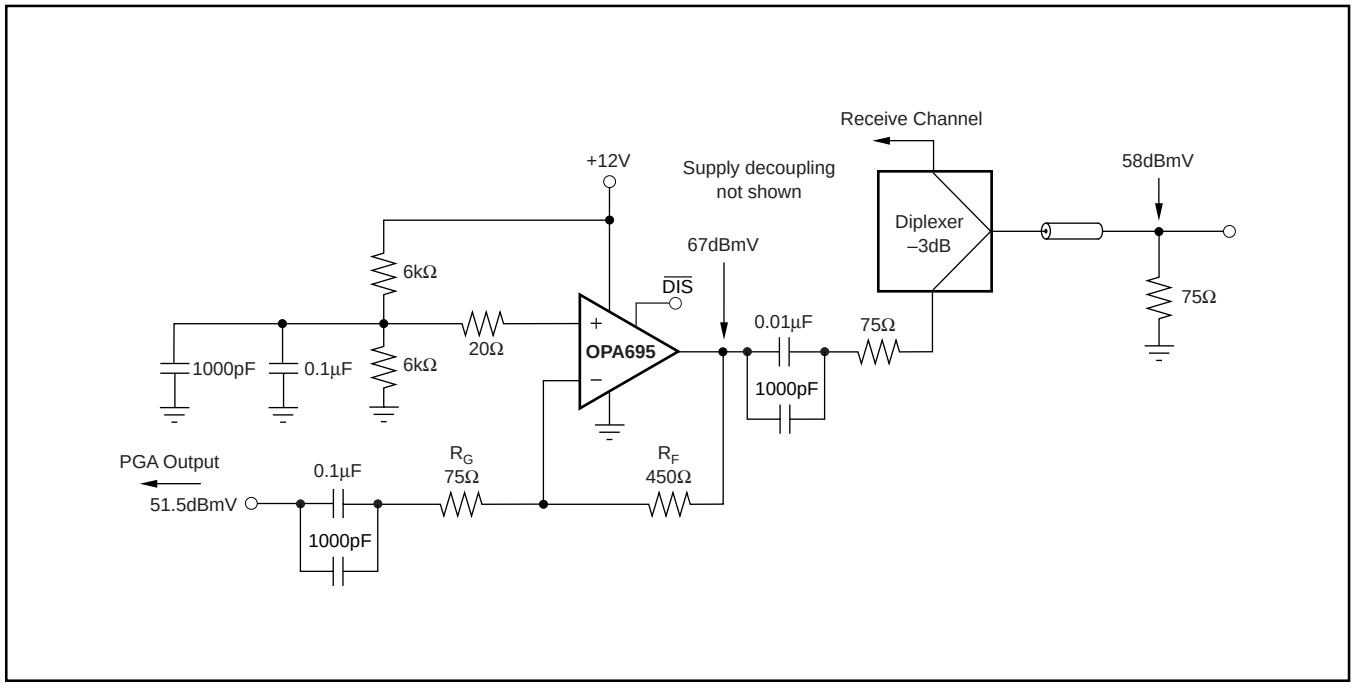


FIGURE 9. Cable Modem Upstream Driver.

bandwidth of 600MHz, which will then support up to 1.26GHz pixel rates. Figure 10 shows an example where three OPA695s provide an auxiliary monitor output for a high-resolution RGB RAMDAC.

An alternative circuit that will take advantage of the higher inverting slew rate of the OPA695 (4300V/µs) takes the complementary current output from the RAMDAC and converts it to positive video to give a very high, full-power bandwidth RGB line driver. This will give sharper pixel edges than the circuit of Figure 10. Most high-speed DACs are current-steering designs where there is both an output current signal that is used for the video, and a complementary output that is typically discarded into a matching resistor. The complementary current output can be used as an auxiliary output if it is inverted, as shown in Figure 11.

In the circuit of Figure 11, the complementary current output is terminated by an equivalent 75Ω impedance (the parallel combination of R_T and R_G) that also provides a current division to reduce the signal current through the feedback resistor, R_F. This allows R_F to be increased to a value which will hold a flat frequency response. Since the complementary current output is essentially an inverted video signal, this circuit sets up a white video level at the output of the OPA695 for zero DAC output current (using the 0.77V DC bias on the

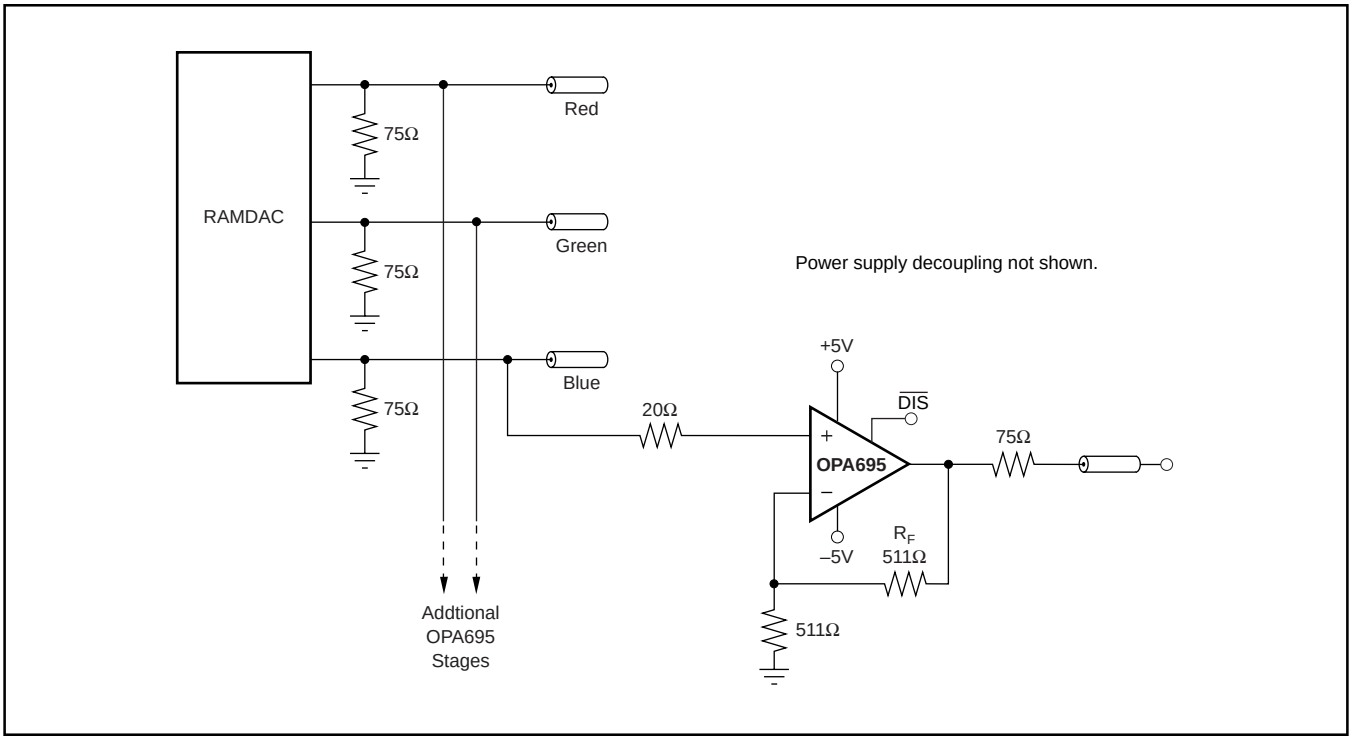


FIGURE 10. Gain of +2, High-Resolution RGB Monitor Output.

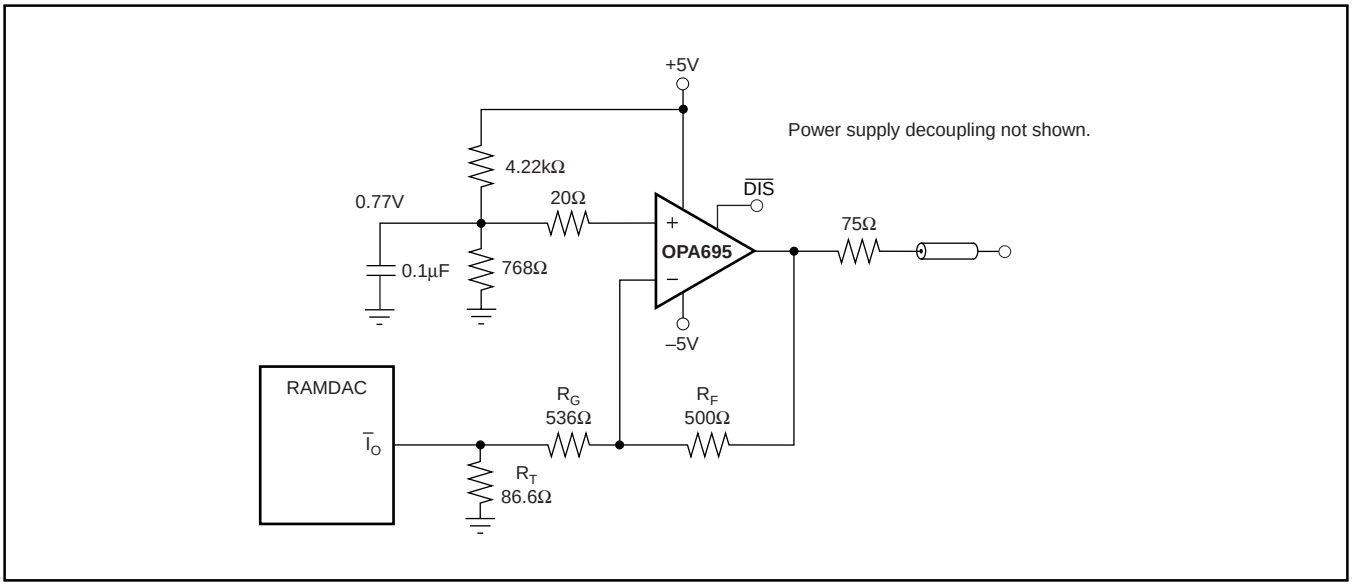


FIGURE 11. High-Resolution RGB Driver Using DAC Complementary Output Current.

noninverting input), then inverts the complementary output current to produce a signal that ranges from this 1.4V at zero output current down to 0V at maximum output current level (assuming a 20mA maximum output current). This will give a very wideband (> 800MHz) video signal capability.

ARBITRARY WAVEFORM DRIVER

The OPA695 may be used as the output stage for moderate output power Arbitrary Waveform Driver applications. Driving out through a series 50Ω matching resistor into a 50Ω matched load will allow up to a 4.0V_{PP} swing at the matched load (15dBm) when operating the OPA695 on a ±5V power supply. This level of power is available for gains of either ±8 with a flat response through 100MHz. When interfacing directly from a complementary current output DAC, consider the circuit of Figure 11, modified for the peak output currents of the particular DAC being considered. Where purely AC-coupled output signals are required from a complementary current output DAC, consider a push-pull output stage using the circuit of Figure 12. The resistor values here have been calculated for a 20mA peak output current DAC which produces up to a 5V_{PP} swing at the matched load (18dBm). This approach will give higher power at the load with much lower 2nd-harmonic distortion.

For a 20mA peak output current DAC, the mid-scale current of 10mA will give a 2V DC output common-mode operating voltage due to the 200Ω resistor to ground at the outputs. The total AC impedance at each output is 50Ω, giving a ±0.5V swing around this 2V common-mode voltage for the DAC. These resistors also act as a current divider, sending 75% of the DAC output current through the feedback resistor (464Ω). The blocking capacitor references the OPA695 output voltage to ground, and turns the unipolar DAC output current into a bipolar swing of 0.75 • 20mA • 464Ω = 7V_{PP} at each amplifier output. Each output is exactly 180° out-of-phase from the other, producing double 7V_{PP} into the matching resistors. To limit the peak output current and improve distortion, the circuit of Figure 12 is set up with a 1.4:1 step-down transformer. This reflects the 50Ω load to be 100Ω at the primary side of the transformer. For the maximum 14V_{PP} swing across the outputs of the two amplifiers, the matching resistors will drop this to 7V_{PP} at the input of the transformer, then down to 5V_{PP} maximum at the 50Ω load at the output of the transformer. This step-down approach reduces the peak output current to 14V_P/(200Ω) = 70mA.

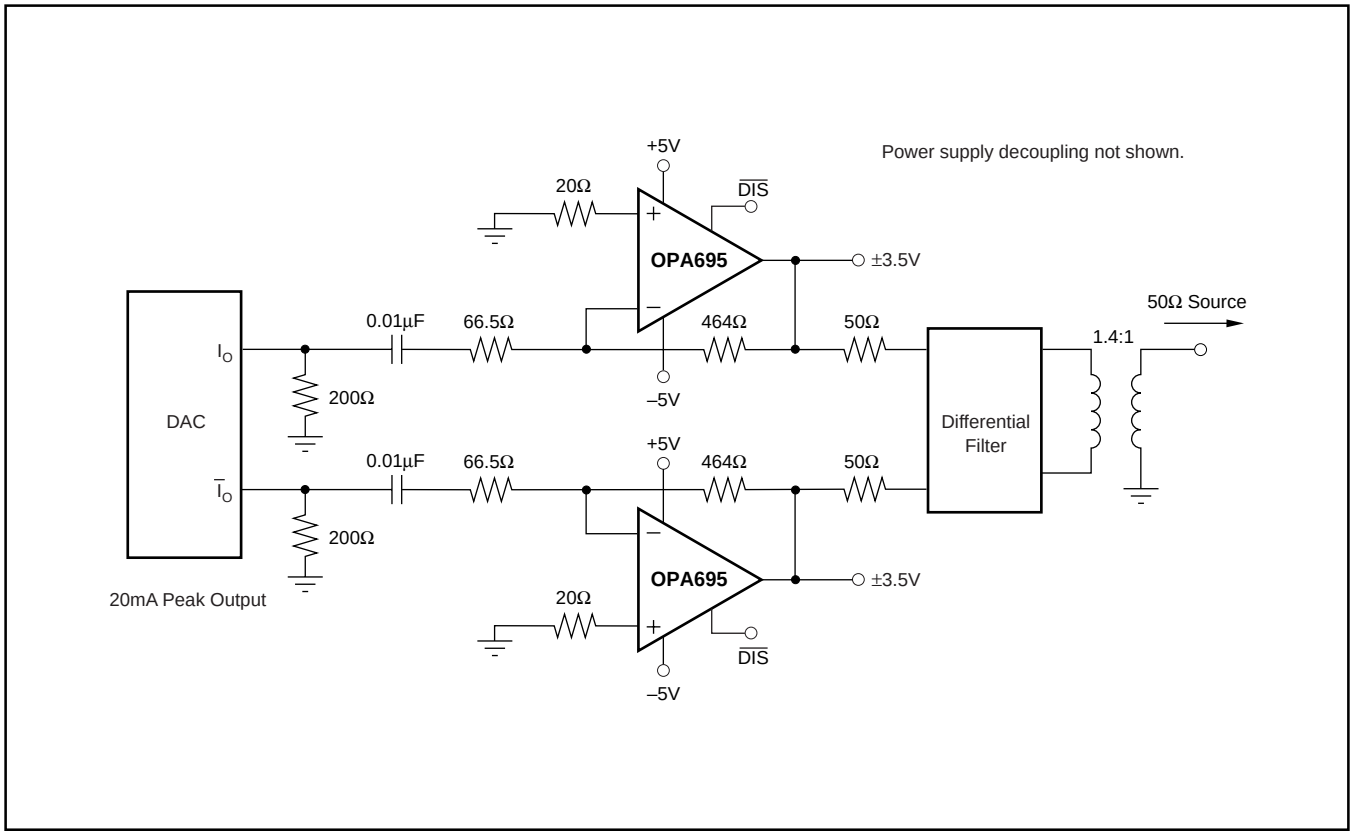


FIGURE 12. High Power, Wideband AC-Coupled Arbitrary Waveform Driver.

DIFFERENTIAL I/O APPLICATIONS

The OPA695 offers very low 3rd-order distortion terms with a dominant 2nd-order distortion for the single amplifier operation. For the lowest distortion, particularly where differential outputs are needed, operating two OPA695s in a differential I/O design will suppress these even-order terms, delivering extremely low harmonic distortion through high frequencies and powers. Differential outputs are often preferred for high performance ADCs, twisted-pair driving, and mixer interfaces. Two basic approaches to differential I/Os are the noninverting or inverting configurations. Since the output is differential, the signal polarity is somewhat meaningless—the noninverting and inverting terminology applies here to where the input is brought into the two OPA695s. Each approach has its advantages and disadvantages. Figure 13 shows a basic starting point for non-inverting differential I/O applications.

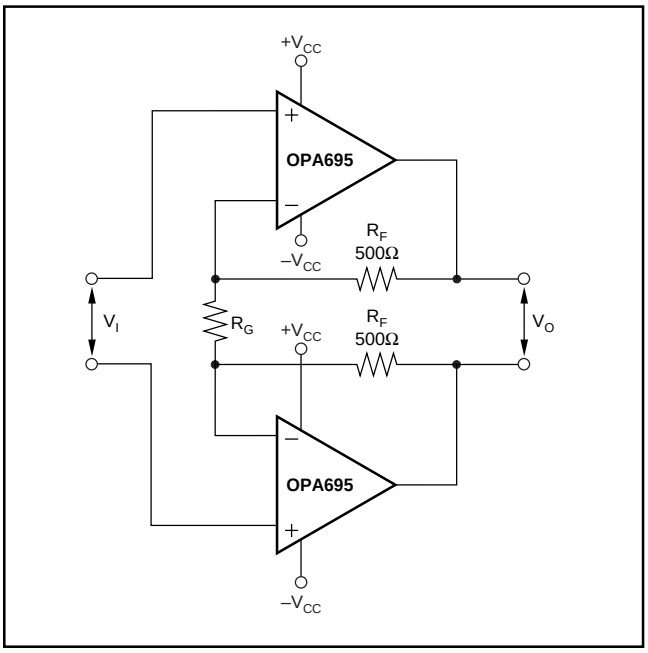


FIGURE 13. Noninverting Input Differential I/O Amplifier.

This approach allows for a source termination impedance that is independent of the signal gain. For instance, simple differential filters may be included in the signal path right up to the non-inverting inputs without interacting with the gain setting. The differential signal gain for the circuit of Figure 13 is:

$$A_D = 1 + 2 \bullet R_F/R_G \quad (6)$$

Since the OPA695 is a current feedback amplifier, its bandwidth is principally controlled with the feedback resistor value—Figure 13 shows a typical value of 500Ω. However, the differential gain may be adjusted with considerable freedom using just the R_G resistor. In fact, R_G may be a reactive network providing a very isolated shaping to the differential frequency response. It is common for AC-coupled applications to include a blocking capacitor in series with R_G. This reduces the gain to 1 at low frequency, rising to the A_D expression shown above at higher frequencies. The noninverting input approach of Figure 13 can be used for higher gains than the inverting input approach. It will, however, have a reduced full-power bandwidth due to the lower slew rate of the OPA695 running noninverting vs inverting input mode of operation.

Various combinations of single-supply or AC-coupled gain can also be delivered using the basic circuit of Figure 13. Common-mode bias voltages on the two noninverting inputs pass on to the output with a gain of 1, since an equal DC voltage at each inverting node creates no current through R_G. This circuit does show a common-mode gain of 1 from input to output. The source connection should either remove this common-mode signal if undesired (using an input transformer can provide this function), or the common-mode voltage at the inputs can be used to set the output common-mode bias. If the low common-mode rejection of this circuit is a problem, the output interface may also be used to reject that common-mode. For instance, most modern differential input ADCs reject common-mode signals very well, while a line driver application through a transformer will also remove the common-mode signal at the secondary of the transformer.

Figure 14 shows a differential I/O stage configured as an inverting amplifier. In this case, the gain resistors (R_G) become part of the input resistance for the source. This provides a better noise performance than the non-inverting configuration, but does limit the flexibility in setting the input impedance separately from the gain.

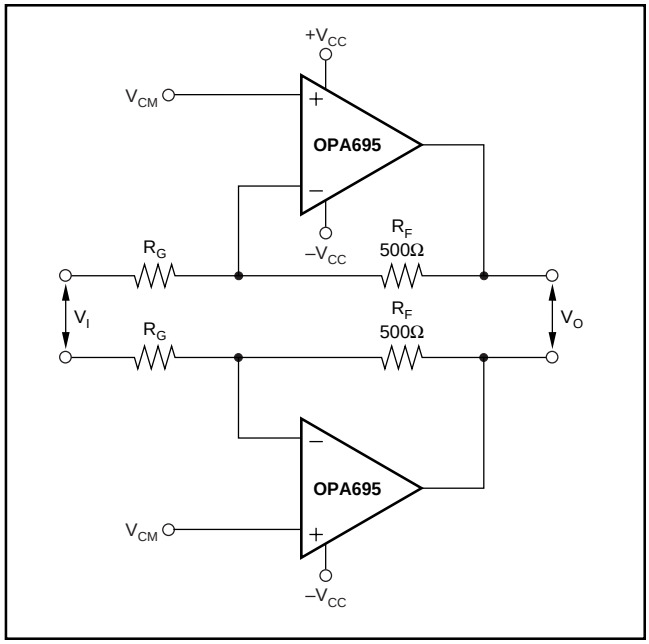


FIGURE 14. Inverting Input Differential I/O Amplifier.

The two noninverting inputs provide an easy common-mode control input. This is particularly easy if the source is AC-coupled through either blocking caps or a transformer. In either case, the common-mode input voltages on the two

noninverting inputs again have a gain of 1 to the output pins, giving particularly easy common-mode control for single-supply operation. The OPA695 used in this configuration does constrain the feedback to the 500Ω region for best frequency response. With R_F fixed, the input resistors may be adjusted to the desired gain, but will also be changing the input impedance as well. The high-frequency common-mode gain for this circuit from input to output will be the same as for the signal gain. Again, if the source might include an undesired common-mode signal, that could be rejected at the input using blocking caps (for low-frequency and DC common-mode) or a transformer coupling. The differential performance plots shown in the Typical Characteristics used the configuration of Figure 14 and an input 1:1 transformer. The differential signal gain in the circuit of Figure 14 is:

$$A_D = R_F/R_G \quad (7)$$

Using this configuration suppresses the 2nd-harmonics, leaving only 3rd-harmonic terms as the limit to output SFDR. The much higher slew rate of the inverting configuration also extends the full-power bandwidth and the range of very low intermodulation distortion over the performance bandwidth available from the circuit of Figure 13. The Typical Characteristics show that the circuit of Figure 14 operating at an A_D = 10 can deliver a $16V_{PP}$ signal with over 500MHz –3dB bandwidth. Using Equation 4, this implies a differential output slew of 18000V/µsec, or 9000V/µsec at each output. This output slew rate is far higher than specified, and probably due to the lighter load used in the differential tests.

This inverting input differential configuration is particularly suited to very high SFDR converter interfaces—specifically narrowband IF channels. The Typical Characteristics show the 2-tone, 3rd-order intermodulation intercept exceeding 45dBm through 90MHz. Although this data was taken with an 800Ω load, the intercept model appears to work for this circuit, simply treating the power level as if it were into 50Ω. For example, at 70MHz, the differential Typical Characteristic plots show a 48dBm intercept. To predict the 2-tone intermodulation SFDR, assuming a –1dB below full-scale envelope to a $2V_{PP}$ maximum differential input converter, the test power level would be 9dBm – 6dBm = 3dBm for each tone. Putting this into the intercept equation, gives:

$$\Delta dBc = 2 \bullet (48 - 3) = 90dBc \quad (8)$$

The single-tone distortion data shows approximately 72dB SFDR at 70MHz for a $2V_{PP}$ output into this light 800Ω load. A modest post filter after the amplifier can reduce these harmonics (2nd at 140MHz, 3rd at 210MHz) to the point where the full SFDR to a converter can be in the 85dB range for a 70MHz IF operation.

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA695 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in the table below.

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA695ID	SO-8	DEM-OPA-SO-1B	SBOU026
OPA691IDBV	SOT23-6	DEM-OPA-SOT-1B	SBOU027

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA695 product folder.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO OPTIMIZE BANDWIDTH

A current-feedback op amp such as the OPA695 can hold an almost constant bandwidth over signal gain settings with the proper adjustment of the external resistor values. This is shown in the Typical Characteristic curves. The small-signal bandwidth decreases only slightly with increasing gain. These curves also show that the feedback resistor has been changed for each gain setting. The resistor ***values*** on the inverting side of the circuit for a current-feedback op amp can be treated as frequency response compensation elements while their ***ratios*** set the signal gain. Figure 15 shows the analysis circuit for the OPA695 small-signal frequency response.

The key elements of this current feedback op amp model are:

$\alpha \Rightarrow$ Buffer gain from the noninverting input to the inverting input

$R_I \Rightarrow$ Buffer output impedance

$i_{ERR} \Rightarrow$ Feedback error current signal

$Z(s) \Rightarrow$ Frequency-dependent, open-loop transimpedance gain from i_{ERR} to V_O

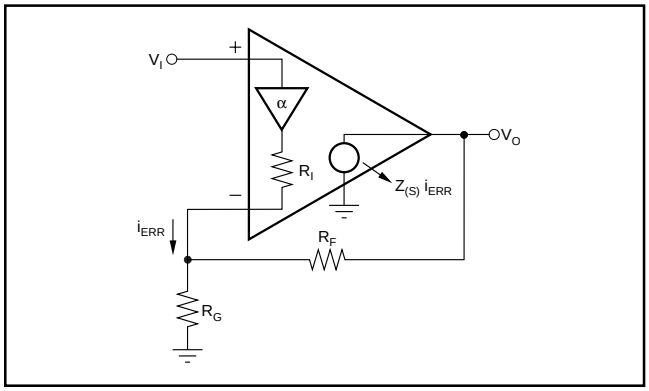


FIGURE 15. Current-Feedback Transfer Function Analysis Circuit.

The buffer gain is typically very close to 1.00 and is normally neglected from signal gain considerations. It will, however, set the CMRR for a single op amp differential amplifier configuration. For the buffer gain $\alpha < 1.0$, the CMRR = $-20 \cdot \log(1 - \alpha)$.

R_I, the buffer output impedance, is a critical portion of the bandwidth control equation. For the OPA695, it is typically about 28Ω for ±5V operation and 31Ω for single +5V operation.

A current-feedback op amp senses an error current in the inverting node (as opposed to a differential input error voltage for a voltage-feedback op amp) and passes this on to the output through an internal frequency-dependent transimpedance gain. The Typical Characteristic curves show this open-loop transimpedance response. This is analogous to the open-loop voltage gain curve for a voltage-feedback op amp. Developing the transfer function for the circuit of Figure 18 gives Equation 9:

$$\frac{V_O}{V_I} = \frac{\alpha\left(1+\frac{R_F}{R_G}\right)}{1+\frac{R_F + R_I\left(1+\frac{R_F}{R_G}\right)}{Z_{(S)}}} = \frac{\alpha \bullet NG}{1+\frac{R_F + R_I \bullet NG}{Z_{(S)}}} \quad (9)$$

Where

$$NC = 1+\frac{R_F}{R_G} = \text{Noise Gain}$$

This is written in a loop gain analysis format, where the errors arising from a non-infinite open-loop gain are shown in the denominator. If Z(s) were infinite over all frequencies, the denominator of Equation 9 would reduce to 1, and the ideal desired signal gain shown in the numerator would be achieved. The fraction in the denominator of Equation 9 determines the frequency response. Equation 10 shows this as the loop gain equation:

$$\frac{Z_{(S)}}{R_F + R_I \bullet NG} = \text{Loop Gain} \quad (10)$$

If $20 \cdot \log (R_F + NG \cdot R_I)$ were superimposed on the open-loop transimpedance plot, the difference between the two would be the loop gain at a given frequency. Eventually, Z(s) rolls off to equal the denominator of Equation 10, at which point the loop gain has reduced to 1 (and the curves have intersected). This point of equality is where the amplifier closed-loop frequency response given by Equation 9 will start to roll off, and is exactly analogous to the frequency at which the noise gain equals the open-loop voltage gain for a voltage-feedback op amp. The difference here is that the total impedance in the denominator of Equation 10 may be controlled separately from the desired signal gain (or NG).

The OPA695 is internally compensated to give a maximally flat frequency response for R_F = 402Ω at NG = 8 on ±5V supplies. Evaluating the denominator of Equation 7 (which is the feedback transimpedance) gives an optimal target of 663Ω. As the signal gain changes, the contribution of the $NG \cdot R_I$ term in the feedback transimpedance will change, but the total can be held constant by adjusting R_F. Equation 11 gives an approximate equation for optimum R_F over signal gain:

$$R_F = 663\Omega - NG \bullet R_I \quad (11)$$

As the desired signal gain increases, this equation will eventually predict a negative R_F. A somewhat subjective limit to this adjustment can also be set by holding R_G to a minimum value of 10Ω. Lower values will load both the buffer stage at the input and the output stage if R_F gets too low, actually decreasing the bandwidth. Figure 16 shows the recommended R_F versus NG for both ±5V and a single +5V operation. The optimum target feedback impedance for +5V operation used in Equation 8 is 663Ω, while the typical buffer output impedance is 32Ω. The values for R_F versus gain shown here are approximately equal to the values used to generate the Typical Characteristic curves. In some cases, the values used differ slightly from that shown here, in that the values used in the Typical Characteristics are also correcting for board parasitics not considered in the simplified analysis leading to Equation 11. The values shown in Figure 16 give a good starting point for designs where bandwidth optimization is desired and a flat frequency response is needed.

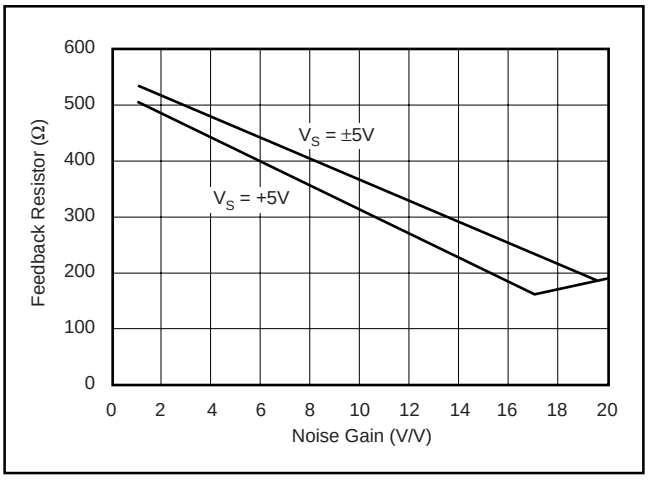


FIGURE 16. Recommended Feedback Resistor vs Noise Gain.

The total impedance presented to the inverting input may be used to adjust the closed-loop signal bandwidth. Inserting a series resistor between the inverting input and the summing junction will increase the feedback impedance (denominator of Equation 10), decreasing the bandwidth. The internal buffer output impedance for the OPA695 is slightly influenced by the source impedance looking out of the non-inverting input terminal. High source resistors will have the effect of increasing R_I, decreasing the bandwidth. For those single-supply applications which develop a midpoint bias at the non-inverting input through high-valued resistors, the decoupling capacitor is essential for power-supply ripple rejection, non-inverting input noise current shunting, and minimizing the high-frequency value for R_I in Figure 15.

Inverting feedback optimization is somewhat complicated by the impedance matching requirement at the input, as shown in Figure 2. The resistor values shown in Table III should be used in this case.

OUTPUT CURRENT AND VOLTAGE

The OPA695 provides output voltage and current capabilities that are consistent with driving doubly-terminated 50Ω lines. For a 100Ω load at a gain of +8 (see Figure 1), the total load is the parallel combination of the 100Ω load and the 456Ω total feedback network impedance. This 82Ω load will require no more than 45mA output current to support the ±3.7V minimum output voltage swing specified for 100Ω loads. This is well below the minimum ±90mA specifications.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage • current, or V-I, product which is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* plot in the Typical Characteristic curves. The X and Y axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants provide a more detailed view of the OPA695 output drive capabilities. Superimposing resistor load lines onto the plot shows the available output voltage and current for specific loads.

The minimum specified output voltage and current over-temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the specification tables. As the output transistors deliver power, the junction temperatures will increase, decreasing the V_{BE}s (increasing the available output voltage swing) and increasing the current gains (increasing the available output current). In steady-state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications, since the output stage junction temperatures will be higher than the minimum specified operating ambient.

To maintain maximum output stage linearity, no output short-circuit protection is provided. This will not normally be a problem, since most applications include a series-matching resistor at the output that will limit the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power supply pin will, in most cases, destroy the amplifier. If additional short-circuit protection is required, consider a small series resistor in the power-supply leads. Under heavy output loads, this will reduce the available output voltage swing. A 5Ω series resistor in each power-supply lead will limit the internal power dissipation to less than 1W for an output short circuit while decreasing the available output voltage swing only 0.25V for up to 50mA desired load currents. Always place the 0.1μF power supply decoupling capacitors directly on the supply pins after these supply current-limiting resistors.

DRIVING CAPACITIVE LOADS

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an A/D converter—including additional external capacitance which may be recommended to improve A/D linearity. A high-speed, high open-loop gain amplifier like the OPA695 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended R_S versus capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA695. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully and add the recommended series resistor as close as possible to the OPA695 output pin (see *Board Layout Guidelines*).

DISTORTION PERFORMANCE

The OPA695 provides good distortion performance into a 100Ω load on ±5V supplies. Relative to alternative solutions, the OPA695 holds much lower distortion at higher frequencies (> 20MHz). Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic will dominate the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember, the total load includes the feedback network. In the non-inverting configuration (Figure 1), this is the sum of $R_F + R_G$, while in the inverting configuration, it is just R_F. Also, providing an additional supply decoupling capacitor (0.01μF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. The Typical Performance Curves show the 2nd-harmonic increasing at a little less than the expected 2x rate, while the 3rd-harmonic increases at a little less than the expected 3x rate. Where the test power doubles, the difference between it and the 2nd harmonic decreases less than the expected 6dB, while the difference between it and the 3rd decreases by less than the expected 12dB.

The OPA695 has extremely low 3rd-order harmonic distortion. This also gives a high 2-tone, 3rd-order intermodulation intercept, as shown in the Typical Characteristic curves. This intercept curve is defined at the 50Ω load when driven through a 50Ω matching resistor to allow direct comparisons to RF MMIC devices and is shown for both gains of ±8. There is a slight improvement in intercept by operating the OPA695 in the inverting mode. The output matching resistor attenuates the voltage swing from the output pin to the load by 6dB. If the OPA695 drives directly into the input of a high impedance device, such as an ADC, this 6dB attenuation is not taken. Under these conditions, the intercept will increase by a minimum 6dBm.

The intercept is used to predict the intermodulation products for two closely-spaced frequencies. If the two test frequencies, F_1 and F_2, are specified in terms of average and delta frequency, $F_O = (F_1 + F_2)/2$ and $\Delta F = |F_2 - F_1|/2$, the two 3rd-order, close-in spurious tones will appear at $F_O \pm 3 \bullet \Delta F$. The difference between two equal test-tone power levels and these intermodulation spurious power levels is given by $\Delta dBc = 2 \bullet (OP_3 - P_O)$, where OP_3 is the intercept taken from the Typical Characteristic curve and P_O is the power level in dBm at the 50Ω load for one of the two closely-spaced test frequencies. For example, at 50MHz, gain of –8, the OPA695 has an intercept of 42dBm at a matched 50Ω load. If the full envelope of the two frequencies needs to be $2V_{PP}$, this requires each tone to be 4dBm. The 3rd-order intermodulation spurious tones will then be 2 • (42 – 4) = 76dBc below the test-tone power level (–72dBm). If this same $2V_{PP}$ 2-tone envelope were delivered directly into the input of an ADC without the matching loss or the loading of the 50Ω network, the intercept would increase to at least 48dBm. With the same signal and gain conditions, but now driving directly into a light load, the 3rd-order spurious tones will then be at least 2 • (48 – 4) = 88dBc below the 4dBm test-tone power levels centered on 50MHz. Tests have shown that, in reality, the 3rd-order spurious levels are much lower due to the lighter loading presented by most ADCs.

NOISE PERFORMANCE

The OPA695 offers an excellent balance between voltage and current noise terms to achieve low output noise. The inverting current noise (22pA/$\sqrt{Hz}$) is lower than most other current-feedback op amps while the input voltage noise (1.8nV/$\sqrt{Hz}$) is lower than any unity-gain stable, wideband, voltage-feedback op amp. This low-input voltage noise was achieved at the price of a higher noninverting input current noise (18pA/$\sqrt{Hz}$). As long as the AC source impedance looking out of the noninverting node is less than 50Ω, this current noise will not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 17 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

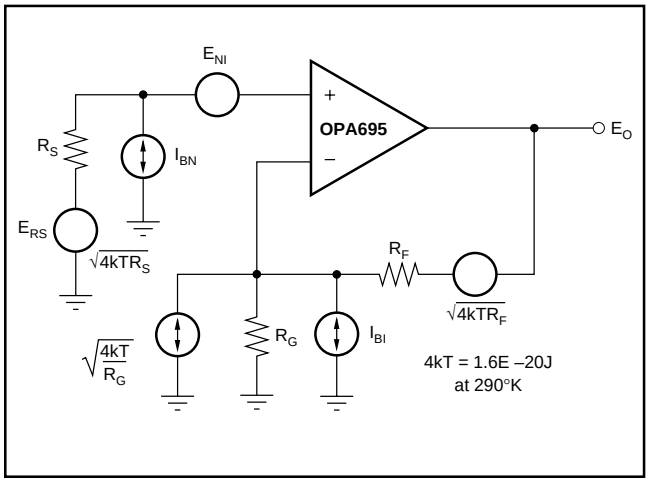


FIGURE 17. Op Amp Noise Figure Analysis Model.

The total output spot-noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 12 shows the general form for the output noise voltage using the terms shown in Figure 13.

(12)

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)G_N^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FG_N}$$

Dividing this expression by the noise gain (NG = $(1+R_F/R_G)$) will give the equivalent input referred spot-noise voltage at the noninverting input as shown in Equation 13:

(13)

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}}$$

Evaluating these two equations for the OPA695 circuit and component values shown in Figure 1 will give a total output spot-noise voltage of 18.7nV/$\sqrt{Hz}$ and a total equivalent input spot-noise voltage of 2.3nV/$\sqrt{Hz}$. This total input referred spot-noise voltage is higher than the 1.8nV/$\sqrt{Hz}$ specification for the op amp voltage noise alone. This reflects the noise added to the output by the inverting current noise times the feedback resistor. If the feedback resistor is reduced in high-gain configurations (as suggested previously), the total input referred voltage noise given by Equation 13 will just approach the 1.8nV/$\sqrt{Hz}$ of the op amp itself. For example, going to a gain of +20 (using R_F = 200Ω) will give a total input referred noise of 2.0nV/$\sqrt{Hz}$.

For a more complete discussion of op amp noise calculation, see TI Application Note, SBOA066, *Noise Analysis for High Speed Op Amps*, available through the TI web site.

DC ACCURACY AND OFFSET CONTROL

A current-feedback op amp like the OPA695 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate DC accuracy. The typical specifications show an input offset voltage comparable to high-speed voltage-feedback amplifiers; however, the two input bias currents are

somewhat higher and are unmatched. Although bias current cancellation techniques are very effective with most voltage-feedback op amps, they do not generally reduce the output DC offset for wideband current-feedback op amps. Since the two input bias currents are unrelated in both magnitude and polarity, matching the source impedance looking out of each input to reduce their error contribution to the output is ineffective. Evaluating the configuration of Figure 1, using a worst-case +25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

$$\pm(NG \bullet V_{OS}) + (I_{BN} \bullet R_S/2 \bullet NG) \pm(I_{BI} \bullet R_F)$$

where NG = non-inverting signal gain

$$= \pm(8 \bullet 3.0mV) \pm (30\mu A \bullet 25\Omega \bullet 8) \pm(402\Omega \bullet 60\mu A)$$

$$= \pm 24mV \pm 1.6mV \pm 24mV$$

$$= \pm 54mV$$

A fine-scale output offset null, or DC operating point adjustment, is often required. Numerous techniques are available for introducing DC offset control into an op amp circuit. Most simple adjustment techniques do not correct for temperature drift.

POWER SHUTDOWN OPERATION

The OPA695 provides an optional power shutdown feature that can be used to reduce system power. If the $V_{\overline{DIS}}$ control pin is left unconnected, the OPA695 operates normally. This shutdown is intended only as a power-saving feature. Forward path isolation is very good for small signals. Large signal isolation is not ensured. Using this feature to multiplex two or more outputs together is not recommended. Large signals applied to the shutdown output stages can turn on parasitic devices, degrading signal linearity for the desired channel.

Turn-on time is very quick from the shutdown condition, typically < 60ns. Turn-off time is strongly dependent on the external circuit configuration, but is typically 200ns for the circuit of Figure 1.

To shut down, the control pin must be asserted low. This logic control is referenced to the positive supply, as shown in the simplified circuit of Figure 18.

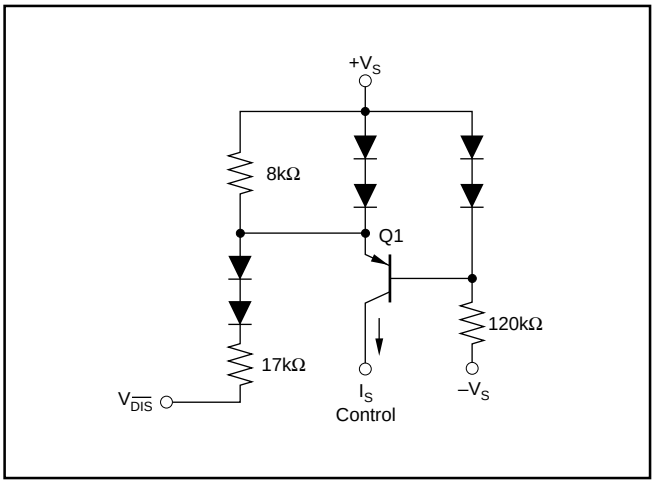


FIGURE 18. Op Amp Noise Figure Analysis Model.

In normal operation, base current to Q1 is provided through the 120kΩ resistor, while the emitter current through the 8kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in Q1's emitter. As $V_{\overline{DIS}}$ is pulled low, additional current is pulled through the 8kΩ resistor, eventually turning on these two diodes (≈ 180μA). At this point, any further current pulled out of $V_{\overline{DIS}}$ goes through those diodes holding the emitter-base voltage of Q1 at approximately 0V. This shuts off the collector current out of Q1, turning the amplifier off. The supply current in the shutdown mode is only that required to operate the circuit of Figure 18.

When disabled, the output and input nodes go to a high impedance state. If the OPA695 is operating in a gain of +1, this will show a very high impedance (3pF || 1MΩ) at the output and exceptional signal isolation. If operating at a gain greater than +1, the total feedback network resistance (R_F + R_G) will appear as the impedance looking back into the output, but the circuit will still show very high forward and reverse isolation. If configured as an inverting amplifier, the input and output will be connected through the feedback network resistance (R_F + R_G), giving relatively poor input to output isolation.

THERMAL ANALYSIS

The OPA695 does not require external heatsinking for most applications. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load. However, for a grounded resistive load, P_{DL} would be at a maximum when the output is fixed at a voltage equal to one-half of either supply voltage (for equal bipolar supplies). Under this condition, $P_{DL} = V_S^2/(4 \bullet R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As an absolute worst-case example, compute the maximum T_J using an OPA695IDBV (SOT23-6 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C and driving a grounded 100Ω load.

$$P_D = 10V \bullet 14.1mA + 5^2/(4 \bullet (100\Omega \parallel 458\Omega)) = 217mW$$

$$\text{Maximum } T_J = +85°C + (0.22W \bullet 150°C/W) = 118°C$$

This maximum operating junction temperature is well below most system level targets. Most applications will be lower since an absolute worst-case output stage power was assumed in this calculation.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA695 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the non-inverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power supply pins to high frequency 0.1μF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. An optional supply-decoupling capacitor across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at a lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high frequency performance of the OPA695. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wirewound-type resistors in a high frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. The frequency response is primarily determined by the feedback resistor value, as described previously. Increasing its value will reduce the bandwidth, while decreasing it will give a more peaked frequency response. The 402Ω feedback resistor (used in the typical performance specifications at a gain of +8 on ±5V supplies) is a good starting point for design. Note that a 523Ω feedback resistor, rather than a direct short, is required for the unity gain follower application. A current-feedback op amp requires a feedback resistor—even in the unity gain follower configuration—to control stability.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of *Recommended R_S vs Capacitive Load*. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA695 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is usually not necessary on board. In fact, a higher impedance environment will improve distortion, as shown in the distortion versus load plots. With a characteristic board trace impedance defined (based on board material and trace dimensions), a matching series resistor into the trace from the output of the OPA695 is used. A terminating shunt resistor at the input of the destination device is used as well. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA695 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of *R_S vs Capacitive Load*. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA695 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA695 directly onto the board.

INPUT AND ESD PROTECTION

The OPA695 is built using a very high-speed, complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table where an absolute maximum ±6.5V supply is reported. All device pins have limited ESD protection using internal diodes to the power supplies, as shown in Figure 19.

These diodes also provide moderate protection to input overdrive voltages above the supplies. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA695), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

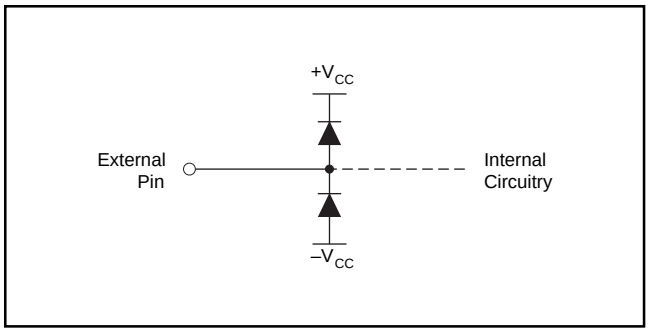


FIGURE 19. Internal ESD Protection.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
4/09	G	1	Front Page	Updated front page appearance.
		1, 4, 5	Various	Added DGK (MSOP-8) package to Package Ordering Information table and to Thermal Resistance specification in the Electrical Characteristics tables.
7/06	F	2	Absolute Maximum Ratings	Changed Storage Temperature Range from –40°C to +125C to –65°C to +125C.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA695ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 695	Samples
OPA695IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	A71L	Samples
OPA695IDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	A71L	Samples
OPA695IDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	A71L	Samples
OPA695IDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	A71L	Samples
OPA695IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 695	Samples
OPA695IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	695	Samples
OPA695IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	695	Samples
OPA695IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 695	Samples
OPA695IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 695	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

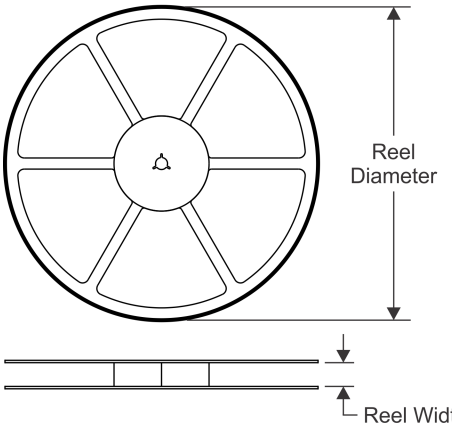
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

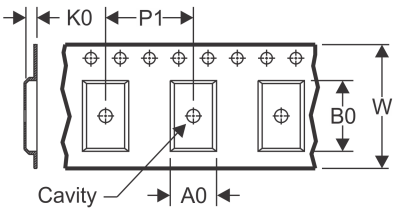
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

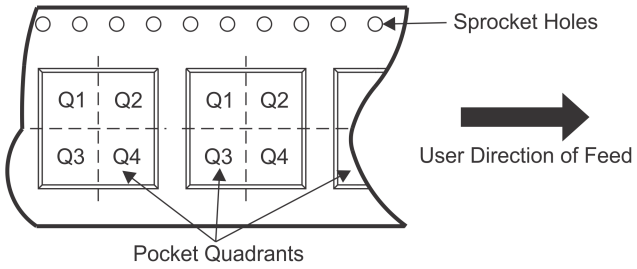


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

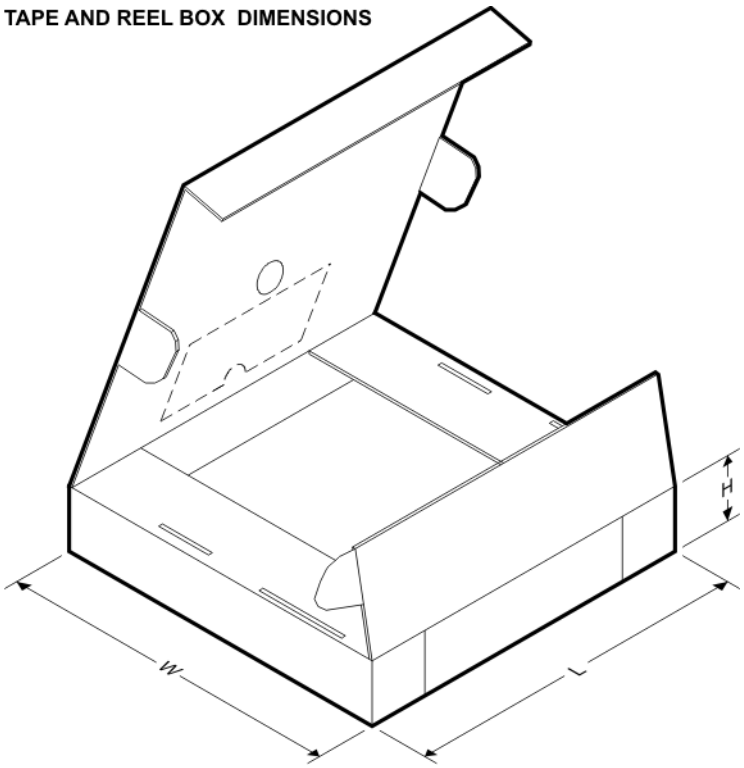
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA695IDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
OPA695IDBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
OPA695IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA695IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA695IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

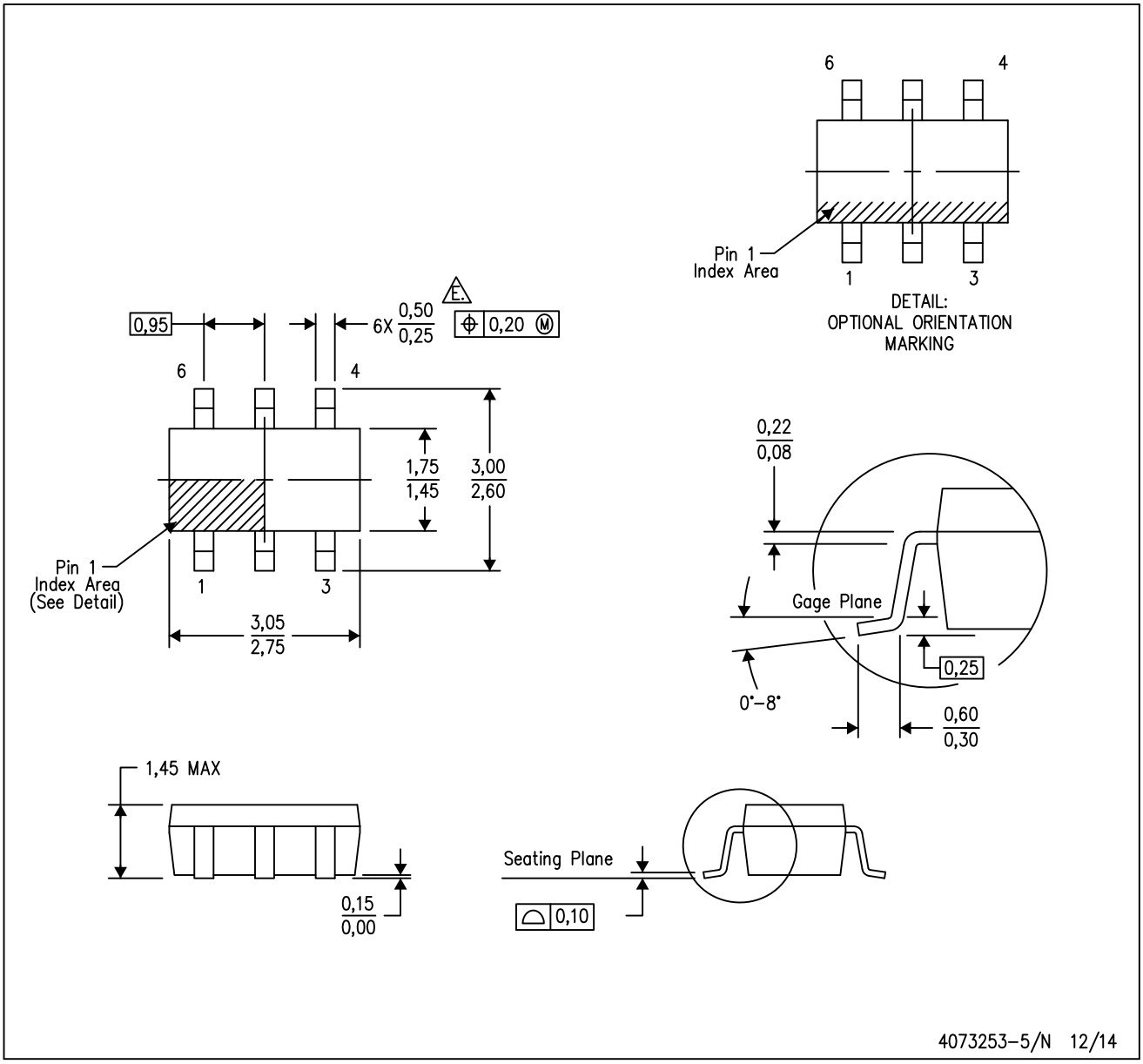
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

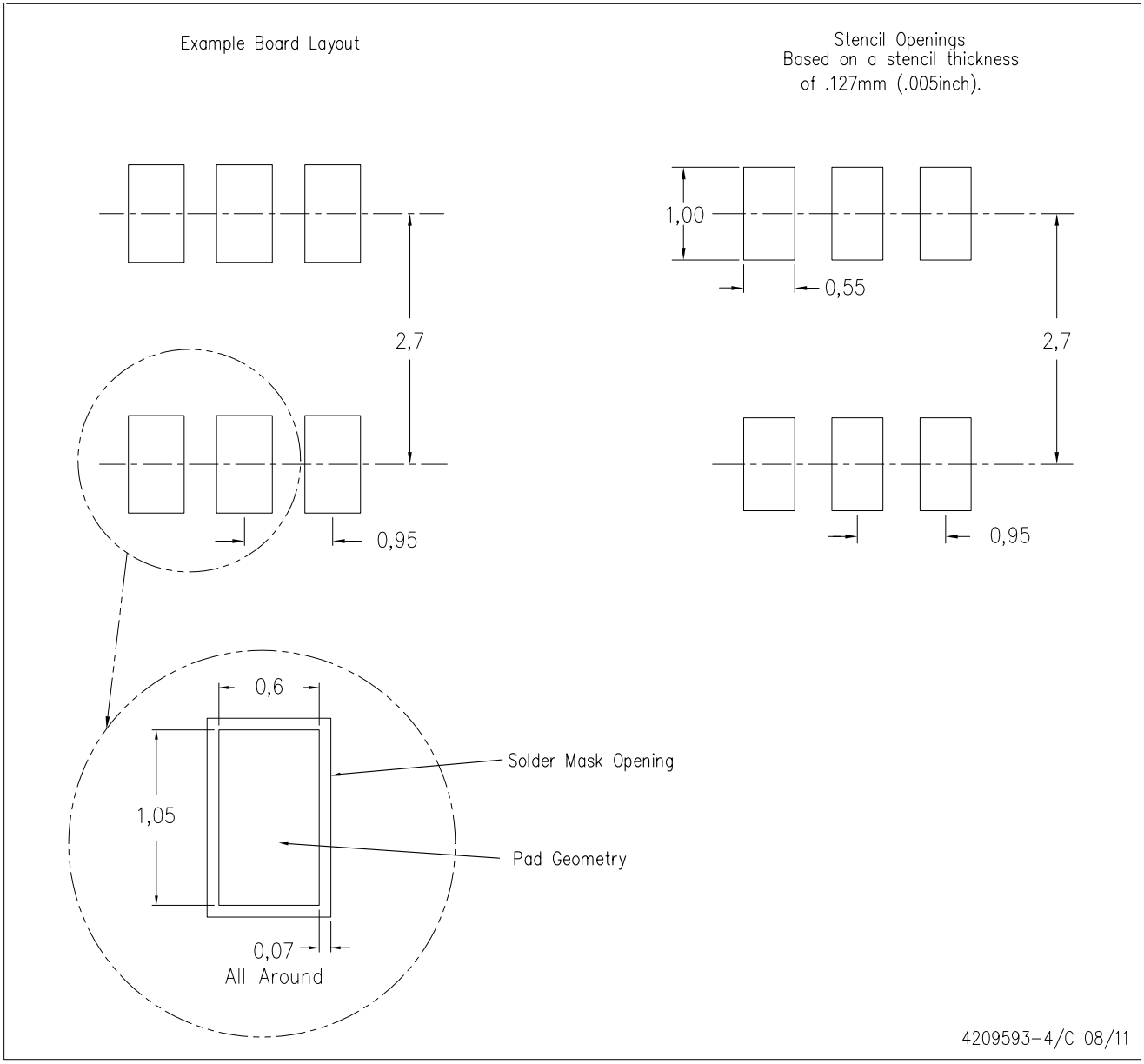
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA695IDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
OPA695IDBVT	SOT-23	DBV	6	250	210.0	185.0	35.0
OPA695IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA695IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA695IDR	SOIC	D	8	2500	367.0	367.0	35.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



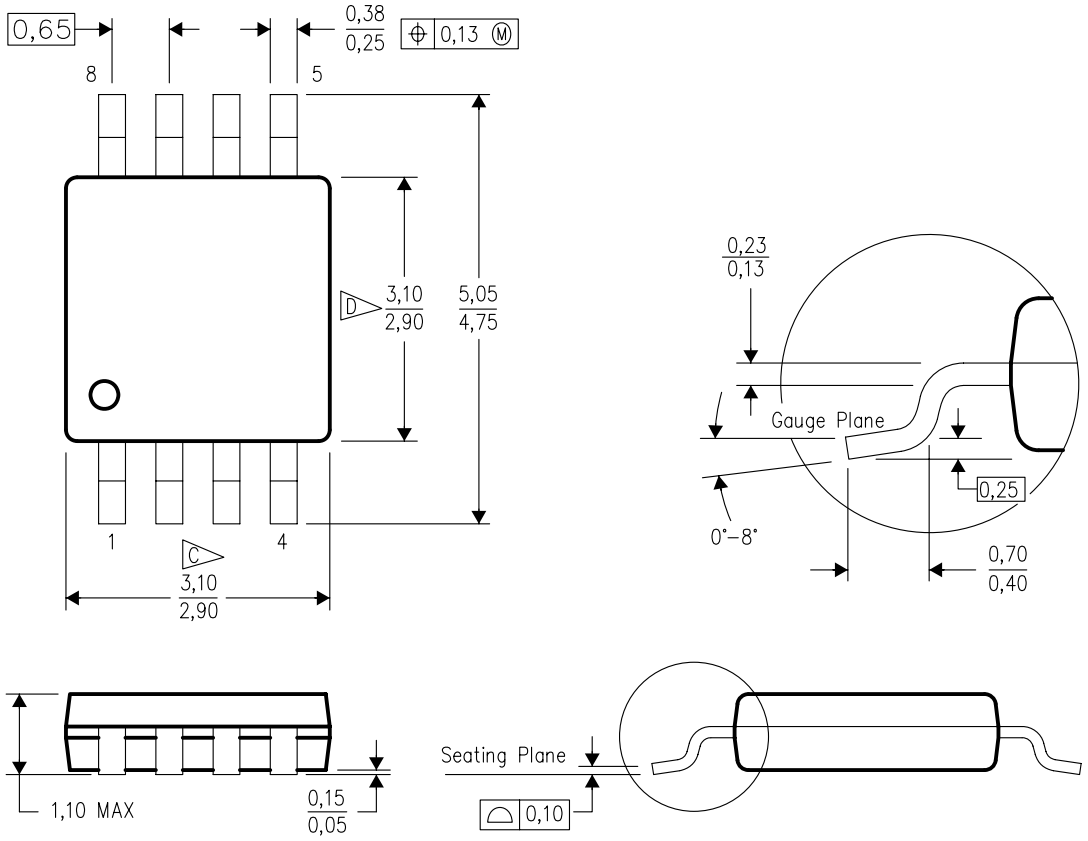
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

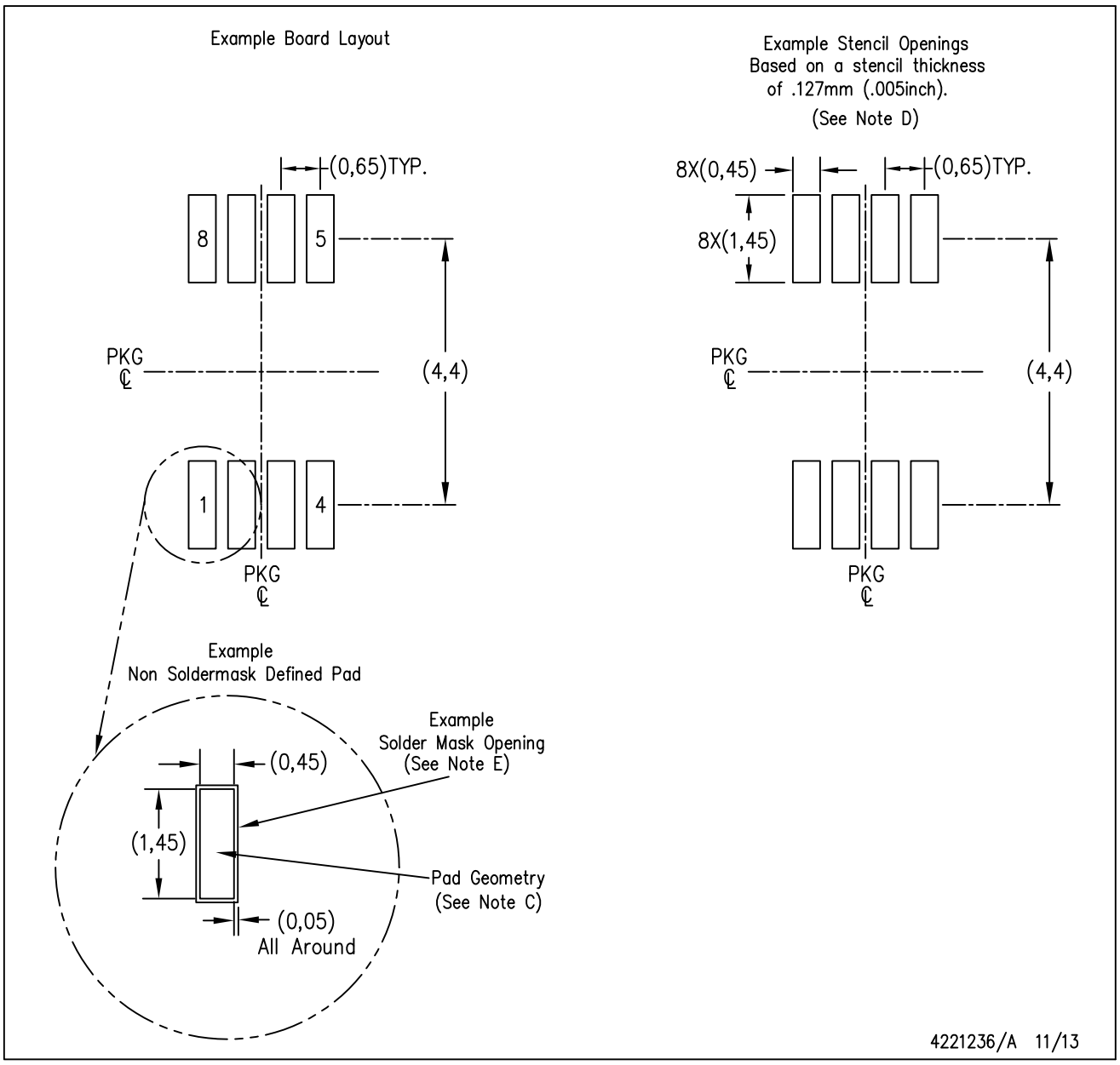
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

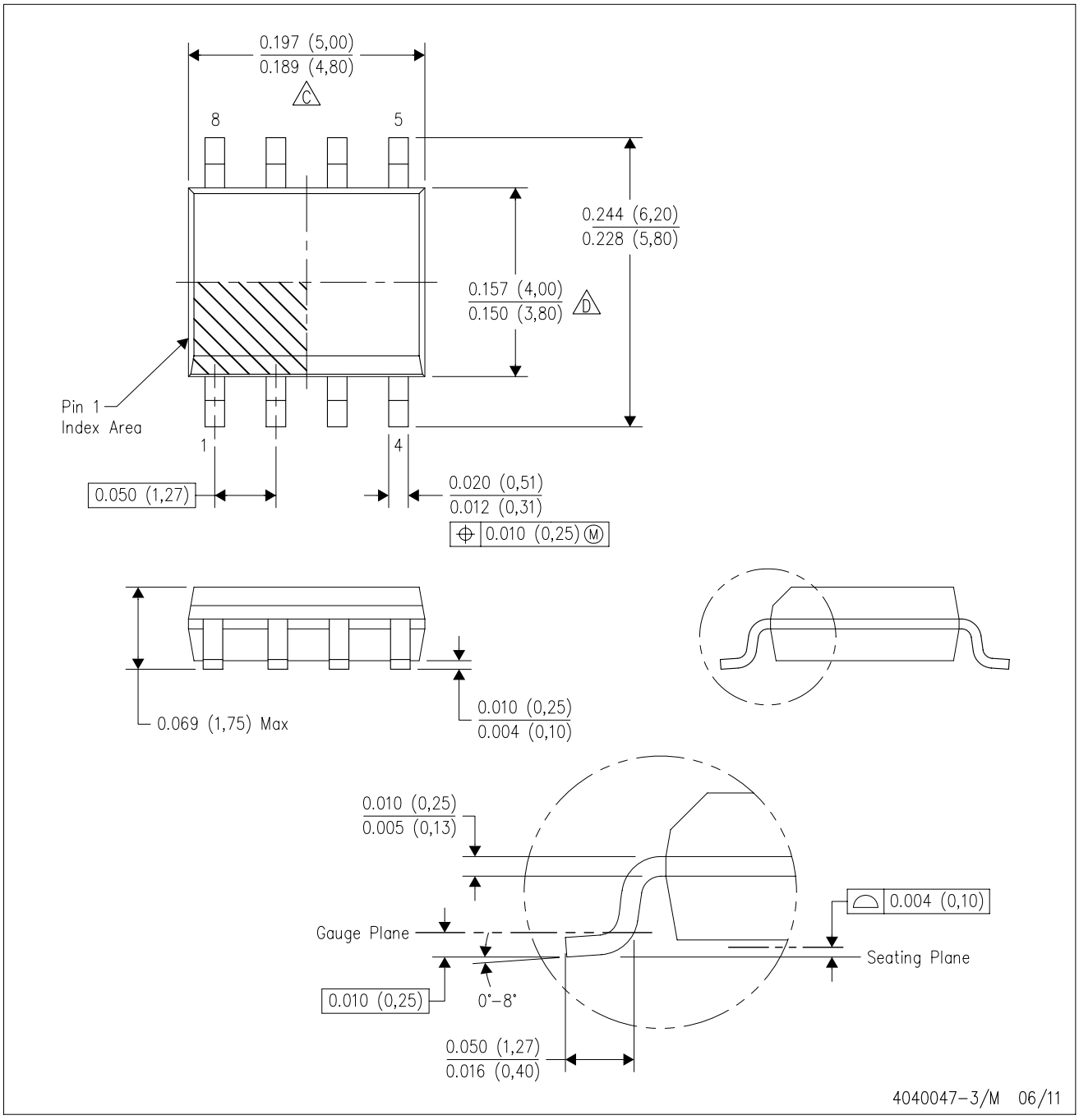
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



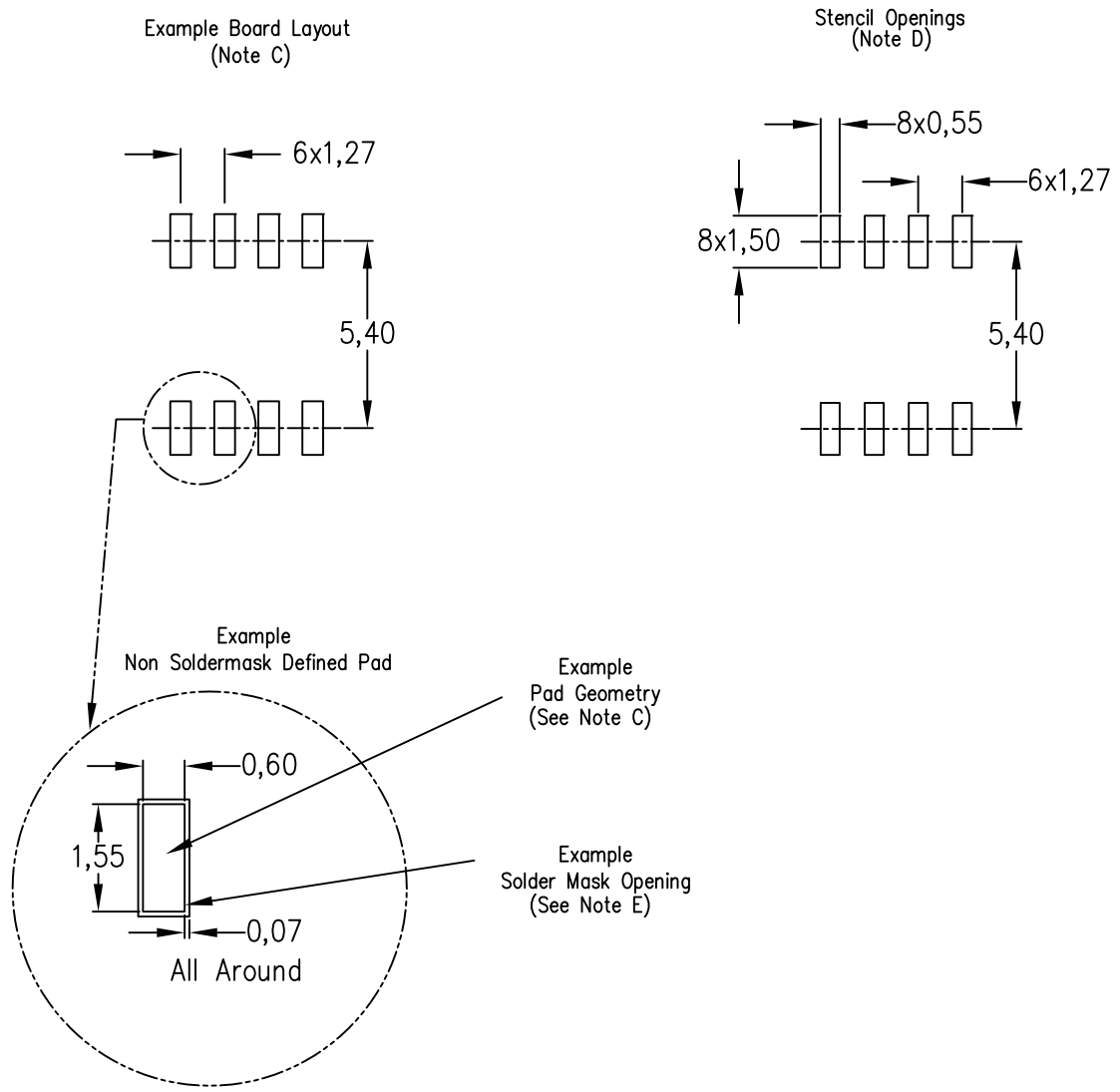
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265