

CMOS BCD Rate Multiplier

High-Voltage Types (20-Volt Rating)

■ CD4527B is a low-power 4-bit digital rate multiplier that provides an output-pulse rate which is the clock-input-pulse rate multiplied by 1/10 times the BCD input. For example, when the BCD input is 8, there will be 8 output pulses for every 10 input pulses. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric functions, A/D and D/A conversion, and frequency division.

For fractional multipliers with more than one digit, CD4527B devices may be cascaded in two different modes: the Add mode and the Multiply mode. (See Figs.12 and 15). In the Add mode,

$$\text{Output Rate} = (\text{Clock Rate}) \left[\begin{matrix} 0.1 \text{ BCD}_1 + 0.01 \text{ BCD}_2 + \\ 0.001 \text{ BCD}_3 + \dots \end{matrix} \right]$$

In the Multiply mode, the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second one,

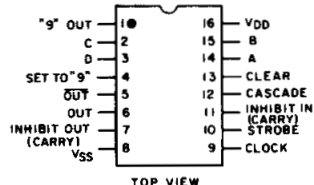
$$\text{e.g. } \frac{9}{10} \times \frac{4}{10} = \frac{36}{100} \text{ or 36 output}$$

pulses for every 100 clock input pulses.

The CD4527B types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Applications:

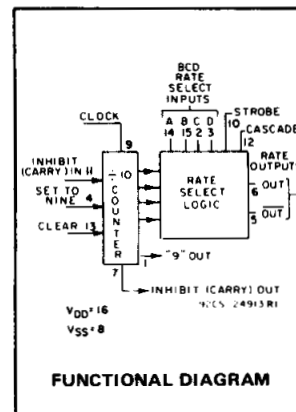
- Numerical control
- Instrumentation
- Digital filtering
- Frequency synthesis



TERMINAL ASSIGNMENT

Features:

- Cascadable in multiples of 4-bits
- Set to "9" input and "9" detect output
- 100% test for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
 - 1 V at V_{DD} = 5 V
 - 2 V at V_{DD} = 10 V
 - 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, 'Standard Specifications for Description of 'B' Series CMOS Devices'



MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT ±10mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -55°C to +100°C 500mW

For T_A = +100°C to +125°C Derate Linearity at 12mW/°C to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)..... 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to +125°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max +265°C

RECOMMENDED OPERATING CONDITIONS AT T_A = 25°C, Except as Noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | V _{DD} (V) | LIMITS | | UNITS | |
|--|--|--------|------|-------|----|
| | | Min. | Max. | | |
| Supply Voltage Range (For T _A = Full Package-Temperature Range) | | 3 | 18 | V | |
| Set or Clear Pulse Width, t _W | 5 | 160 | — | ns | |
| | 10 | 90 | — | | |
| | 15 | 60 | — | | |
| Clock Pulse Width, t _W | 5 | 330 | — | ns | |
| | 10 | 170 | — | | |
| | 15 | 100 | — | | |
| Clock Frequency, f _{CL} | 5 | — | 1.2 | MHz | |
| | 10 | dc | 2.5 | | |
| | 15 | — | 3.5 | | |
| Clock Rise or Fall Time, t _{rCL} or t _{fCL} | 5,10,15 | — | 15 | μs | |
| | Inhibit In Setup Time, t _{SU} | 5 | 100 | — | ns |
| | | 10 | 40 | — | |
| 15 | | 20 | — | | |
| Inhibit In Removal Time, t _{REM} | 5 | 240 | — | ns | |
| | 10 | 130 | — | | |
| | 15 | 110 | — | | |
| Set Removal Time, t _{REM} | 5 | 150 | — | ns | |
| | 10 | 80 | — | | |
| | 15 | 50 | — | | |
| Clear Removal Time, t _{REM} | 5 | 60 | — | ns | |
| | 10 | 40 | — | | |
| | 15 | 30 | — | | |

CD4527B Types

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|--|--------------------|---------------------|---------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | | | | | +25 | | | |
| | | | | -55 | -40 | +85 | +125 | Min. | Typ. | Max. | |
| Quiescent Device Current, I _{DD} Max. | - | 0,5 | 5 | 5 | 5 | 150 | 150 | - | 0.04 | 5 | μA |
| | - | 0,10 | 10 | 10 | 10 | 300 | 300 | - | 0.04 | 10 | |
| | - | 0,15 | 15 | 20 | 20 | 600 | 600 | - | 0.04 | 20 | |
| | - | 0,20 | 20 | 100 | 100 | 3000 | 3000 | - | 0.08 | 100 | |
| Output Low (Sink) Current I _{OL} Min. | 0.4 | 0,5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | - | mA |
| | 0.5 | 0,10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | - | |
| | 1.5 | 0,15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | - | |
| Output High (Source) Current, I _{OH} Min. | 4.6 | 0,5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | - | mA |
| | 2.5 | 0,5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | - | |
| | 9.5 | 0,10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | - | |
| Output Voltage: Low-Level, V _{OL} Max. | - | 0,5 | 5 | 0.05 | | | | - | 0 | 0.05 | V |
| | - | 0,10 | 10 | 0.05 | | | | - | 0 | 0.05 | |
| | - | 0,15 | 15 | 0.05 | | | | - | 0 | 0.05 | |
| Output Voltage: High-Level, V _{OH} Min. | - | 0,5 | 5 | 4.95 | | | | 4.95 | 5 | - | V |
| | - | 0,10 | 10 | 9.95 | | | | 9.95 | 10 | - | |
| | - | 0,15 | 15 | 14.95 | | | | 14.95 | 15 | - | |
| Input Low Voltage, V _{IL} Max. | 0.5, 4.5 | - | 5 | 1.5 | | | | - | - | 1.5 | V |
| | 1,9 | - | 10 | 3 | | | | - | - | 3 | |
| | 1.5, 13.5 | - | 15 | 4 | | | | - | - | 4 | |
| Input High Voltage, V _{IH} Min. | 0.5, 4.5 | - | 5 | 3.5 | | | | 3.5 | - | - | V |
| | 1,9 | - | 10 | 7 | | | | 7 | - | - | |
| | 1.5, 13.5 | - | 15 | 11 | | | | 11 | - | - | |
| Input Current I _{IN} Max. | | 0,18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | - | ±10 ⁻⁵ | ±0.1 | μA |

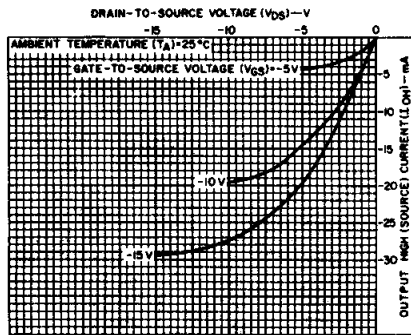


Fig. 3 - Typical output high (source) current characteristics.

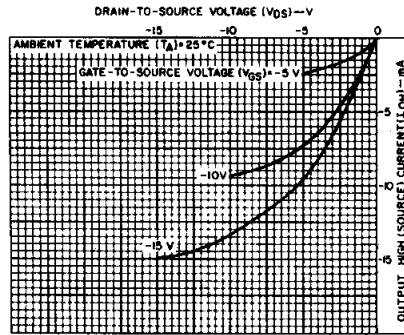


Fig. 4 - Minimum output high (source) current characteristics.

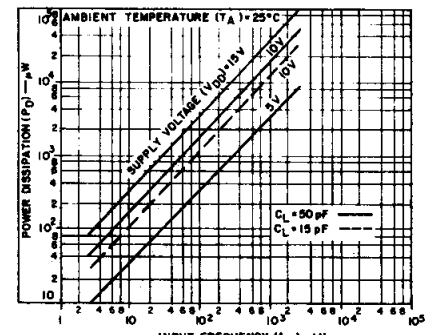


Fig. 5 - Typical dynamic power dissipation as a function of input frequency.

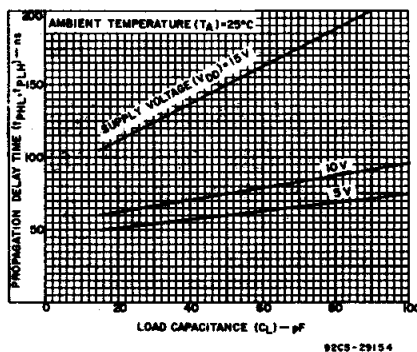


Fig. 6 - Typical propagation delay time as a function of load capacitance (Clock or Strobe to Out).

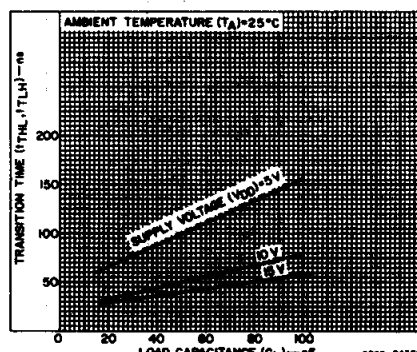


Fig. 7 - Typical transition time as a function of load capacitance.

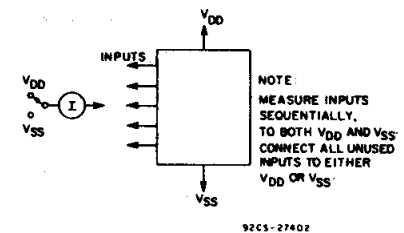


Fig. 8 - Input current test circuit.

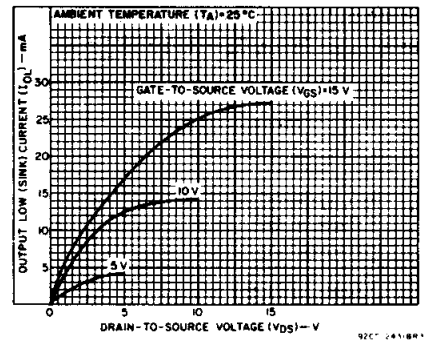


Fig. 1 - Typical output low (sink) current characteristics.

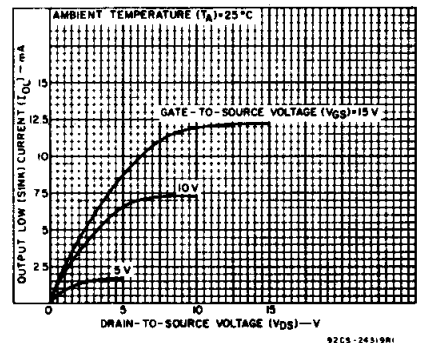


Fig. 2 - Minimum output low (sink) current characteristics.

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COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4527B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C:
 Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

| CHARACTERISTIC | TEST CONDITIONS | LIMITS | | | UNITS |
|---|-----------------|---------------------|------|------|-------|
| | | V _{DD} (V) | Min. | Typ. | |
| Propagation Delay Time, t _{PHL} , t _{PLH} Clock to Out | | 5 | — | 110 | ns |
| | | 10 | — | 55 | |
| | | 15 | — | 45 | |
| Clock or Strobe to Out | | 5 | — | 150 | ns |
| | | 10 | — | 75 | |
| | | 15 | — | 60 | |
| Clock to Inhibit Out High Level to Low Level | | 5 | — | 320 | ns |
| | | 10 | — | 145 | |
| | | 15 | — | 100 | |
| Low Level to High Level | | 5 | — | 250 | ns |
| | | 10 | — | 100 | |
| | | 15 | — | 75 | |
| Clear to Out | | 5 | — | 380 | ns |
| | | 10 | — | 175 | |
| | | 15 | — | 130 | |
| Clock to "9" or "15" Out | | 5 | — | 300 | ns |
| | | 10 | — | 125 | |
| | | 15 | — | 90 | |
| Cascade to Out | | 5 | — | 90 | ns |
| | | 10 | — | 45 | |
| | | 15 | — | 35 | |
| Inhibit In to Inhibit Out | | 5 | — | 130 | ns |
| | | 10 | — | 60 | |
| | | 15 | — | 45 | |
| Set to Out | | 5 | — | 330 | ns |
| | | 10 | — | 150 | |
| | | 15 | — | 110 | |
| Transition Time, t _{THL} , t _{TLH} | | 5 | — | 100 | ns |
| | | 10 | — | 50 | |
| | | 15 | — | 40 | |
| Maximum Clock Frequency, f _{CL} | | 5 | 1.2 | 2.4 | MHz |
| | | 10 | 2.5 | 5 | |
| | | 15 | 3.5 | 7 | |
| Minimum Clock Pulse Width, t _w | | 5 | — | 165 | ns |
| | | 10 | — | 85 | |
| | | 15 | — | 50 | |
| Clock Rise or Fall Time, t _{rCL} , t _{fCL} | | 5 | — | 15 | μs |
| | | 10 | — | 15 | |
| | | 15 | — | 15 | |
| Minimum Set or Clear Pulse Width, t _w | | 5 | — | 80 | ns |
| | | 10 | — | 45 | |
| | | 15 | — | 30 | |
| Minimum Inhibit In Setup Time, t _{SU} | | 5 | — | 50 | ns |
| | | 10 | — | 20 | |
| | | 15 | — | 10 | |
| Minimum Inhibit In Removal Time, t _{REM} | | 5 | — | 120 | ns |
| | | 10 | — | 65 | |
| | | 15 | — | 55 | |
| Minimum Set Removal Time, t _{REM} | | 5 | — | 75 | ns |
| | | 10 | — | 40 | |
| | | 15 | — | 25 | |
| Minimum Clear Removal Time, T _{REM} | | 5 | — | 30 | ns |
| | | 10 | — | 20 | |
| | | 15 | — | 15 | |
| Input Capacitance, C _{IN} | Any Input | | — | 5 | pF |

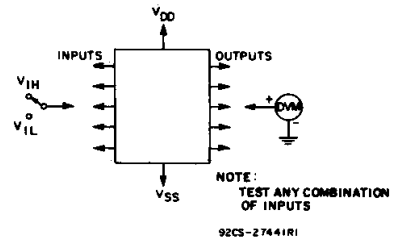


Fig. 9 - Input voltage test circuit.

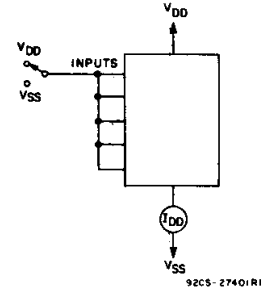


Fig. 10 - Quiescent device current test circuit.

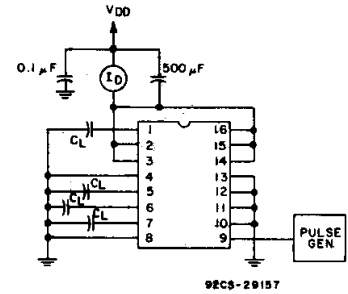


Fig. 11 - Dynamic power dissipation test circuit.

APPLICATIONS

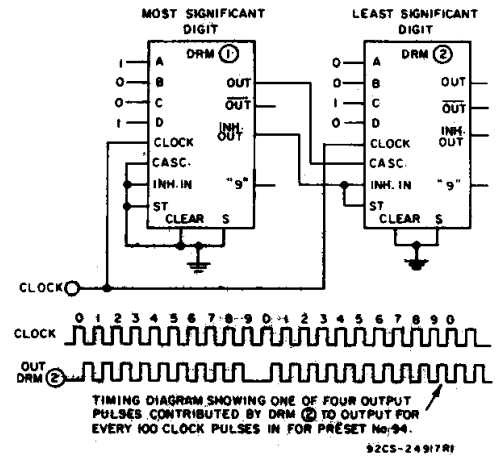


Fig. 12 - Two CD4527B's cascaded in the "Add" mode with a preset number

$$\text{of } 94 \left(\frac{9}{10} + \frac{4}{100} = \frac{94}{100} \right)$$

CD4527B Types

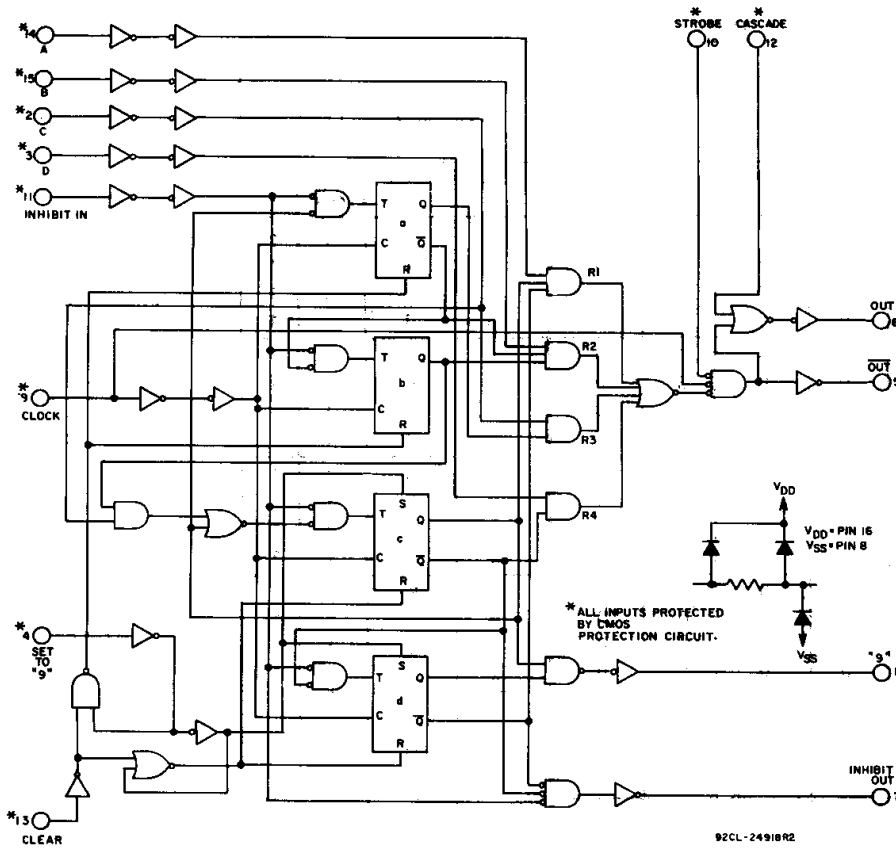


Fig. 13 - Logic diagram.

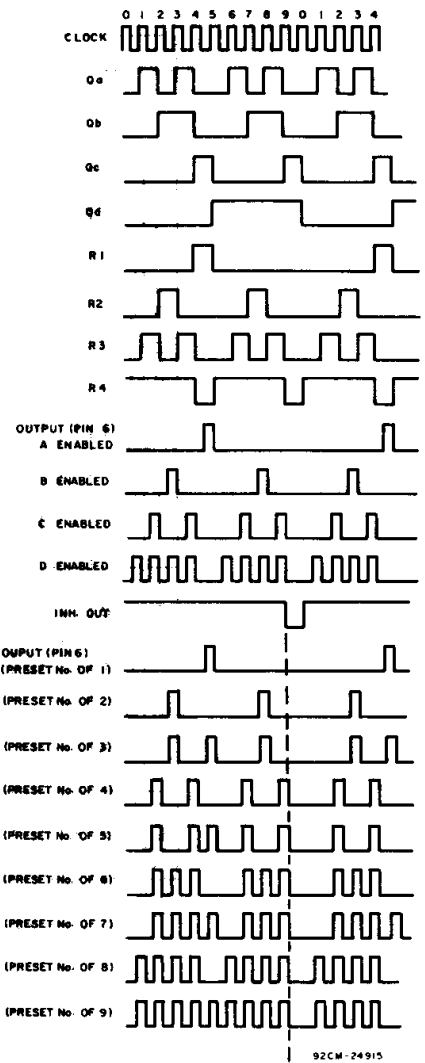
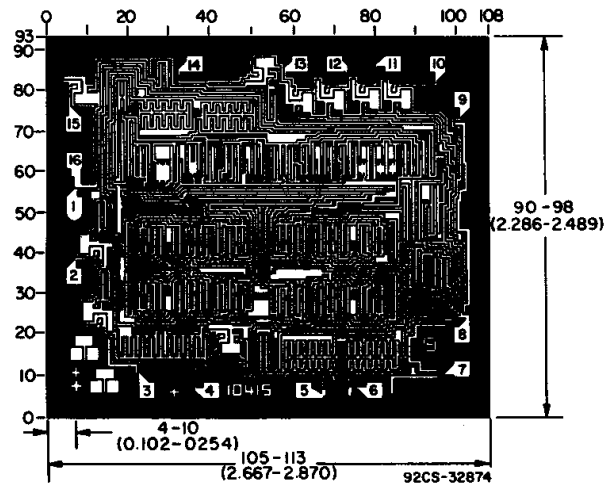


Fig. 14 - Timing diagram (See Logic Diagram).



Dimensions and Pad Layout for CD4527BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

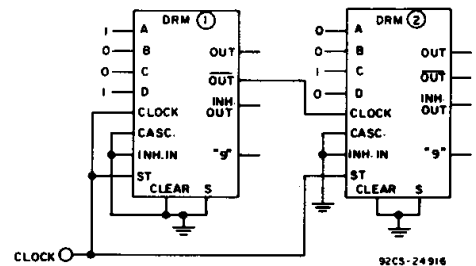


Fig. 15 - Two CD4527B's cascaded in the "Multiply" mode with a preset number

$$\text{of } 36 \left(\frac{9}{10} \times \frac{4}{10} = \frac{36}{100} \right)$$

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HIGH VOLTAGE ICs

CD4527B Types

TRUTH TABLE

| INPUTS | | | | | | | | | | OUTPUTS | | | |
|--|---|---|---|-----|-----------|-----|-----|----------|----------|---|-------------------------|------------|------------|
| Number of Pulses or Input Logic Level (0 = Low; 1 = High; X = Don't Care) | | | | | | | | | | Number of Pulses or Output Logic Level (L = Low; H = High) | | | |
| D | C | B | A | CLK | INH IN | STR | CAS | CLR # | SET # | OUT | $\overline{\text{OUT}}$ | INH OUT | "9" OUT |
| 0 | 0 | 0 | 0 | 10 | 0 | 0 | 0 | 0 | 0 | L | H | 1 | 1 |
| 0 | 0 | 0 | 1 | 10 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 10 | 0 | 0 | 0 | 0 | 0 | 2 | 2 | 1 | 1 |
| 0 | 0 | 1 | 1 | 10 | 0 | 0 | 0 | 0 | 0 | 3 | 3 | 1 | 1 |
| 0 | 1 | 0 | 0 | 10 | 0 | 0 | 0 | 0 | 0 | 4 | 4 | 1 | 1 |
| 0 | 1 | 0 | 1 | 10 | 0 | 0 | 0 | 0 | 0 | 5 | 5 | 1 | 1 |
| 0 | 1 | 1 | 0 | 10 | 0 | 0 | 0 | 0 | 0 | 6 | 6 | 1 | 1 |
| 0 | 1 | 1 | 1 | 10 | 0 | 0 | 0 | 0 | 0 | 7 | 7 | 1 | 1 |
| 1 | 0 | 0 | 0 | 10 | 0 | 0 | 0 | 0 | 0 | 8 | 8 | 1 | 1 |
| 1 | 0 | 0 | 1 | 10 | 0 | 0 | 0 | 0 | 0 | 9 | 9 | 1 | 1 |
| 1 | 0 | 1 | 0 | 10 | 0 | 0 | 0 | 0 | 0 | 8 | 8 | 1 | 1 |
| 1 | 0 | 1 | 1 | 10 | 0 | 0 | 0 | 0 | 0 | 9 | 9 | 1 | 1 |
| 1 | 1 | 0 | 0 | 10 | 0 | 0 | 0 | 0 | 0 | 8 | 8 | 1 | 1 |
| 1 | 1 | 0 | 1 | 10 | 0 | 0 | 0 | 0 | 0 | 9 | 9 | 1 | 1 |
| 1 | 1 | 1 | 0 | 10 | 0 | 0 | 0 | 0 | 0 | 8 | 8 | 1 | 1 |
| 1 | 1 | 1 | 1 | 10 | 0 | 0 | 0 | 0 | 0 | 9 | 9 | 1 | 1 |
| X | X | X | X | 10 | 1 | 0 | 0 | 0 | 0 | † | † | H | † |
| X | X | X | X | 10 | 0 | 1 | 0 | 0 | 0 | L | H | 1 | 1 |
| X | X | X | X | 10 | 0 | 0 | 1 | 0 | 0 | H | * | 1 | 1 |
| 1 | X | X | X | 10 | 0 | 0 | 0 | 1 | 0 | 10 | 10 | H | L |
| 0 | X | X | X | 10 | 0 | 0 | 0 | 1 | 0 | L | H | H | L |
| X | X | X | X | 10 | 0 | 0 | 0 | 0 | 1 | L | H | L | H |

* Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).

† Depends on internal state of counter.

#Clear and Set Inputs should not be high at the same time; device draws increased quiescent current when in this non-valid state.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CD4527BE | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD4527BE | Samples |
| CD4527BEE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD4527BE | Samples |
| CD4527BNSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4527B | Samples |
| CD4527BNSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4527B | Samples |
| CD4527BPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM527B | Samples |
| CD4527BPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM527B | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4527BNSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD4527BPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4527BNSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| CD4527BPWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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