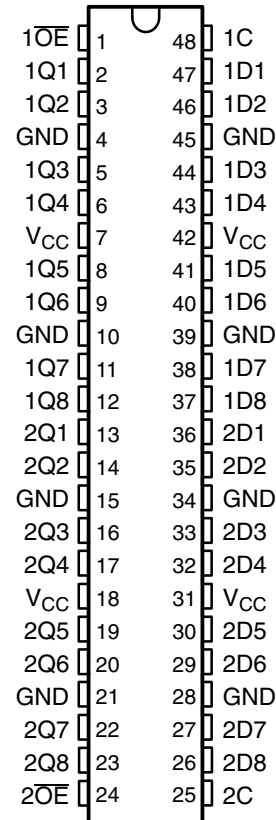


SN54ACT16373, 74ACT16373 16-BIT D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS122C – MARCH 1990 – REVISED SEPTEMBER 1996

- Members of the Texas Instruments *Widebus*™ Family
- Inputs Are TTL-Voltage Compatible
- 3-State Bus Driving True Outputs
- Full Parallel Access for Loading
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Shrink Small-Outline (DL) 300-mil Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings

SN54ACT16373 . . . WD PACKAGE
74ACT16373 . . . DL PACKAGE
(TOP VIEW)



description

The SN54ACT16373 and 74ACT16373 are 16-bit D-type transparent latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. These devices can be used as two 8-bit latches or one 16-bit latch. The Q outputs of the latches follow the data (D) inputs if enable C is taken high. When C is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines in a bus-organized system without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74ACT16373 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ACT16373 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT16373 is characterized for operation from -40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
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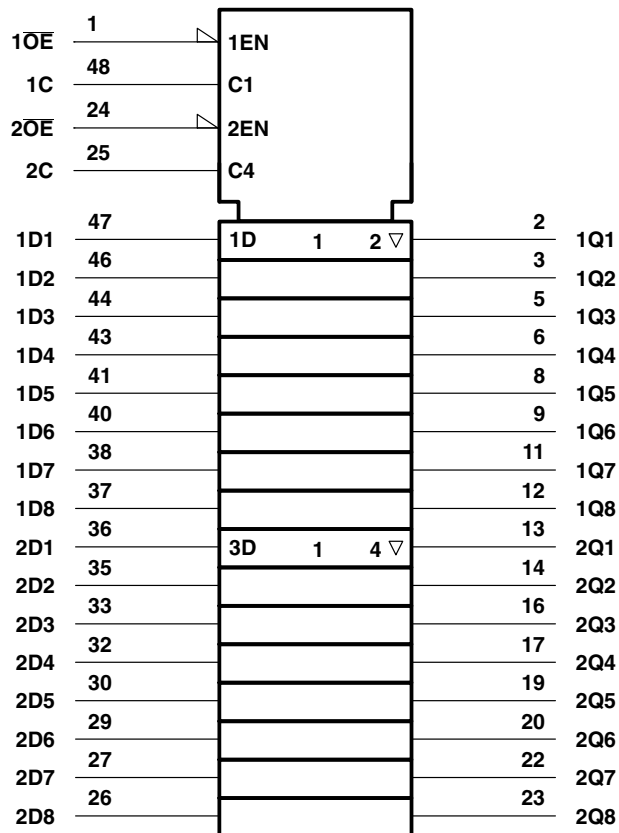
SN54ACT16373, 74ACT16373 16-BIT D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

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FUNCTION TABLE

| INPUTS | | | OUTPUT |
|-----------------|---|---|--------|
| \overline{OE} | C | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q_0 |
| H | X | X | Z |

logic symbol†

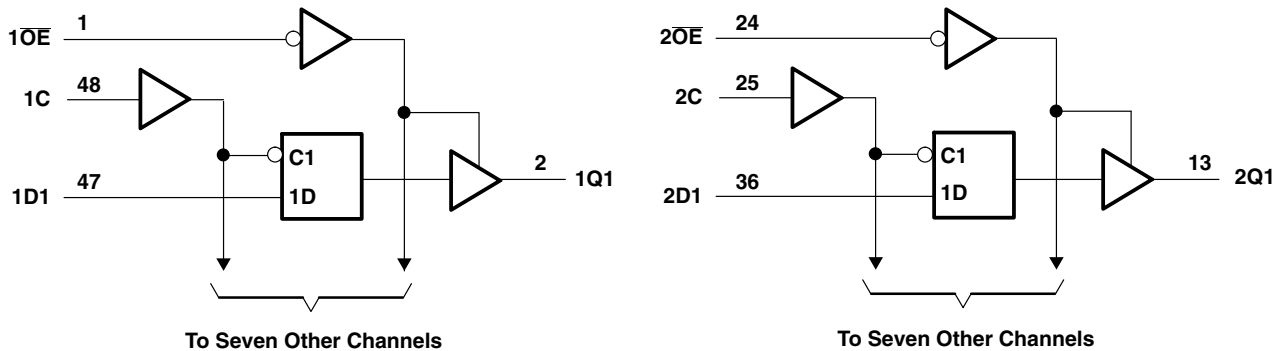


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54ACT16373, 74ACT16373 16-BIT D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|---|--|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to $V_{CC} + 0.5$ V |
| Output voltage range, V_O (see Note 1) | -0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) | ± 20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ± 50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 50 mA |
| Continuous current through V_{CC} or GND | ± 400 mA |
| Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package | 1.2 W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

| | SN54ACT16373 | | 74ACT16373 | | UNIT |
|--|--------------|----------|------------|----------|------------------|
| | MIN | MAX | MIN | MAX | |
| V_{CC} Supply voltage (see Note 4) | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V_{IH} High-level input voltage | 2 | | 2 | | V |
| V_{IL} Low-level input voltage | | 0.8 | | 0.8 | V |
| V_I Input voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| V_O Output voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} High-level output current | | -24 | | -24 | mA |
| I_{OL} Low-level output current | | 24 | | 24 | mA |
| $\Delta t/\Delta v$ Input transition rise or fall rate | 0 | 10 | 0 | 10 | ns/V |
| T_A Operating free-air temperature | -55 | 125 | -40 | 85 | $^\circ\text{C}$ |

- NOTES: 3. Unused inputs should be tied to V_{CC} through a pullup resistor of approximately 5 k Ω or greater to prevent them from floating.
4. All V_{CC} and GND pins must be connected to the proper voltage supply.

SN54ACT16373, 74ACT16373 16-BIT D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS122C – MARCH 1990 – REVISED SEPTEMBER 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54ACT16373 | | 74ACT16373 | | UNIT |
|---------------------------------------|---|-----------------|-----------------------|-----|------|--------------|------|------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = -50 μA | 4.5 V | 4.4 | | | 4.4 | | 4.4 | V | |
| | | 5.5 V | 5.4 | | | 5.4 | | 5.4 | | |
| | I _{OH} = -24 mA | 4.5 V | 3.94 | | | 3.7 | | 3.8 | | |
| | | 5.5 V | 4.94 | | | 4.7 | | 4.8 | | |
| | I _{OH} = -50 mA [†] | 5.5 V | | | | 3.85 | | | | |
| I _{OH} = -75 mA [†] | 5.5 V | | | | | | 3.85 | | | |
| V _{OL} | I _{OL} = 50 μA | 4.5 V | | | 0.1 | | 0.1 | 0.1 | V | |
| | | 5.5 V | | | 0.1 | | 0.1 | 0.1 | | |
| | I _{OL} = 24 mA | 4.5 V | | | 0.36 | | 0.5 | 0.44 | | |
| | | 5.5 V | | | 0.36 | | 0.5 | 0.44 | | |
| | I _{OL} = 50 mA [†] | 5.5 V | | | | | 1.65 | | | |
| I _{OL} = 75 mA [†] | 5.5 V | | | | | | 1.65 | | | |
| I _I | V _I = V _{CC} or GND | 5.5 V | | | ±0.1 | | ±1 | ±1 | μA | |
| I _{OZ} | V _O = V _{CC} or GND | 5.5 V | | | ±0.5 | | ±10 | ±5 | μA | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 8 | | 160 | 80 | μA | |
| ΔI _{CC} [‡] | One input at 3.4 V, Other inputs at GND or V _{CC} | 5.5 V | | | 0.9 | | 1 | 1 | mA | |
| C _i | V _I = V _{CC} or GND | 5 V | | | 4.5 | | | | pF | |
| C _o | V _I = V _{CC} or GND | 5 V | | | 12 | | | | pF | |

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| | | T _A = 25°C | | SN54ACT16373 | | 74ACT16373 | | UNIT |
|-----------------|-----------------------------|-----------------------|-----|--------------|-----|------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _w | Pulse duration, LE high | 4 | | 4 | | 1 | | ns |
| t _{su} | Setup time, data before LE↓ | 1 | | 1 | | 1 | | ns |
| t _h | Hold time, data after LE↓ | 5 | | 5 | | 5 | | ns |

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | T _A = 25°C | | | SN54ACT16373 | | 74ACT16373 | | UNIT |
|------------------|--------------|-------------|-----------------------|-----|------|--------------|------|------------|------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | D | Q | 3.8 | 7.9 | 9.4 | 3.8 | 11.8 | 3.8 | 11.1 | ns |
| t _{PHL} | | | 3.1 | 8.2 | 9.7 | 3.1 | 13 | 3.1 | 12.3 | |
| t _{PLH} | LE | Q | 4.6 | 9.3 | 10.8 | 4.6 | 13.7 | 4.6 | 12.8 | ns |
| t _{PHL} | | | 4.5 | 9.1 | 10.5 | 4.5 | 13 | 4.5 | 12.2 | |
| t _{PZH} | OE | Q | 3.1 | 8 | 9.5 | 3.1 | 13 | 3.1 | 12.1 | ns |
| t _{PZL} | | | 3.8 | 9.4 | 11.1 | 3.8 | 15.1 | 3.8 | 14.2 | |
| t _{PHZ} | OE | Q | 5.3 | 8.6 | 9.9 | 5.3 | 11 | 5.3 | 10.7 | ns |
| t _{PLZ} | | | 4.3 | 7.4 | 8.7 | 4.3 | 9.8 | 4.3 | 9.4 | |



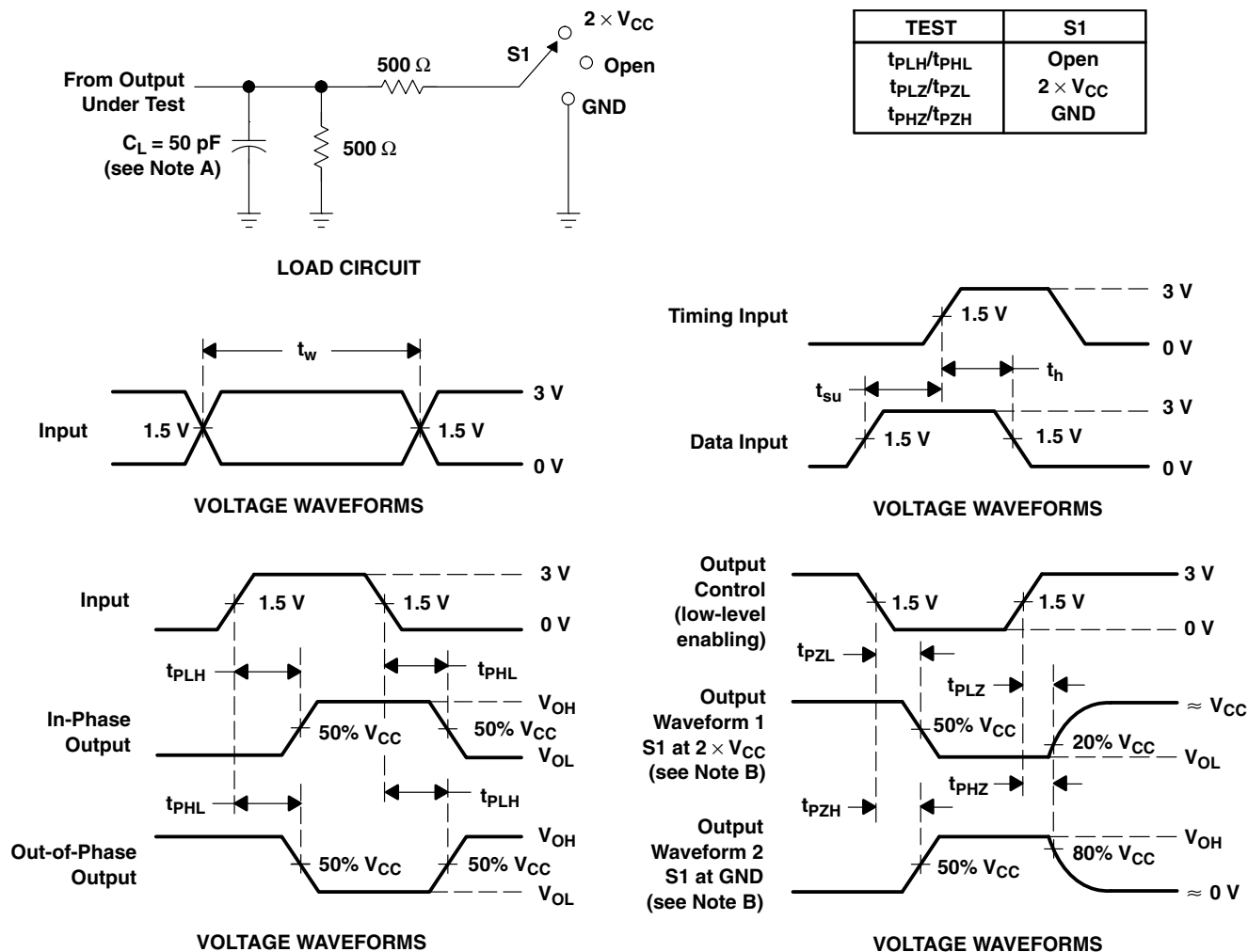
SN54ACT16373, 74ACT16373 16-BIT D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS122C – MARCH 1990 – REVISED SEPTEMBER 1996

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------|---|------------------|-----|------|
| C_{pd} | Power dissipation capacitance per latch | Outputs enabled | 43 | pF |
| | | Outputs disabled | 4.5 | |

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|--|-------------------------|
| 5962-9202401MXA | ACTIVE | CFP | WD | 48 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9202401MX A SNJ54ACT16373W D | Samples |
| 74ACT16373DL | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT16373 | Samples |
| 74ACT16373DLG4 | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT16373 | Samples |
| 74ACT16373DLR | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT16373 | Samples |
| 74ACT16373DLRG4 | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT16373 | Samples |
| SNJ54ACT16373WD | ACTIVE | CFP | WD | 48 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9202401MX A SNJ54ACT16373W D | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74ACT16373DLR | SSOP | DL | 48 | 1000 | 330.0 | 32.4 | 11.35 | 16.2 | 3.1 | 16.0 | 32.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74ACT16373DLR | SSOP | DL | 48 | 1000 | 367.0 | 367.0 | 55.0 |

WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
 GDFP1-F56 and JEDEC MO-146AB

MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

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