- 2-V to 6-V V_{CC} Operation
- Inputs Accept Voltages to 6 V
- Max t_{pd} of 11 ns at 5 V
- 3-State Inverting Outputs Drive Bus Lines Directly
- Full Parallel Access for Loading
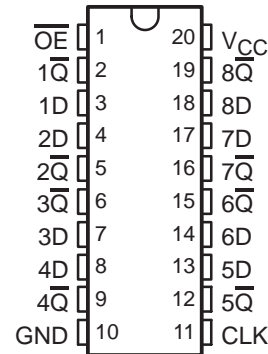
description/ordering information

These octal edge-triggered D-type flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the $\overline{Q}$ outputs are set to the complements of the logic levels set up at the data (D) inputs.
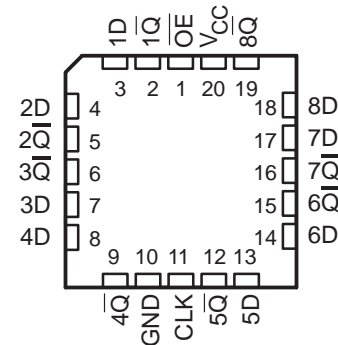
A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

SN54AC534 . . . J OR W PACKAGE
SN74AC534 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)

$\overline{OE}$	1		20	V_{CC}
$1\overline{Q}$	2		19	$8\overline{Q}$
1D	3		18	8D
2D	4		17	7D
$2\overline{Q}$	5		16	$7\overline{Q}$
$3\overline{Q}$	6		15	$6\overline{Q}$
3D	7		14	6D
4D	8		13	5D
$4\overline{Q}$	9		12	$5\overline{Q}$
GND	10		11	CLK

SN54AC534 . . . FK PACKAGE
(TOP VIEW)

Top pins: 1D (3), $1\overline{Q}$ (2), $\overline{OE}$ (1), V_{CC} (20), $8\overline{Q}$ (19)

2D	4		18	8D
$2\overline{Q}$	5		17	7D
$3\overline{Q}$	6		16	$7\overline{Q}$
3D	7		15	$6\overline{Q}$
4D	8		14	6D

Bottom pins: $4\overline{Q}$ (9), GND (10), CLK (11), $5\overline{Q}$ (12), 5D (13)

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP – N	Tube	SN74AC534N	SN74AC534N
	SOIC – DW	Tube	SN74AC534DW	AC534
		Tape and reel	SN74AC534DWR	
	SOP – NS	Tape and reel	SN74AC534NSR	AC534
	SSOP – DB	Tape and reel	SN74AC534DBR	AC534
	TSSOP – PW	Tube	SN74AC534PW	AC534
		Tape and reel	SN74AC534PWR	
−55°C to 125°C	CDIP – J	Tube	SNJ54AC534J	SNJ54AC534J
	CFP – W	Tube	SNJ54AC534W	SNJ54AC534W
	LCCC – FK	Tube	SNJ54AC534FK	SNJ54AC534FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

SN54AC534, SN74AC534
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS
SCAS554D – NOVEMBER 1995 – REVISED OCTOBER 2003

description/ordering information (continued)

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{\text{OE}}$	CLK	D	$\overline{\text{Q}}$
L	↑	H	L
L	↑	L	H
L	H or L	X	$\overline{\text{Q}}_0$
H	X	X	Z

logic diagram (positive logic)

To Seven Other Channels
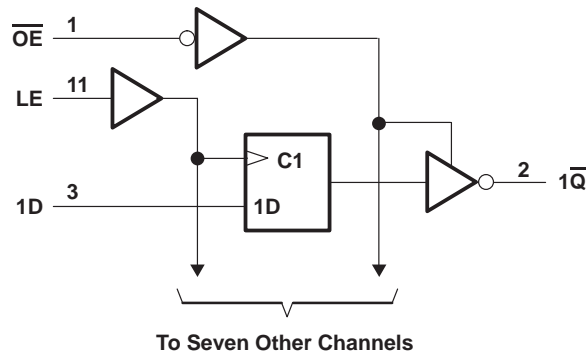
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±200 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package .... 70°C/W
                                                                          DW package .... 58°C/W
                                                                          N package .... 69°C/W
                                                                          NS package .... 60°C/W
                                                                          PW package .... 83°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
        2. The package thermal impedance is calculated in accordance with JESD 51-7.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

recommended operating conditions (see Note 3)

			SN54AC534 MIN	SN54AC534 MAX	SN74AC534 MIN	SN74AC534 MAX	UNIT
V_{CC}	Supply voltage		2	6	2	6	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1		2.1		V
		V_{CC} = 4.5 V	3.15		3.15		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 3 V		0.9		0.9	V
		V_{CC} = 4.5 V		1.35		1.35	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V		−12		−12	mA
		V_{CC} = 4.5 V		−24		−24	
		V_{CC} = 5.5 V		−24		−24	
I_{OL}	Low-level output current	V_{CC} = 3 V		12		12	mA
		V_{CC} = 4.5 V		24		24	
		V_{CC} = 5.5 V		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			8		8	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	SN54AC534 MIN	SN54AC534 MAX	SN74AC534 MIN	SN74AC534 MAX	UNIT
V_{OH}	I_{OH} = −50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −12 mA	3 V	2.56			2.4		2.46		
	I_{OH} = −24 mA	4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
V_{OL}	I_{OL} = 50 µA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±5		±2.5	µA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	µA
C_i	V_I = V_{CC} or GND	5 V		4.5						pF

TEXAS INSTRUMENTS

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3

SN54AC534, SN74AC534
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

SCAS554D – NOVEMBER 1995 – REVISED OCTOBER 2003

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AC534		SN74AC534		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		70		60		70	MHz
t_w	Pulse duration, CLK high or low	5		8		6.5		ns
t_{su}	Setup time, data before CLK↑	5		8		6.5		ns
t_h	Hold time, data after CLK↑	1		3		1.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AC534		SN74AC534		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		150		75		140	MHz
t_w	Pulse duration, CLK high or low	3.5		5.5		4		ns
t_{su}	Setup time, data before CLK↑	3.5		5.5		4		ns
t_h	Hold time, data after CLK↑	1		3		1.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C		SN54AC534		SN74AC534		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			70		60		70		MHz
t_{PLH}	CLK	$\overline{Q}$	3	14	2	17.5	2.5	16	ns
t_{PHL}			3	13	2	16.5	2.5	15	
t_{PZH}	$\overline{OE}$	$\overline{Q}$	3	12.5	2	15.5	2.5	14	ns
t_{PZL}			3	12.5	2	15.5	2.5	14	
t_{PHZ}	$\overline{OE}$	$\overline{Q}$	2	13.5	1	16.5	1.5	15	ns
t_{PLZ}			2	12	1	15	1.5	13.5	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C		SN54AC534		SN74AC534		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		75		140		MHz
t_{PLH}	CLK	$\overline{Q}$	2.5	10.5	1.5	13.5	2	12	ns
t_{PHL}			2.5	9.5	1.5	12.5	2	11	
t_{PZH}	$\overline{OE}$	$\overline{Q}$	2.5	10	1.5	13	2	11.5	ns
t_{PZL}			2.5	10	1.5	13	2	11.5	
t_{PHZ}	$\overline{OE}$	$\overline{Q}$	1.5	11.5	1	14	1	12.5	ns
t_{PLZ}			1.5	10	1	12.5	1	11	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	40	pF

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PARAMETER MEASUREMENT INFORMATION
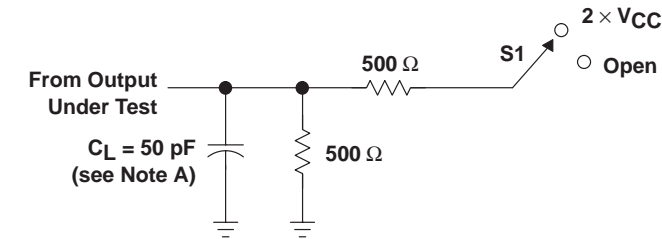
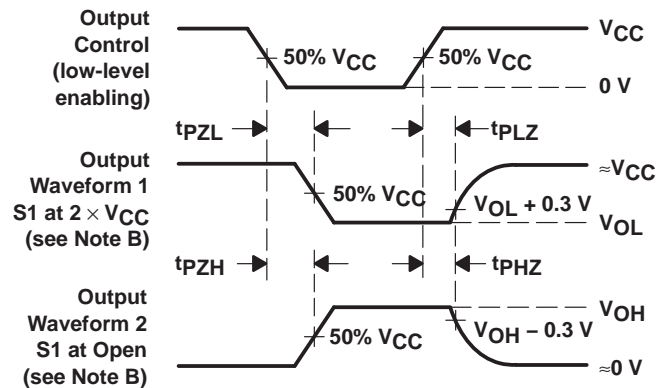| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT
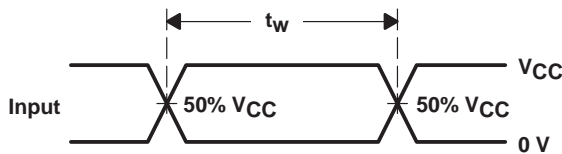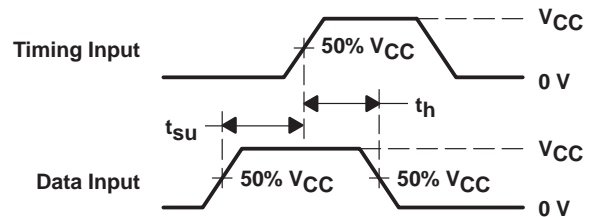
VOLTAGE WAVEFORMS
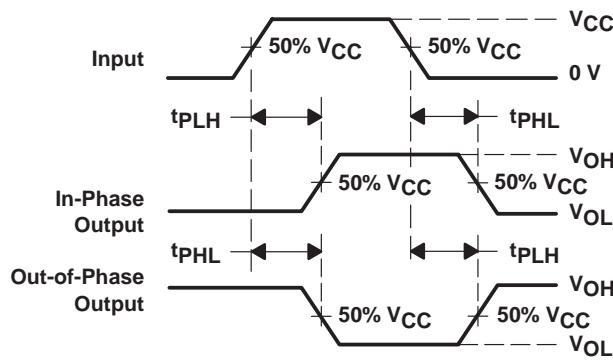
VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
   D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AC534DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	-40 to 85		
SN74AC534DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC534	Samples
SN74AC534DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC534	Samples
SN74AC534DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC534	Samples
SN74AC534N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC534N	Samples
SN74AC534NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC534	Samples
SN74AC534PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC534	Samples
SN74AC534PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		
SN74AC534PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC534	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC534DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AC534DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AC534NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.4	4.0	24.0	Q1
SN74AC534PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC534DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74AC534DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AC534NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AC534PWR	TSSOP	PW	20	2000	367.0	367.0	38.0

N (R−PDIP−T)**   **PLASTIC DUAL−IN−LINE PACKAGE**

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60) / 0.240 (6,10)

1   8

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.010 (0,25) NOM

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

0.430 (10,92) MAX

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

4040049/E   12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
        B.   This drawing is subject to change without notice.
        C.   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
        D.   The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

$\frac{0.512\ (13,00)}{0.496\ (12,60)}$

20   11

$\frac{0.419\ (10,63)}{0.393\ (9,97)}$

$\frac{0.299\ (7,60)}{0.291\ (7,40)}$

1   10

Pin 1
Index Area

0.050 (1,27)

$\frac{0.020\ (0,51)}{0.012\ (0,31)}$

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

$\frac{0.012\ (0,30)}{0.004\ (0,10)}$

$\frac{0.013\ (0,33)}{0.008\ (0,20)}$

⌒ | 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

$\frac{0.050\ (1,27)}{0.016\ (0,40)}$

4040000−4/G 01/11

NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS−013 variation AC.

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0,65   0,30
              0,19   ⊕ | 0,10 Ⓜ

20   11

4,50   6,60
4,30   6,20

Ⓓ

1   10

6,60
6,40

Ⓒ

0,15 NOM

Gage Plane

0°−8°   0,25

                               0,75
                               0,50

1,20 MAX   0,15
              0,05

Seating Plane

⌒ | 0,10

4040064−5/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        Ⓒ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed 0,15 each side.
        Ⓓ Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
        E. Falls within JEDEC MO−153

PW (R–PDSO–G20)   PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

20x0,25

1,55

5,6

5,6

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note F)

0,3

1,6

Pad Geometry

0,07
All Around

4211284–5/F   12/12

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Publication IPC–7351 is recommended for alternate design.
          D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
               contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
          E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS
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DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A.   All linear dimensions are in millimeters.
        B.   This drawing is subject to change without notice.
        C.   Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D.   Falls within JEDEC MO-150

NS (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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