

# HCPL-0720/7720/0721/7721

## 40 ns Propagation Delay, CMOS Optocoupler



### Data Sheet

#### Description

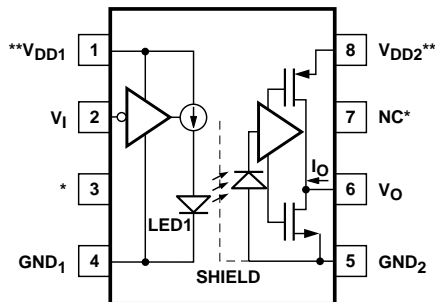
Available in either an 8-pin DIP or SO-8 package style respectively, the HCPL-772X or HCPL-072X optocouplers utilize the latest CMOS IC technology to achieve outstanding performance with very low power consumption. The HCPL-772X/072X require only two bypass capacitors for complete CMOS compatibility.

Basic building blocks of the HCPL-772X/072X are a CMOS LED driver IC, a high speed LED and a CMOS detector IC. A CMOS logic input signal controls the LED driver IC which supplies current to the LED. The detector IC incorporates an integrated photodiode, a high-speed transimpedance amplifier, and a voltage comparator with an output driver.

#### Features

- +5 V CMOS compatibility
- 20 ns maximum prop. delay skew
- High speed: 25 MBd
- 40 ns max. prop. delay
- 10 kV/ $\mu$ s minimum common mode rejection
- -40 to 85°C temperature range
- Safety and regulatory approvals
  - UL recognized
    - 3750 Vrms for 1 min. per UL 1577
    - 5000 Vrms for 1 min. per UL 1577 (for option 020)
  - CSA component acceptance notice #5
  - IEC/EN/DIN EN 60747-5-2
    - $V_{IORM} = 630 V_{peak}$  for HCPL-772X option 060
    - $V_{IORM} = 560 V_{peak}$  for HCPL-072X option 060

#### Functional Diagram



\* Pin 3 is the anode of the internal LED and must be left unconnected for guaranteed data sheet performance. Pin 7 is not connected internally.

\*\* A 0.1  $\mu$ F bypass capacitor must be connected between pins 1 and 4, and 5 and 8.

#### Applications

- Digital fieldbus isolation: CC-Link, DeviceNet, Profibus, SDS
- AC plasma display panel level shifting
- Multiplexed data transmission
- Computer peripheral interface
- Microprocessor system interface

TRUTH TABLE  
(POSITIVE LOGIC)

$V_I$ , INPUT	LED1	$V_O$ , OUTPUT
H	OFF	H
L	ON	L

**CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

## Selection Guide

8-Pin DIP (300 Mil)	Small Outline SO-8	Data Rate	PWD
HCPL-7721	HCPL-0721	25 MB	6 ns
HCPL-7720	HCPL-0720	25 MB	8 ns

## Ordering Information

Specify Part Number followed by Option Number (if desired)

Example

HCPL-7720#XXXXX

_____	020 = 5000 Vrms/1 minute UL Rating Option*
_____	060 = IEC/EN/DIN EN 60747-5-2 Option
_____	300 = Gull Wing Surface Mount Option (HCPL-7720 only)
_____	500 = Tape and Reel Packaging Option
_____	XXXXE = Lead Free Option

No Option and Option 300 contain 50 units (HCPL-772X), 100 units (HCPL-072X) per tube.

Option 500 contain 1000 units (HCPL-772X), 1500 units (HCPL-072X) per reel.

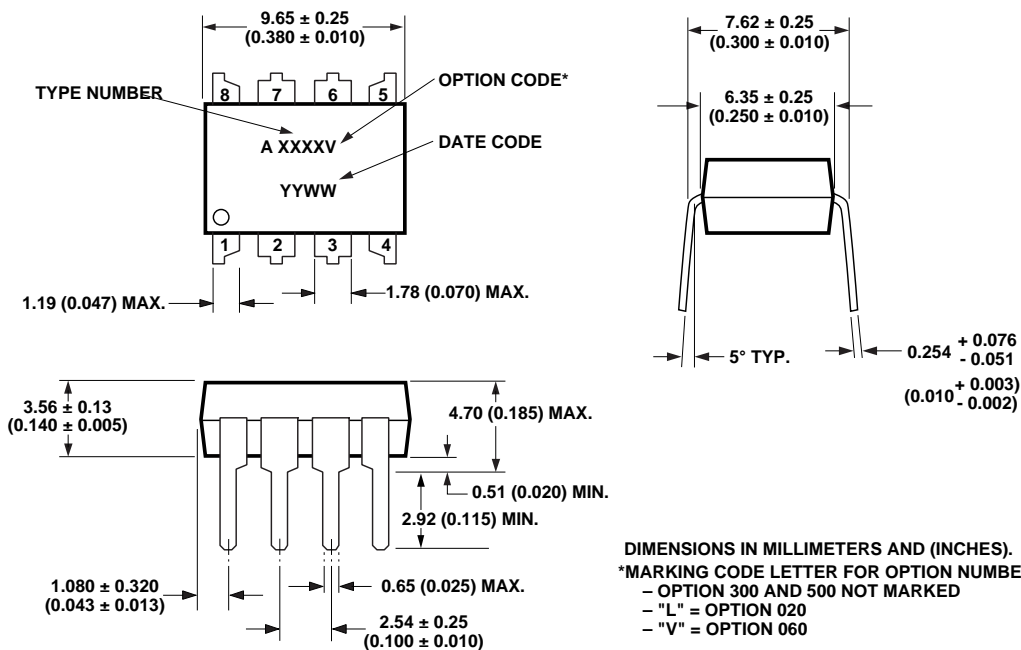
Option data sheets available. Contact Avago sales representative or authorized distributor.

\*Combination of Option 020 and Option 060 is not available.

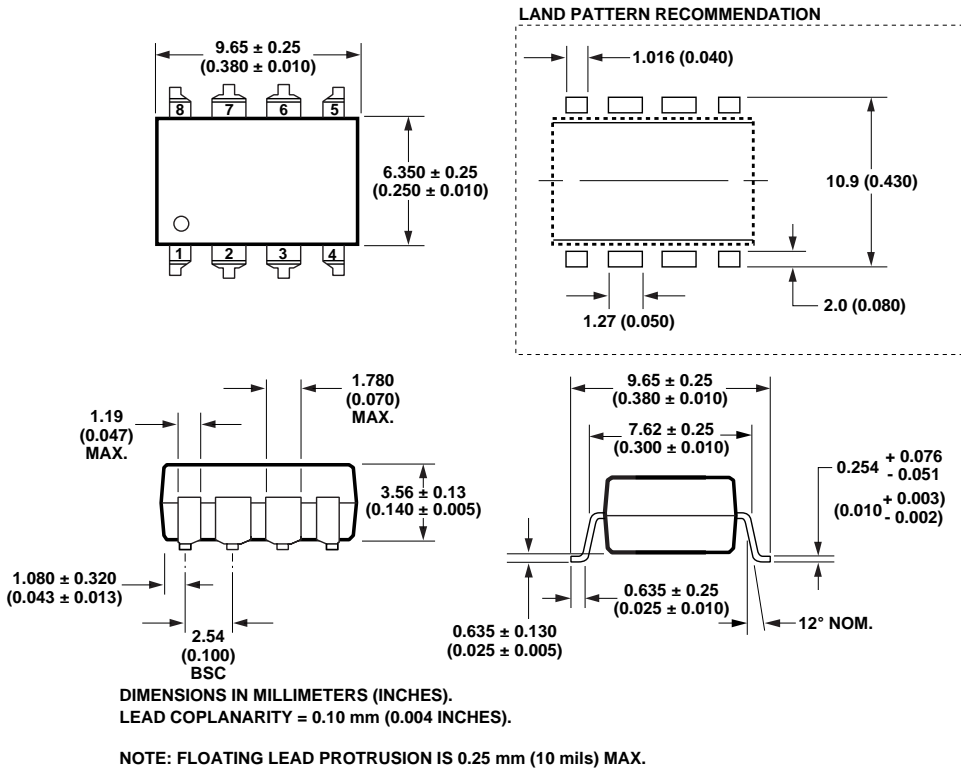
Remarks: The notation “#” is used for existing products, while (new) products launched since 15th July 2001 and lead free option will use “-”

## Package Outline Drawing

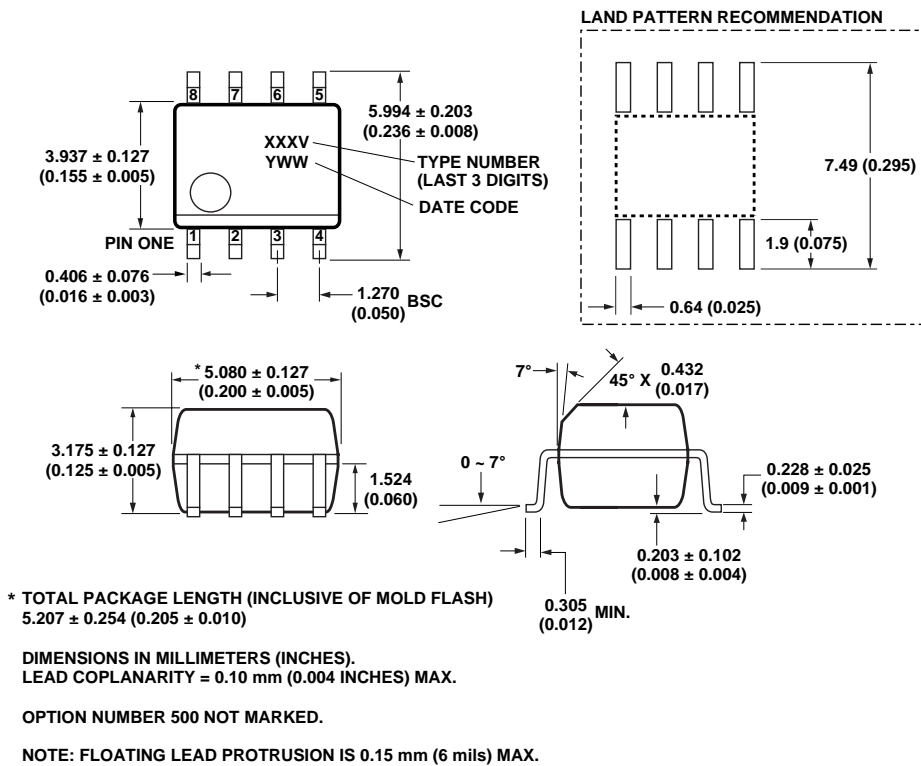
### HCPL-772X 8-Pin DIP Package



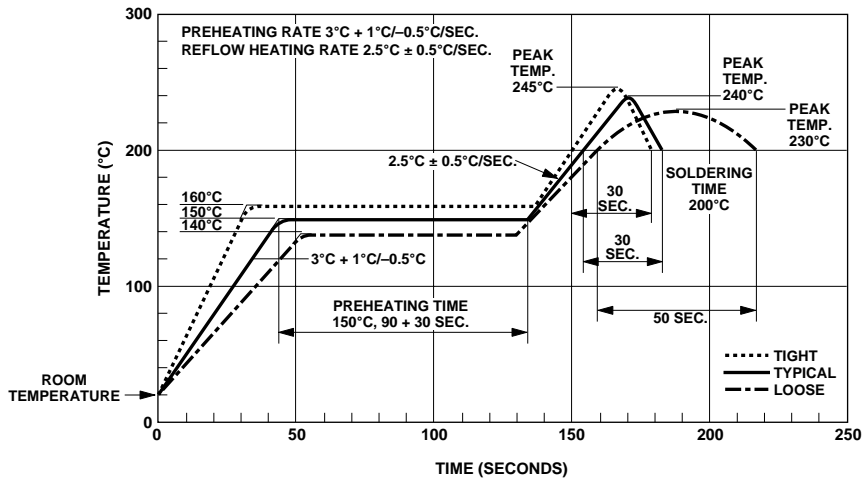
Package Outline Drawing  
 HCPL-772X Package with Gull Wing Surface Mount Option 300



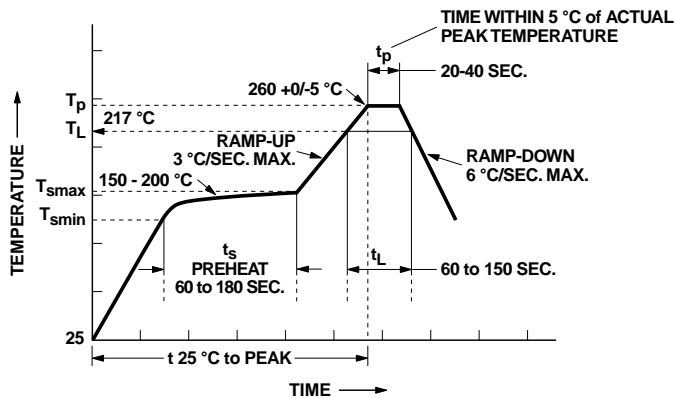
Package Outline Drawing  
 HCPL-072X Outline Drawing (Small Outline SO-8 Package)



## Solder Reflow Thermal Profile



## Pb-Free IR Profile



### NOTES:

1. THE TIME FROM 25 °C TO PEAK TEMPERATURE = 8 MINUTES MAX.  
 $T_{smax} = 200^{\circ}\text{C}$ ,  $T_{smin} = 150^{\circ}\text{C}$
2. USE OF NON-CHLORINE-ACTIVATED FLUXES IS HIGHLY RECOMMENDED.

## Regulatory Information

The HCPL-772X/072X have been approved by the following organizations:

### UL

Recognized under UL 1577, component recognition program, File E55361.

### CSA

Approved under CSA Component Acceptance Notice #5, File CA88324.

### IEC/EN/DIN EN 60747-5-2

Approved under:  
 IEC 60747-5-2:1997 + A1:2002  
 EN 60747-5-2:2001 + A1:2002  
 DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01.  
 (Option 060 only)

## Insulation and Safety Related Specifications

Parameter	Symbol	Value		Units	Conditions
		772X	072X		
Minimum External Air Gap (Clearance)	L(I01)	7.1	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(I02)	7.4	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Insulation thickness between emitter and detector; also known as distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	≥175	≥175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

All Avago data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit

board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered.

There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

## IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics (Option 060)

Description	Symbol	HCPL-772X Option 060	HCPL-072X Option 060	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage $\leq 150$ V rms for rated mains voltage $\leq 300$ V rms for rated mains voltage $\leq 450$ V rms		I-IV I-IV I-III	I-IV I-III	
Climatic Classification		55/85/21	55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	2	
Maximum Working Insulation Voltage	$V_{IORM}$	630	560	V peak
Input to Output Test Voltage, Method bt $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1$ sec, Partial Discharge $< 5$ pC	$V_{PR}$	1181	1050	V peak
Input to Output Test Voltage, Method at $V_{IORM} \times 1.5 = V_{PR}$ , Type and Sample Test, $t_m = 60$ sec, Partial Discharge $< 5$ pC	$V_{PR}$	945	840	V peak
Highest Allowable Overvoltage† (Transient Overvoltage, $t_{ini} = 10$ sec)	$V_{IOTM}$	6000	4000	V peak
<b>Safety Limiting Values</b> (Maximum values allowed in the event of a failure, also see Thermal Derating curve, Figure 11.)				
Case Temperature	$T_S$	175	150	°C
Input Current	$I_{S,INPUT}$	230	150	mA
Output Power	$P_{S,OUTPUT}$	600	600	mW
Insulation Resistance at $T_S$ , $V_{I0} = 500$ V	$R_{I0}$	$\geq 10^9$	$\geq 10^9$	$\Omega$

† Refer to the front of the optocoupler section of the Isolation and Control Component Designer's Catalog, under Product Safety Regulations section IEC/EN/DIN EN 60747-5-2, for a detailed description.

Note: These optocouplers are suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

Note: The surface mount classification is Class A in accordance with CECC 00802.

### Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Figure
Storage Temperature	$T_S$	-55	125	°C	
Ambient Operating Temperature <sup>[1]</sup>	$T_A$	-40	+85	°C	
Supply Voltages	$V_{DD1}, V_{DD2}$	0	6.0	Volts	
Input Voltage	$V_I$	-0.5	$V_{DD1} + 0.5$	Volts	
Output Voltage	$V_O$	-0.5	$V_{DD2} + 0.5$	Volts	
Average Output Current	$I_O$		10	mA	
Lead Solder Temperature		260°C for 10 sec., 1.6 mm below seating plane			
Solder Reflow Temperature Profile		See Solder Reflow Temperature Profile Section			

### Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Figure
Ambient Operating Temperature	$T_A$	-40	+85	°C	
Supply Voltages	$V_{DD1}, V_{DD2}$	4.5	5.5	V	
Logic High Input Voltage	$V_{IH}$	2.0	$V_{DD1}$	V	1, 2
Logic Low Input Voltage	$V_{IL}$	0.0	0.8	V	
Input Signal Rise and Fall Times	$t_r, t_f$		1.0	ms	

## Electrical Specifications

Test conditions that are not specified can be anywhere within the recommended operating range.

All typical specifications are at  $T_A = +25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = +5\text{ V}$ .

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
<b>DC Specifications</b>								
Logic Low Input Supply Current	$I_{DD1L}$		6.0	10.0	mA	$V_I = 0\text{ V}$		2
Logic High Input Supply Current	$I_{DD1H}$		1.5	3.0	mA	$V_I = V_{DD1}$		
Output Supply Current	$I_{DD2L}$		5.5	9.0	mA			
	$I_{DD2H}$		7.0	9.0				
Input Current	$I_I$	-10		10	$\mu\text{A}$			
Logic High Output Voltage	$V_{OH}$	4.4	5.0		V	$I_O = -20\ \mu\text{A}$ , $V_I = V_{IH}$	1, 2	
		4.0	4.8			$I_O = -4\ \text{mA}$ , $V_I = V_{IH}$		
Logic Low Output Voltage	$V_{OL}$		0	0.1	V	$I_O = 20\ \mu\text{A}$ , $V_I = V_{IL}$		
				0.1	V	$I_O = 400\ \mu\text{A}$ , $V_I = V_{IL}$		
			0.5	1.0		$I_O = 4\ \text{mA}$ , $V_I = V_{IL}$		
<b>Switching Specifications</b>								
Propagation Delay Time to Logic Low Output	$t_{PHL}$		20	40	ns	$C_L = 15\ \text{pF}$ CMOS Signal Levels	3, 6	3
Propagation Delay Time to Logic High Output	$t_{PLH}$		23	40				
Pulse Width	PW	40						
Data Rate				25	MBd			
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD	7721/0721	3	6	ns		7	4
		7720/0720	3	8	ns			
Propagation Delay Skew	$t_{PSK}$			20				5
Output Rise Time (10 - 90%)	$t_R$		9		ns			
Output Fall Time (90 - 10%)	$t_F$		8		ns			
Common Mode Transient Immunity at Logic High Output	$ CM_H $	10	20		kV/ $\mu\text{s}$	$V_I = V_{DD1}$ , $V_O > 0.8 V_{DD1}$ , $V_{CM} = 1000\ \text{V}$		6
Common Mode Transient Immunity at Logic Low Output	$ CM_L $	10	20			$V_I = 0\ \text{V}$ , $V_O > 0.8\ \text{V}$ , $V_{CM} = 1000\ \text{V}$		
Input Dynamic Power Dissipation Capacitance	$C_{PD1}$		60		pF			7
Output Dynamic Power Dissipation Capacitance	$C_{PD2}$		10					

## Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage	$V_{ISO}$	3750			Vrms	RH ≤ 50%, t = 1 min., T <sub>A</sub> = 25°C	8, 9, 10	
Resistance (Input-Output)	R <sub>I-O</sub>		10 <sup>12</sup>		Ω	V <sub>I-O</sub> = 500 Vdc		8
Capacitance (Input-Output)	C <sub>I-O</sub>		0.6		pF	f = 1 MHz		
Input Capacitance	C <sub>I</sub>		3.0					11
Input IC Junction-to-Case Thermal Resistance	θ <sub>Jci</sub>		145		°C/W	Thermocouple located at center underside of package		
Output IC Junction-to-Case Thermal Resistance	θ <sub>Jco</sub>		140					
Package Power Dissipation	P <sub>PD</sub>			150	mW			

### Notes:

- Absolute Maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee functionality.
- The LED is ON when V<sub>I</sub> is low and OFF when V<sub>I</sub> is high.
- t<sub>PHL</sub> propagation delay is measured from the 50% level on the falling edge of the V<sub>I</sub> signal to the 50% level of the falling edge of the V<sub>O</sub> signal. t<sub>PLH</sub> propagation delay is measured from the 50% level on the rising edge of the V<sub>I</sub> signal to the 50% level of the rising edge of the V<sub>O</sub> signal.
- PWD is defined as |t<sub>PHL</sub> - t<sub>PLH</sub>|. %PWD (percent pulse width distortion) is equal to the PWD divided by pulse width.
- t<sub>PSK</sub> is equal to the magnitude of the worst case difference in t<sub>PHL</sub> and/or t<sub>PLH</sub> that will be seen between units at any given temperature within the recommended operating conditions.
- CM<sub>H</sub> is the maximum common mode voltage slew rate that can be sustained while maintaining V<sub>O</sub> > 0.8 V<sub>DD2</sub>. CM<sub>L</sub> is the maximum common mode voltage slew rate that can be sustained while maintaining V<sub>O</sub> < 0.8 V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
- Unloaded dynamic power dissipation is calculated as follows: C<sub>PD</sub> \* V<sub>DD2</sub> \* f + I<sub>DD</sub> \* V<sub>DD</sub>, where f is switching frequency in MHz.
- Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
- In accordance with UL1577, each HCPL-072X is proof tested by applying an insulation test voltage ≥ 4500 V<sub>RMS</sub> for 1 second (leakage detection current limit, I<sub>I-O</sub> ≤ 5 μA). Each HCPL-772X is proof tested by applying an insulation test voltage ≥ 4500 Vrms for 1 second (leakage detection current limit, I<sub>I-O</sub> ≤ 5 μA).
- The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to your equipment level safety specification or Avago Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."
- C<sub>I</sub> is the capacitance measured at pin 2 (V<sub>I</sub>).

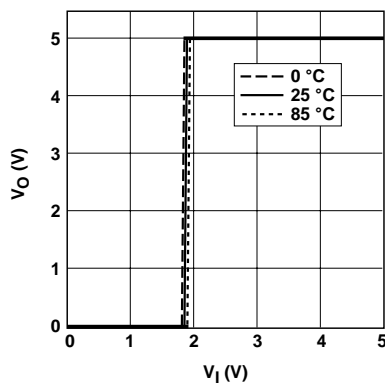


Figure 1. Typical output voltage vs. input voltage.

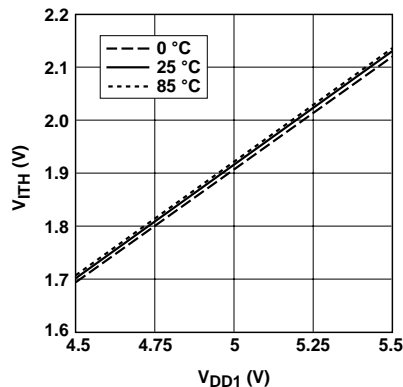


Figure 2. Typical input voltage switching threshold vs. input supply voltage.

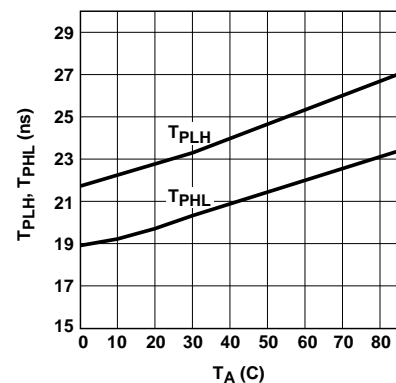


Figure 3. Typical propagation delays vs. temperature.



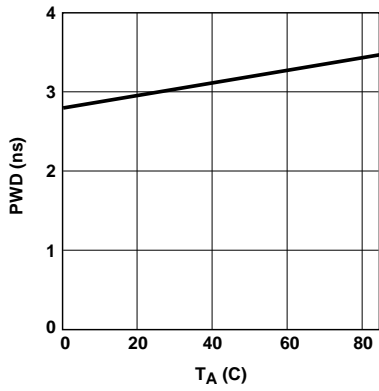


Figure 4. Typical pulse width distortion vs. temperature.

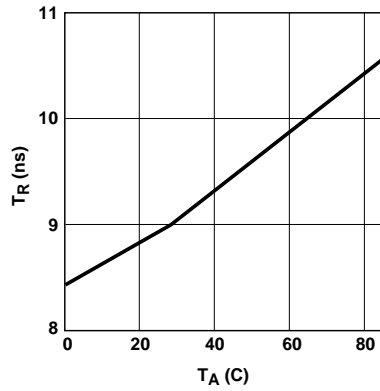


Figure 5. Typical rise time vs. temperature.

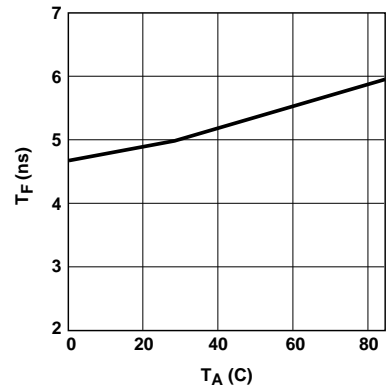


Figure 6. Typical fall time vs. temperature.

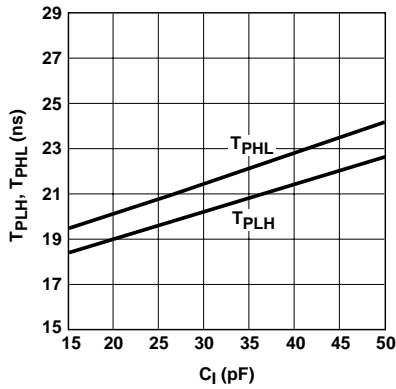


Figure 7. Typical propagation delays vs. output load capacitance.

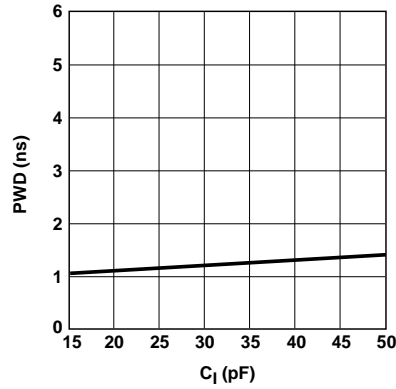


Figure 8. Typical pulse width distortion vs. output load capacitance.

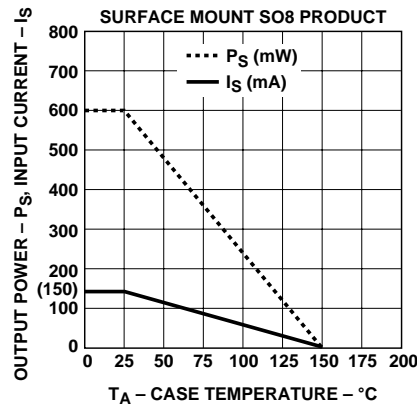
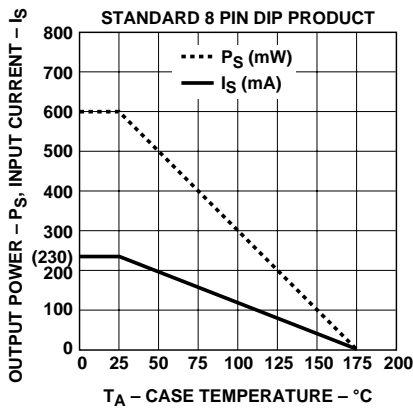


Figure 9. Thermal derating curve, dependence of safety limiting value with case temperature per IEC/EN/DIN EN 60747-5-2.

**Application Information**  
**Bypassing and PC Board Layout**

The HCPL-772X/072X optocouplers are extremely easy to use. No external interface circuitry is required because the HCPL-772X/072X use high-speed CMOS IC technology allowing

CMOS logic to be connected directly to the inputs and outputs.

As shown in Figure 10, the only external components required for proper operation are two bypass capacitors. Capacitor values should be between 0.01  $\mu\text{F}$  and

0.1  $\mu\text{F}$ . For each capacitor, the total lead length between both ends of the capacitor and the power-supply pins should not exceed 20 mm. Figure 11 illustrates the recommended printed circuit board layout for the HCPL-772X/072X.

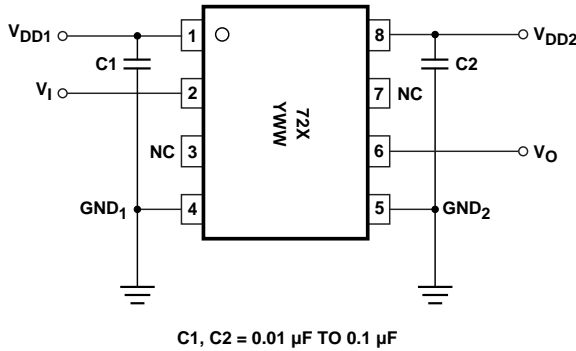


Figure 10. Recommended printed circuit board layout.

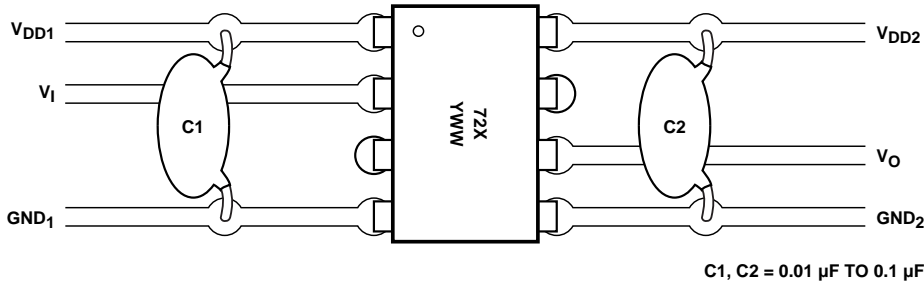


Figure 11. Recommended printed circuit board layout.

**Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew**

Propagation Delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay

from low to high ( $t_{PLH}$ ) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay

from high to low ( $t_{PHL}$ ) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low. See Figure 12.

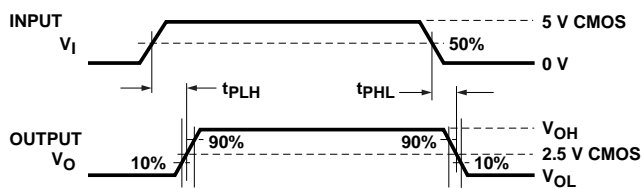


Figure 12.

Pulse-width distortion (PWD) is the difference between  $t_{\text{PHL}}$  and  $t_{\text{PLH}}$  and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20 - 30% of the minimum pulse width is tolerable.

Propagation delay skew,  $t_{\text{PSK}}$ , is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays

will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delay is large enough it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either  $t_{\text{PLH}}$  or  $t_{\text{PHL}}$ , for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 13, if the inputs of a group

of optocouplers are switched either ON or OFF at the same time,  $t_{\text{PSK}}$  is the difference between the shortest propagation delay, either  $t_{\text{PLH}}$  or  $t_{\text{PHL}}$ , and the longest propagation delay, either  $t_{\text{PLH}}$  or  $t_{\text{PHL}}$ .

As mentioned earlier,  $t_{\text{PSK}}$  can determine the maximum parallel data transmission rate. Figure 14 is the timing diagram of a typical parallel data application with both the clock and data lines being sent through the optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. In this case the data is assumed to be clocked off of the rising edge of the clock.

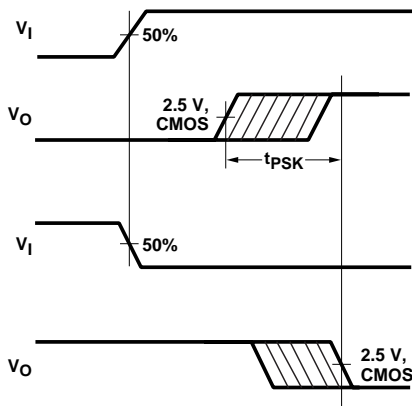


Figure 13. Propagation delay skew waveform.

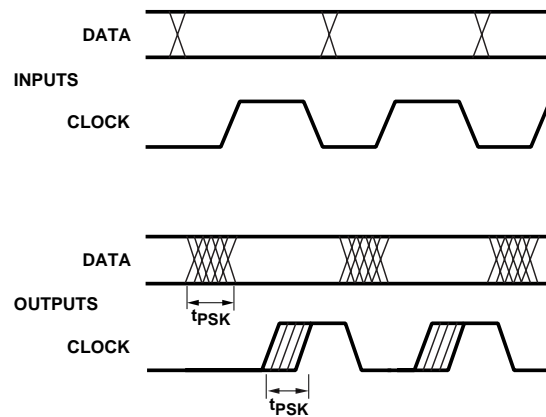


Figure 14. Parallel data transmission example.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 14 shows that there will be uncertainty in both the data and clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or

some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice  $t_{\text{PSK}}$ . A cautious design should use a slightly longer pulse width to ensure that any additional

uncertainty in the rest of the circuit does not cause a problem.

The HCPL-772X/072X optocouplers offer the advantage of guaranteed specifications for propagation delays, pulse-width distortion, and propagation delay skew over the recommended temperature and power supply ranges.

## Digital Field Bus Communication Networks

To date, despite its many drawbacks, the 4 - 20 mA analog current loop has been the most widely accepted standard for implementing process control

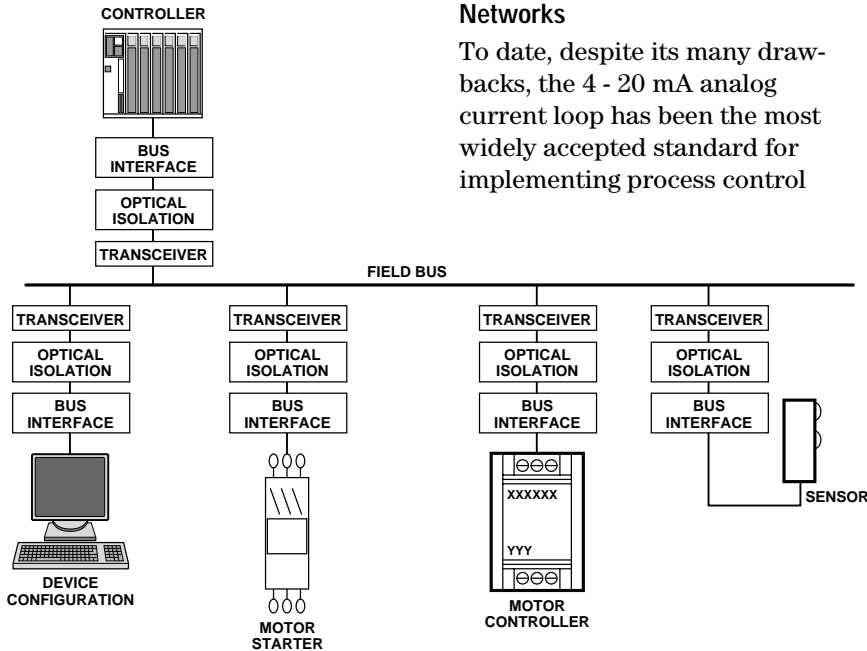


Figure 15. Typical field bus communication physical model.

systems. In today's manufacturing environment, however, automated systems are expected to help manage the process, not merely monitor it. With the advent of digital field bus communication networks such as CC-Link, DeviceNet, PROFIBUS, and Smart Distributed Systems (SDS), gone are the days of constrained information. Controllers can now receive multiple readings from field devices (sensors, actuators, etc.) in addition to diagnostic information.

The physical model for each of these digital field bus communication networks is very similar as shown in Figure 15. Each includes one or more buses, an interface unit, optical isolation, transceiver, and sensing and/or actuating devices.

## Optical Isolation for Field Bus Networks

To recognize the full benefits of these networks, each recommends providing galvanic isolation using Avago optocouplers. Since network communication is bi-directional (involving receiving

data from and transmitting data onto the network), two Avago optocouplers are needed. By providing galvanic isolation, data integrity is retained via noise reduction and the elimination of false signals. In addition, the network receives maximum

protection from power system faults and ground loops.

Within an **isolated node**, such as the DeviceNet Node shown in Figure 16, some of the node's components are referenced to a ground other than V- of the network. These components could include such things as devices with serial ports, parallel ports, RS232 and RS485 type ports. As shown in Figure 16, power from the network is used only for the transceiver and input (network) side of the optocouplers.

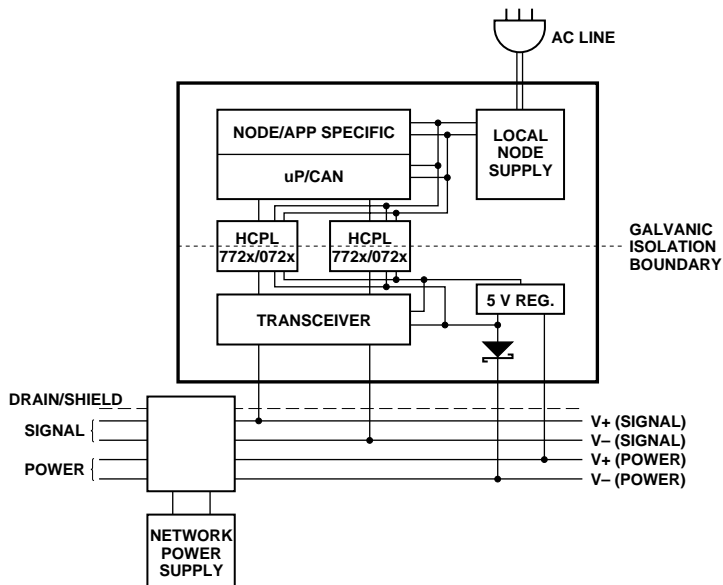


Figure 16. Typical DeviceNet Node.

### Implementing CC-Link with the HCPL-772X/072X

CC-Link (Control and Communication Link) is developed to merge control and information in the low-level network (field network) by PCs, thereby making the multivendor environment a reality. It has data control and message-exchange function, as well as bit control function, and operates at the speed up to 10 Mbps.

### Power Supplies and Bypassing

The recommended CC-Link circuit is shown in Figure 17. Since the HCPL-772X/072X are fully compatible with CMOS logic level signals, the optocoupler is connected directly to the transceiver. Two bypass capacitors (with values between 0.01  $\mu\text{F}$  and 0.1  $\mu\text{F}$ ) are required and should be located as close as

possible to the input and output power supply pins of the HCPL-772X/072X. For each capacitor, the total lead length between both ends of capacitor and the power supply pins should not exceed 20 mm. The bypass capacitors are required because of the high speed digital nature of the signals inside the optocoupler.

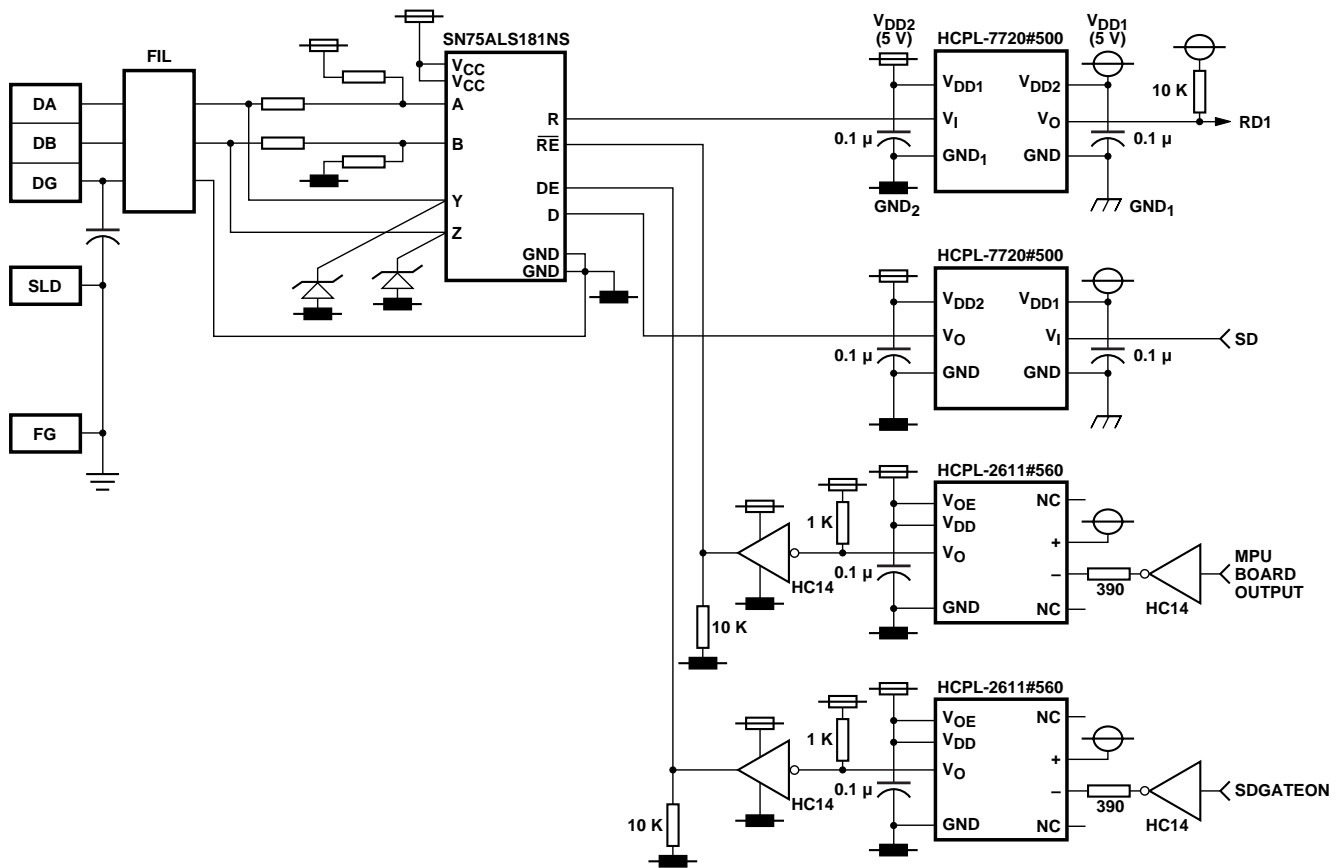


Figure 17. Recommended CC-Link application circuit.

### Implementing DeviceNet and SDS with the HCPL-772X/072X

With transmission rates up to 1 Mbit/s, both DeviceNet and SDS are based upon the same broadcast-oriented, communica-

tions protocol – the Controller Area Network (CAN). Three types of isolated nodes are recommended for use on these networks: Isolated Node Powered by the Network (Figure 18),

Isolated Node with Transceiver Powered by the Network (Figure 19), and Isolated Node Providing Power to the Network (Figure 20).

### Isolated Node Powered by the Network

This type of node is very flexible and as can be seen in Figure 18, is regarded as “isolated” because not all of its components have the same ground reference. Yet, all components are still powered by the network. This node contains two regulators: one is isolated and powers the CAN controller, node-specific application and isolated (node) side of the two optocouplers while the other is non-isolated. The non-isolated regulator supplies the transceiver and the non-isolated (network) half of the two optocouplers.

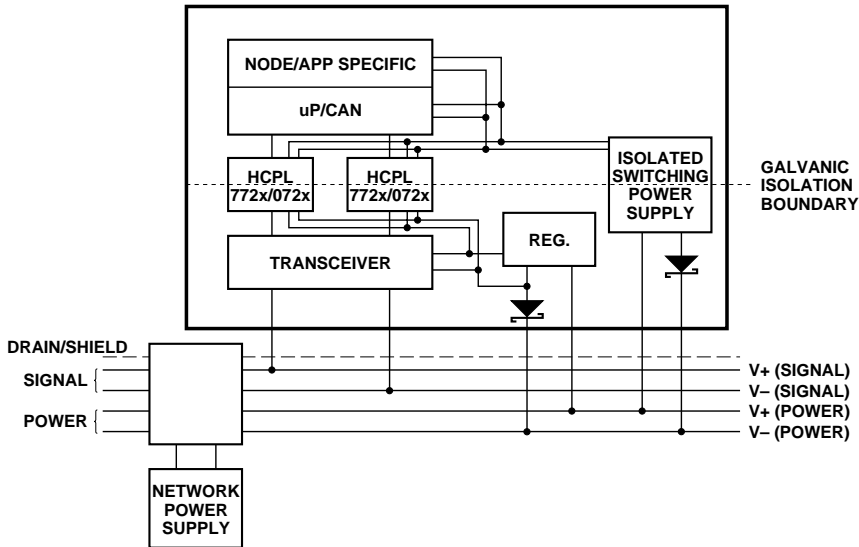


Figure 18. Isolated node powered by the network.

### Isolated Node with Transceiver Powered by the Network

Figure 19 shows a node powered by both the network and another source. In this case, the transceiver and isolated (network) side of the two optocouplers are powered by the network. The rest of the node is powered by the AC line which is very beneficial when an application requires a

significant amount of power. This method is also desirable as it does not heavily load the network.

More importantly, the unique “dual-inverting” design of the HCPL-772X/072X ensure the network will not “lock-up” if either AC line power to the node is lost or the node powered-off. Specifically, when input power

( $V_{DD1}$ ) to the HCPL-772X/072X located in the transmit path is eliminated, a RECESSIVE bus state is ensured as the HCPL-772X/072X output voltage ( $V_O$ ) go HIGH.

### \*Bus V+ Sensing

It is suggested that the Bus V+ sense block shown in Figure 19 be implemented. A locally powered

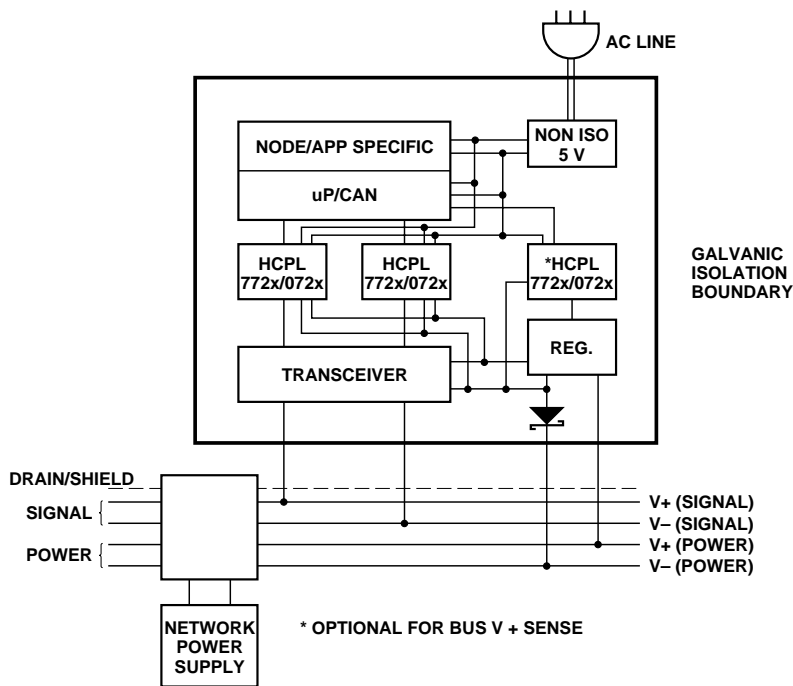


Figure 19. Isolated node with transceiver powered by the network.

node with an un-powered isolated Physical Layer will accumulate errors and become bus-off if it attempts to transmit. The Bus V+ sense signal would be used to change the BOI attribute of the DeviceNet Object to the “auto-reset” (01) value. Refer to Volume 1, Section 5.5.3. This would cause the node to continually reset until bus power was detected. Once power was detected, the BOI attribute would be returned to the “hold in bus-off” (00) value. The BOI attribute should not be left in the “auto-reset” (01) value since this defeats the jabber protection capability of the CAN error confinement. Any inexpensive low frequency optical isolator can be used to implement this feature.

### Isolated Node Providing Power to the Network

Figure 20 shows a node providing power to the network. The AC line powers a regulator which

provides five (5) volts locally. The AC line also powers a 24 volt isolated supply, which powers the network, and another five-volt regulator, which, in turn, powers

the transceiver and isolated (network) side of the two optocouplers. This method is recommended when there are a limited number of devices on the network that don't require much power, thus eliminating the need for separate power supplies.

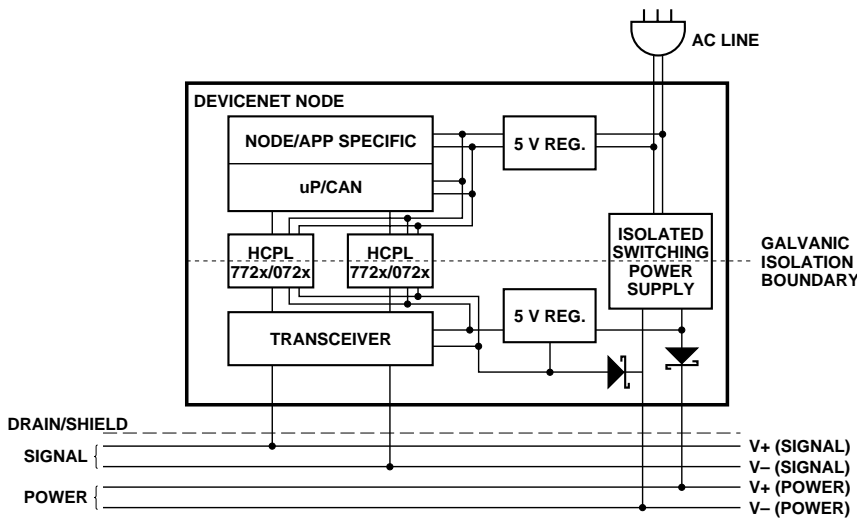


Figure 20. Isolated node providing power to the network.

More importantly, the unique “dual-inverting” design of the HCPL-772X/072X ensure the network will not “lock-up” if either AC line power to the node is lost or the node powered-off. Specifically, when input power ( $V_{DD1}$ ) to the HCPL-772X/072X located in the transmit path is eliminated, a RECESSIVE bus state is ensured as the HCPL-772X/072X output voltage ( $V_O$ ) go HIGH.

### Power Supplies and Bypassing

The recommended DeviceNet application circuit is shown in Figure 21. Since the HCPL-772X/072X are fully compatible with CMOS logic level signals, the optocoupler is connected directly

to the CAN transceiver. Two bypass capacitors (with values between 0.01 and 0.1  $\mu\text{F}$ ) are required and should be located as close as possible to the input and output power-supply pins of the HCPL-772X/072X. For each

capacitor, the total lead length between both ends of the capacitor and the power supply pins should not exceed 20 mm. The bypass capacitors are required because of the high-speed digital nature of the signals inside the optocoupler.

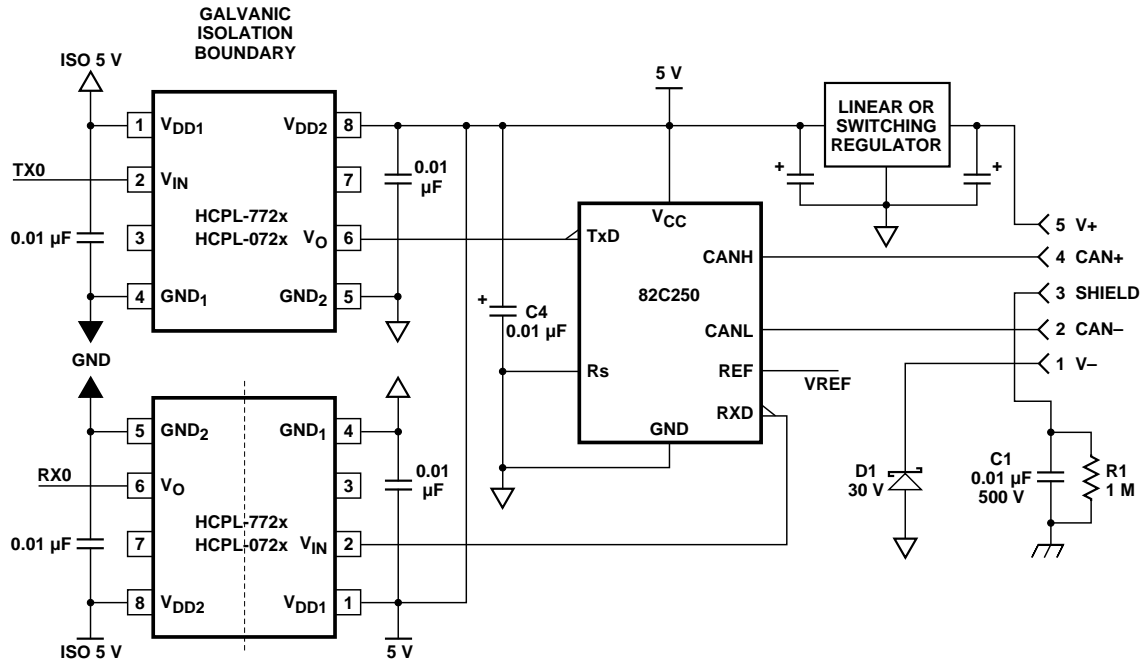


Figure 21. Recommended DeviceNet application circuit.

### Implementing PROFIBUS with the HCPL-772X/072X

An acronym for Process Fieldbus, PROFIBUS is essentially a twisted-pair serial link very similar to RS-485 capable of achieving high-speed communication up to 12 MBd. As shown in Figure 22, a PROFIBUS Controller (PBC) establishes the connection of a field automation unit (control or central processing station) or a field device to the transmission medium. The PBC consists of the line transceiver, optical isolation, frame character transmitter/receiver (UART), and the FDL/APP processor with the interface to the PROFIBUS user.

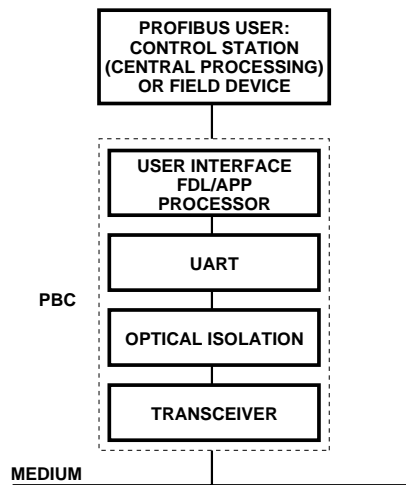


Figure 22. PROFIBUS Controller (PBC).



### Power Supplies and Bypassing

The recommended PROFIBUS application circuit is shown in Figure 23. Since the HCPL-772X/072X are fully compatible with CMOS logic level signals, the optocoupler is connected directly to the transceiver. Two bypass capacitors (with values between 0.01 and 0.1  $\mu\text{F}$ ) are required and should be located as close as possible to the input and output power-supply pins of the HCPL-772X/072X. For each

capacitor, the total lead length between both ends of the capacitor and the power supply pins should not exceed 20 mm. The bypass capacitors are required because of the high-speed digital nature of the signals inside the optocoupler.

Being very similar to multi-station RS485 systems, the HCPL-061N optocoupler provides a transmit disable function which is necessary to make the bus free

after each master/slave transmission cycle. Specifically, the HCPL-061N disables the transmitter of the line driver by putting it into a high state mode. In addition, the HCPL-061N switches the RX/TX driver IC into the listen mode. The HCPL-061N offers HCMOS compatibility and the high CMR performance (1 kV/ $\mu\text{s}$  at  $V_{\text{CM}} = 1000 \text{ V}$ ) essential in industrial communication interfaces.

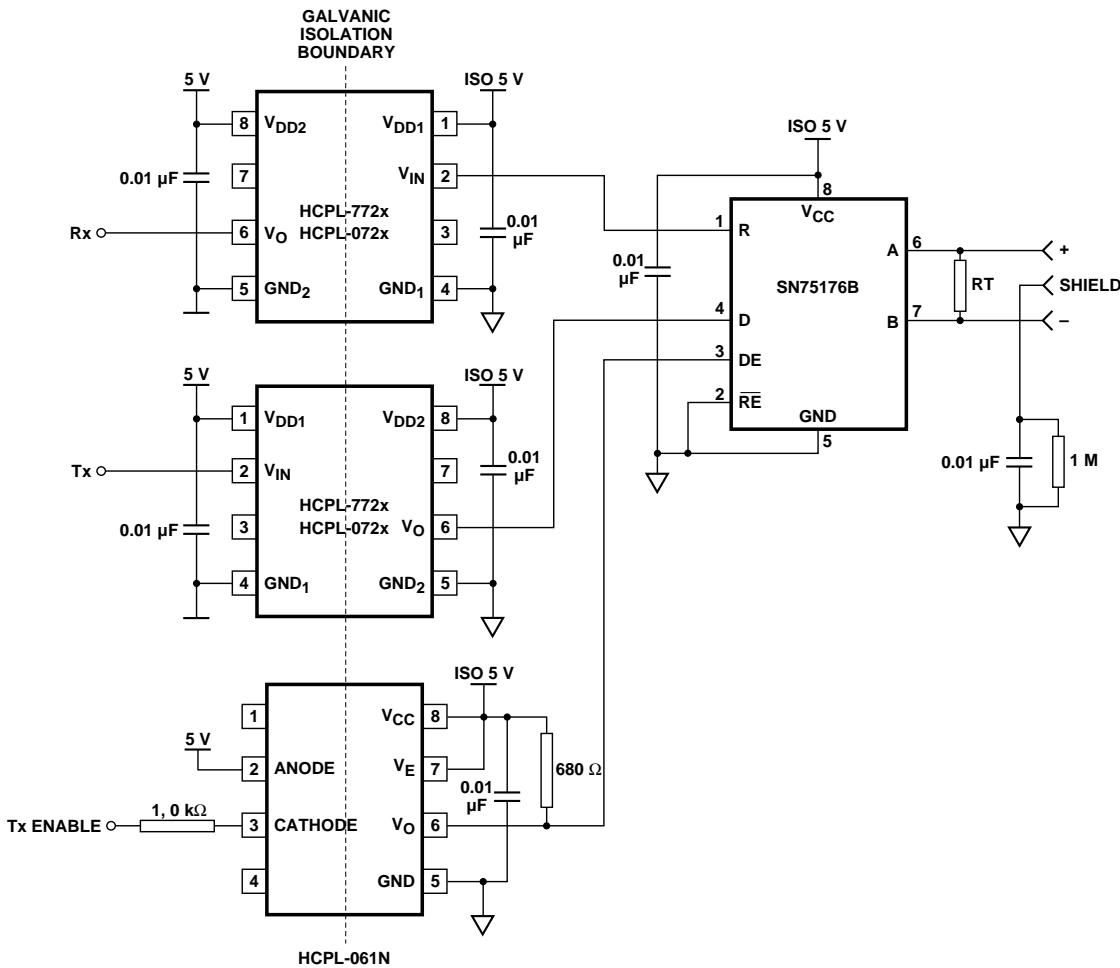


Figure 23. Recommended PROFIBUS application circuit.

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AV01-0195EN September 14, 2006

