PBLS1503Y; PBLS1503V

15 V PNP BISS loadswitch

Rev. 03 — 24 August 2009 Product data sheet

1. Product profile

1.1 General description

Low V_{CEsat} PNP transistor and NPN resistor-equipped transistor in one package.

Table 1. Product overview

Type number	Package	
	NXP	JEITA
PBLS1503Y	SOT363	SC-88
PBLS1503V	SOT666	-

1.2 Features

- Low V_{CEsat} (BISS) and resistor-equipped transistor in one package
- Low 'threshold' voltage (< 1 V) compared to MOSFET
- Low drive power required
- Space-saving solution
- Reduction of component count

1.3 Applications

- Supply line switches
- Battery charger switches
- High-side switches for LEDs, drivers and backlights
- Portable equipment

1.4 Quick reference data

Table 2. Quick reference data

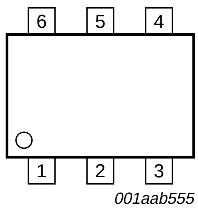
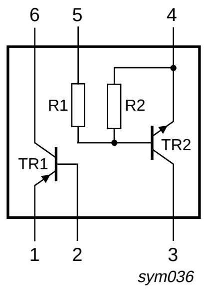
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1; PNP; low V_{CEsat} transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	–15	V
I_C	collector current (DC)		-	-	–500	mA
R_{CEsat}	equivalent on-resistance	I_C = –500 mA; I_B = –50 mA	-	300	500	mΩ
TR2; NPN; resistor-equipped transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	50	V

Table 2. Quick reference data *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_O	output current (DC)		-	-	100	mA
R1	bias resistor 1 (input)		7	10	13	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	

2. Pinning information

Table 3. Discrete pinning

Pin	Description	Simplified outline	Symbol
1	emitter TR1		
2	base TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	collector TR1		

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PBLS1503Y	SC-88	plastic surface mounted package; 6 leads	SOT363
PBLS1503V	-	plastic surface mounted package; 6 leads	SOT666

4. Marking

Table 5. Marking codes

Type number	Marking code[1]
PBLS1503Y	*C3
PBLS1503V	C3

[1] * = -: made in Hong Kong
* = p: made in Hong Kong
* = t: made in Malaysia
* = W: made in China

5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Transistor TR1: PNP						
V_{CBO}	collector-base voltage	open emitter		-	–15	V
V_{CEO}	collector-emitter voltage	open base		-	–15	V
V_{EBO}	emitter-base voltage	open collector		-	–6	V
I_C	collector current (DC)			-	–500	mA
I_{CM}	peak collector current	$t_p \leq 1$ ms; $\delta \leq 0.02$		-	–1	A
I_B	base current (DC)			-	–50	mA
I_{BM}	peak base current	$t_p \leq 1$ ms; $\delta \leq 0.02$		-	–100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	200	mW
Transistor TR2: NPN						
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V_{EBO}	emitter-base voltage	open collector		-	10	V
V_I	input voltage			-		
	positive			-	+40	V
	negative			-	–10	V
I_O	output current (DC)			-	100	mA
I_{CM}	peak collector current			-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	200	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C		-	300	mW
T_{stg}	storage temperature			–65	+150	°C
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			–65	+150	°C

[1] Device mounted on a FR4 printed-circuit board, single-sided copper, tin-plated and standard footprint.

6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air					
	SOT363		[1]	-	-	416	K/W
	SOT666		[1][2]	-	-	416	K/W

[1] Device mounted on a FR4 printed-circuit board, single-sided copper, tin-plated and standard footprint.

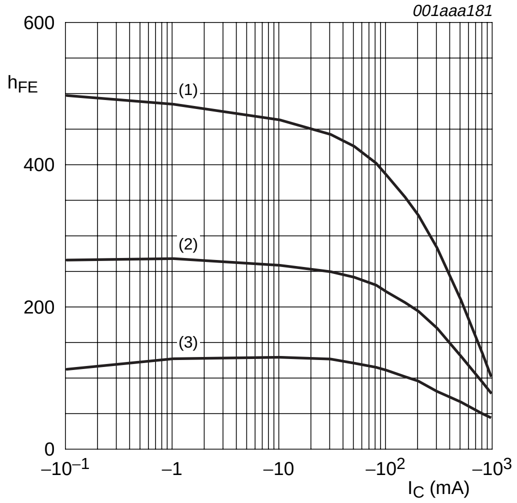
[2] Reflow soldering is the only recommended soldering method.

7. Characteristics

Table 8. Characteristics
T_{amb} = 25 °C unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Transistor TR1: PNP							
I_{CBO}	collector-base cut-off current	V_{CB} = –15 V; I_E = 0 A		-	-	–100	nA
		V_{CB} = –15 V; I_E = 0 A; T_j = 150 °C		-	-	–50	μA
I_{CES}	collector-emitter cut-off current	V_{CE} = –15 V; V_{BE} = 0 V		-	-	–100	nA
I_{EBO}	emitter-base cut-off current	V_{EB} = –5 V; I_C = 0 A		-	-	–100	nA
h_{FE}	DC current gain	V_{CE} = –2 V; I_C = –10 mA		200	-	-	
		V_{CE} = –2 V; I_C = –100 mA	[1]	150	-	-	
		V_{CE} = –2 V; I_C = –500 mA	[1]	90	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = –10 mA; I_B = –0.5 mA		-	-	–25	mV
		I_C = –200 mA; I_B = –10 mA		-	-	–150	mV
		I_C = –500 mA; I_B = –50 mA	[1]	-	-	–250	mV
R_{CEsat}	equivalent on-resistance	I_C = –500 mA; I_B = –50 mA	[1]	-	300	500	mΩ
V_{BEsat}	base-emitter saturation voltage	I_C = –500 mA; I_B = –50 mA	[1]	-	-	–1.1	V
V_{BEon}	base-emitter turn-on voltage	V_{CE} = –2 V; I_C = –100 mA	[1]	-	-	–0.9	V
f_T	transition frequency	V_{CE} = –5 V; I_C = –100 mA; f = 100 MHz		100	280	-	MHz
C_c	collector capacitance	V_{CB} = –10 V; I_E = i_e = 0 A; f = 1 MHz		-	-	10	pF
Transistor TR2: NPN							
I_{CBO}	collector-base cut-off current	V_{CB} = 50 V; I_E = 0 A		-	-	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 30 V; I_B = 0 A		-	-	1	μA
		V_{CE} = 30 V; I_B = 0 A; T_j = 150 °C		-	-	50	μA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 A		-	-	400	μA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 5 mA		30	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA		-	-	150	mV
$V_{I(off)}$	off-state input voltage	V_{CE} = 5 V; I_C = 100 μA		-	1.1	0.8	V
$V_{I(on)}$	on-state input voltage	V_{CE} = 0.3 V; I_C = 10 mA		2.5	1.8	-	V
R1	bias resistor 1 (input)			7	10	13	kΩ
R2/R1	bias resistor ratio			0.8	1	1.2	
C_c	collector capacitance	V_{CB} = 10 V; I_E = i_e = 0 A; f = 1 MHz		-	-	2.5	pF

[1] Pulse test: $t_p \leq 300$ μs; $\delta \leq 0.02$



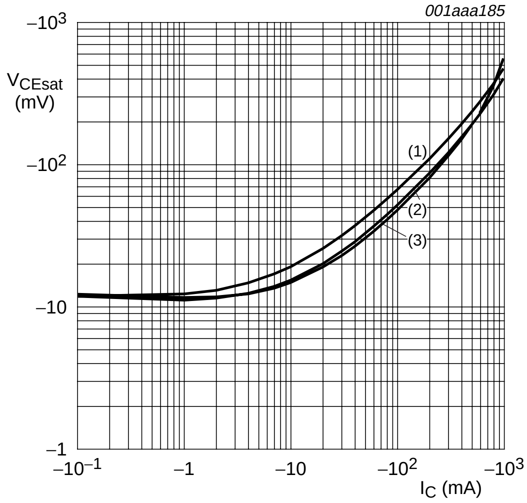
V_{CE} = −2 V

(1) T_{amb} = 150 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig 1. TR1(PNP): DC current gain as a function of collector current; typical values



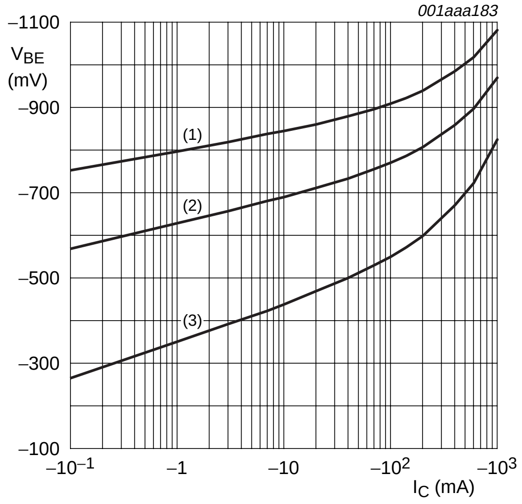
I_C/I_B = 20

(1) T_{amb} = 150 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig 2. TR1(PNP): Collector-emitter saturation voltage as a function of collector current; typical values



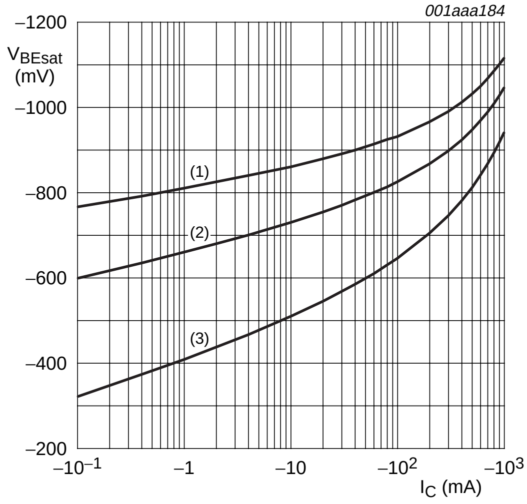
V_{CE} = −2 V

(1) T_{amb} = −55 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 150 °C

Fig 3. TR1(PNP): Base-emitter voltage as a function of collector current; typical values



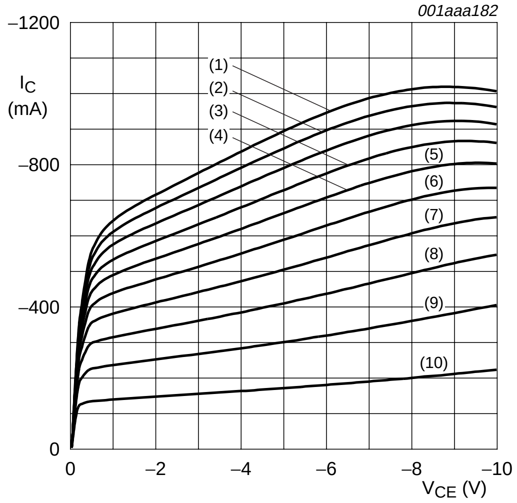
I_C/I_B = 20

(1) T_{amb} = 150 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig 4. TR1(PNP): Base-emitter saturation voltage as a function of collector current; typical values



T_{amb} = 25 °C

(1) I_B = – 7.0 mA

(2) I_B = – 6.3 mA

(3) I_B = – 5.6 mA

(4) I_B = – 4.9 mA

(5) I_B = – 4.2 mA

(6) I_B = – 3.5 mA

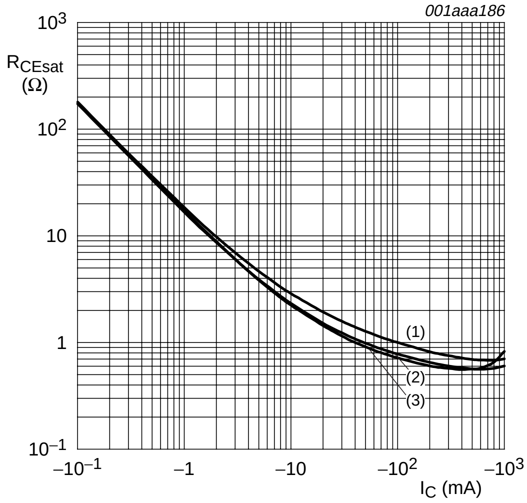
(7) I_B = – 2.8 mA

(8) I_B = – 2.1 mA

(9) I_B = – 1.4 mA

(10) I_B = – 0.7 mA

Fig 5. TR1(PNP): Collector current as a function of collector-emitter voltage; typical values



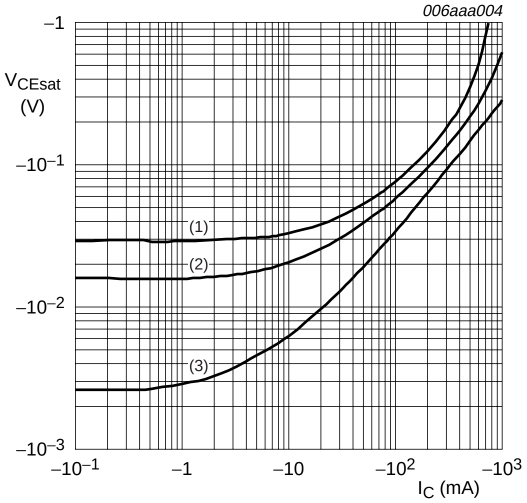
I_C/I_B = 20

(1) T_{amb} = −55 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 150 °C

Fig 6. TR1(PNP): Equivalent on-resistance as a function of collector current; typical values



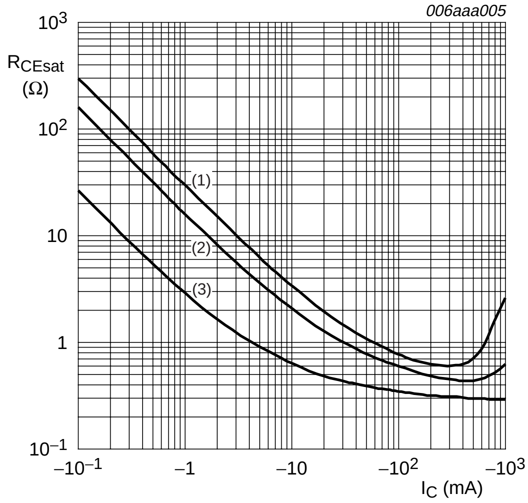
T_{amb} = 25 °C

(1) I_C/I_B = 100

(2) I_C/I_B = 50

(3) I_C/I_B = 10

Fig 7. TR1(PNP): Collector-emitter saturation voltage as a function of collector current; typical values



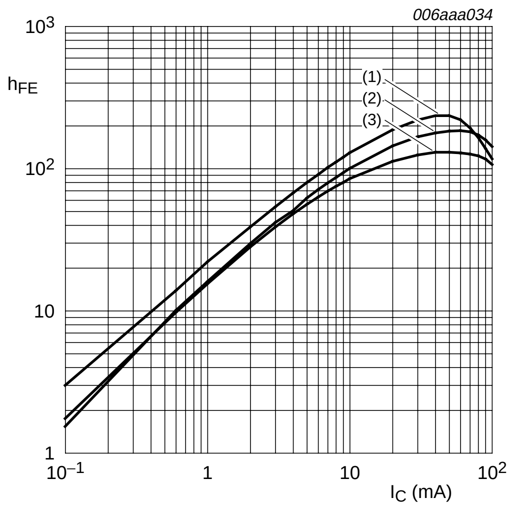
T_{amb} = 25 °C

(1) I_C/I_B = 100

(2) I_C/I_B = 50

(3) I_C/I_B = 10

Fig 8. TR1(PNP): Equivalent-on resistance as a function of collector current; typical values



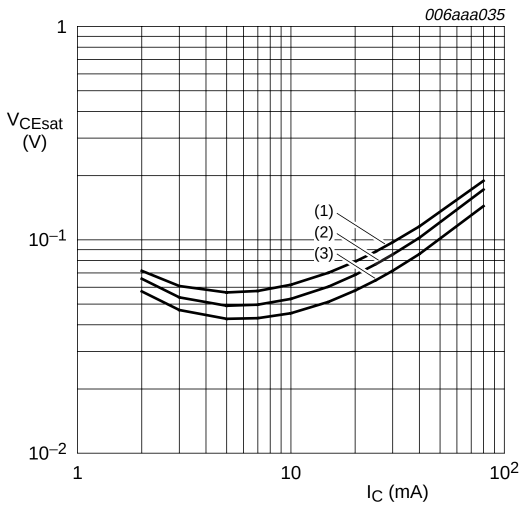
V_{CE} = 5 V

(1) T_{amb} = 150 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 9. TR2(NPN): DC current gain as a function of collector current; typical values



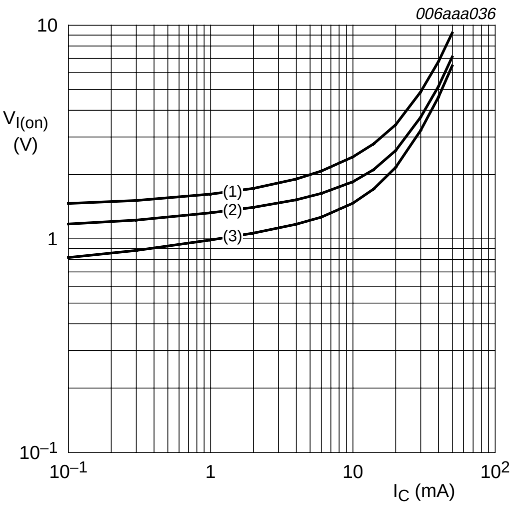
I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 10. TR2(NPN): Collector-emitter saturation voltage as a function of collector current; typical values



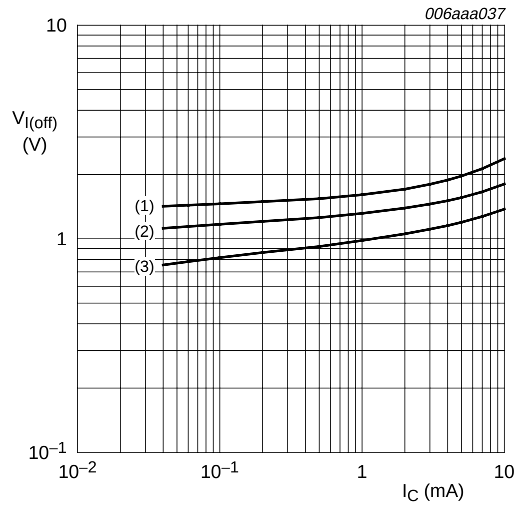
V_{CE} = 0.3 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 11. TR2(NPN): On-state input voltage as a function of collector current; typical values



V_{CE} = 5 V

(1) T_{amb} = −40 °C

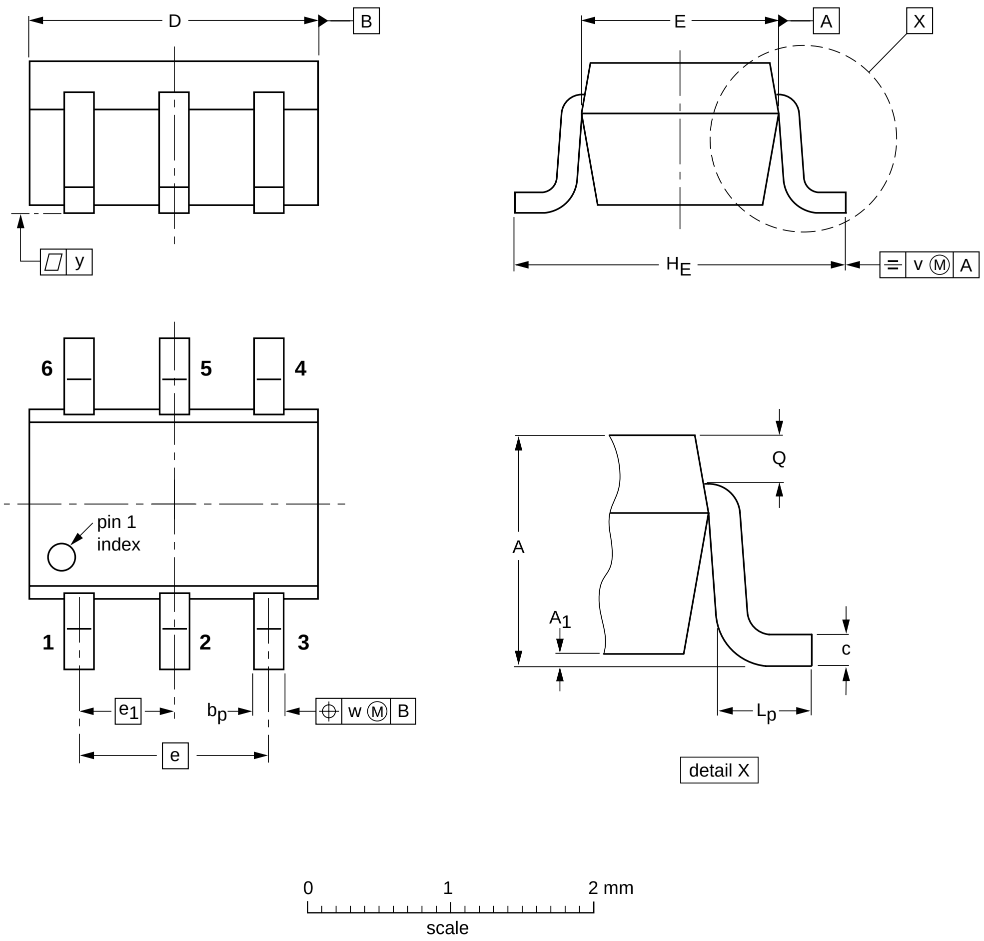
(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 12. TR2(NPN): Off-state input voltage as a function of collector current; typical values

8. Package outline

Plastic surface-mounted package; 6 leads **SOT363**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

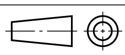
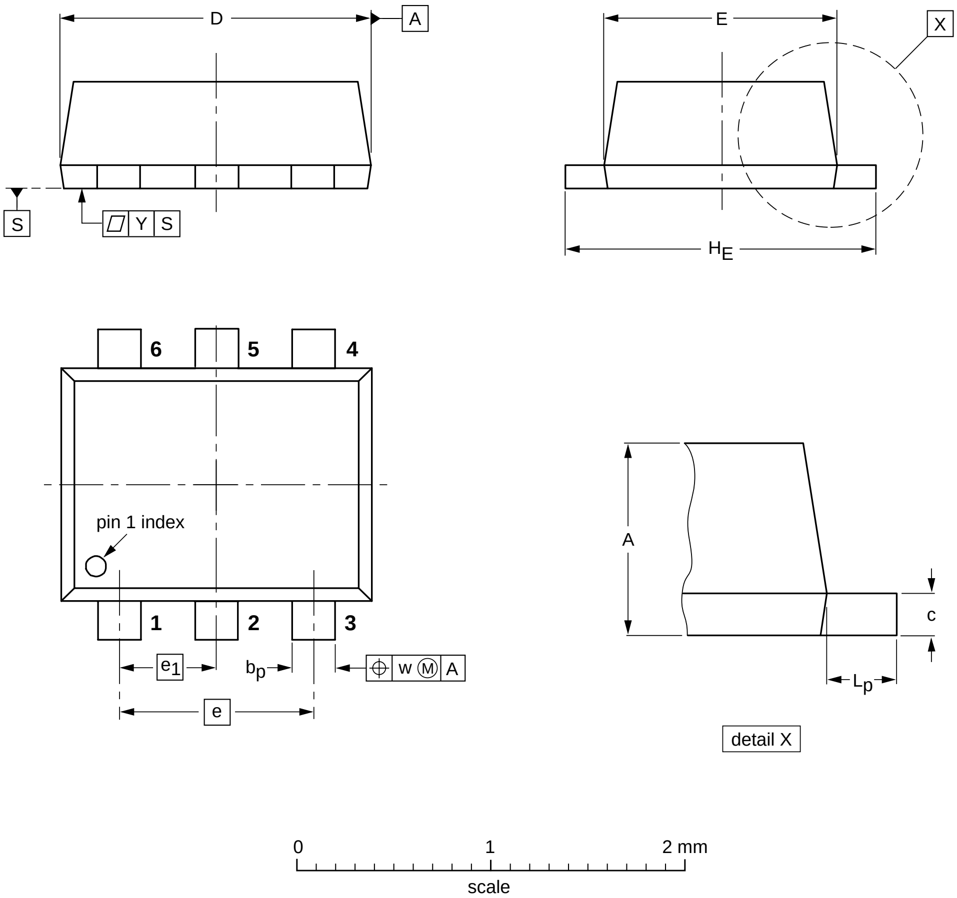
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT363			SC-88			~~04-11-08~~ 06-03-16

Fig 13. Package outline SOT363 (SC-88)

Plastic surface-mounted package; 6 leads **SOT666**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	H_E	L_p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT666						~~04-11-08~~ 06-03-16

Fig 14. Package outline SOT666

9. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description		Packing quantity		
				3000	4000	10000
PBLS1503Y	SOT363	4 mm pitch, 8 mm tape and reel; T1	[2]	-115	-	–135
		4 mm pitch, 8 mm tape and reel; T2	[3]	-125	-	-165
PBLS1503V	SOT666	4 mm pitch, 8 mm tape and reel		-	-115	-

[1] For further information and the availability of packing methods, see Section 12.

[2] T1: normal taping

[3] T2: reverse taping

10. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBLS1503Y_PBLS1503V_3	20090824	Product data sheet	-	PBLS1503Y_PBLS1503V_2
Modifications:	• This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content. • Table 3 "Discrete pinning": amended • Figure 13 "Package outline SOT363 (SC-88)": updated • Figure 14 "Package outline SOT666": updated			
PBLS1503Y_PBLS1503V_2	20041125	Product data sheet	-	PBLS1503V_1
PBLS1503V_1	20031107	Product specification	-	-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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12. Contact information

For more information, please visit: **http://www.nxp.com**

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13. Contents

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