

# PBRN113E series

NPN 800 mA, 40 V BISS RETs; R1 = 1 k $\Omega$ , R2 = 1 k $\Omega$

Rev. 01 — 1 March 2007

Product data sheet

## 1. Product profile

### 1.1 General description

800 mA NPN low  $V_{CEsat}$  Breakthrough In Small Signal (BISS) Resistor-Equipped Transistors (RET) family in small plastic packages.

Table 1. Product overview

Type number	Package		
	NXP	JEITA	JEDEC
PBRN113EK	SOT346	SC-59A	TO-236
PBRN113ES <sup>[1]</sup>	SOT54	SC-43A	TO-92
PBRN113ET	SOT23	-	TO-236AB

[1] Also available in SOT54A and SOT54 variant packages (see [Section 2](#)).

### 1.2 Features

- 800 mA output current capability
- High current gain  $h_{FE}$
- Built-in bias resistors
- Simplifies circuit design
- Low collector-emitter saturation voltage  $V_{CEsat}$
- Reduces component count
- Reduces pick and place costs
- $\pm 10\%$  resistor ratio tolerance

### 1.3 Applications

- Digital application in automotive and industrial segments
- Medium current peripheral driver
- Switching loads

### 1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CEO}$	collector-emitter voltage	open base	-	-	40	V
$I_O$	output current			<sup>[1]</sup>		
	PBRN113EK, PBRN113ET		-	-	600	mA
	PBRN113ES		-	-	800	mA

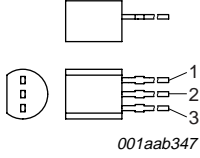
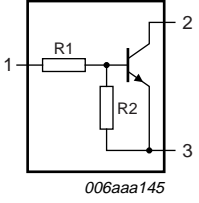
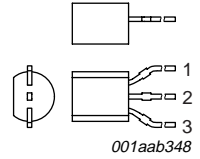
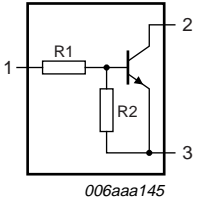
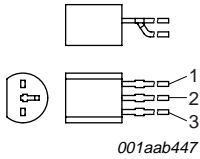
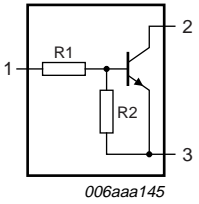
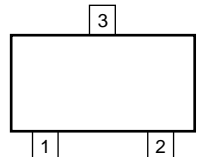
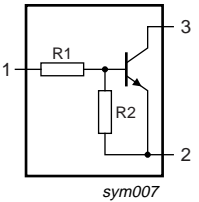
**Table 2. Quick reference data ...continued**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>ORM</sub>	repetitive peak output current					
	PBRN113EK, PBRN113ET	t <sub>p</sub> ≤ 1 ms; δ ≤ 0.33	-	-	800	mA
R1	bias resistor 1 (input)		0.7	1	1.3	kΩ
R2/R1	bias resistor ratio		0.9	1	1.1	

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

## 2. Pinning information

**Table 3. Pinning**

Pin	Description	Simplified outline	Symbol
<b>SOT54</b>			
1	input (base)	 <p>001aab347</p>	 <p>006aaa145</p>
2	output (collector)		
3	GND (emitter)		
<b>SOT54A</b>			
1	input (base)	 <p>001aab348</p>	 <p>006aaa145</p>
2	output (collector)		
3	GND (emitter)		
<b>SOT54 variant</b>			
1	input (base)	 <p>001aab447</p>	 <p>006aaa145</p>
2	output (collector)		
3	GND (emitter)		
<b>SOT23; SOT346</b>			
1	input (base)	 <p>006aaa144</p>	 <p>sym007</p>
2	GND (emitter)		
3	output (collector)		

### 3. Ordering information

Table 4. Ordering information

Type number	Package		Version
	Name	Description	
PBRN113EK	SC-59A	plastic surface-mounted package; 3 leads	SOT346
PBRN113ES <sup>[1]</sup>	SC-43A	plastic single-ended leaded (through hole) package; 3 leads	SOT54
PBRN113ET	-	plastic surface-mounted package; 3 leads	SOT23

[1] Also available in SOT54A and SOT54 variant packages (see [Section 2](#) and [Section 9](#)).

### 4. Marking

Table 5. Marking codes

Type number	Marking code <sup>[1]</sup>
PBRN113EK	G1
PBRN113ES	N113ES
PBRN113ET	*7G

[1] \* = -: made in Hong Kong  
 \* = p: made in Hong Kong  
 \* = t: made in Malaysia  
 \* = W: made in China

### 5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

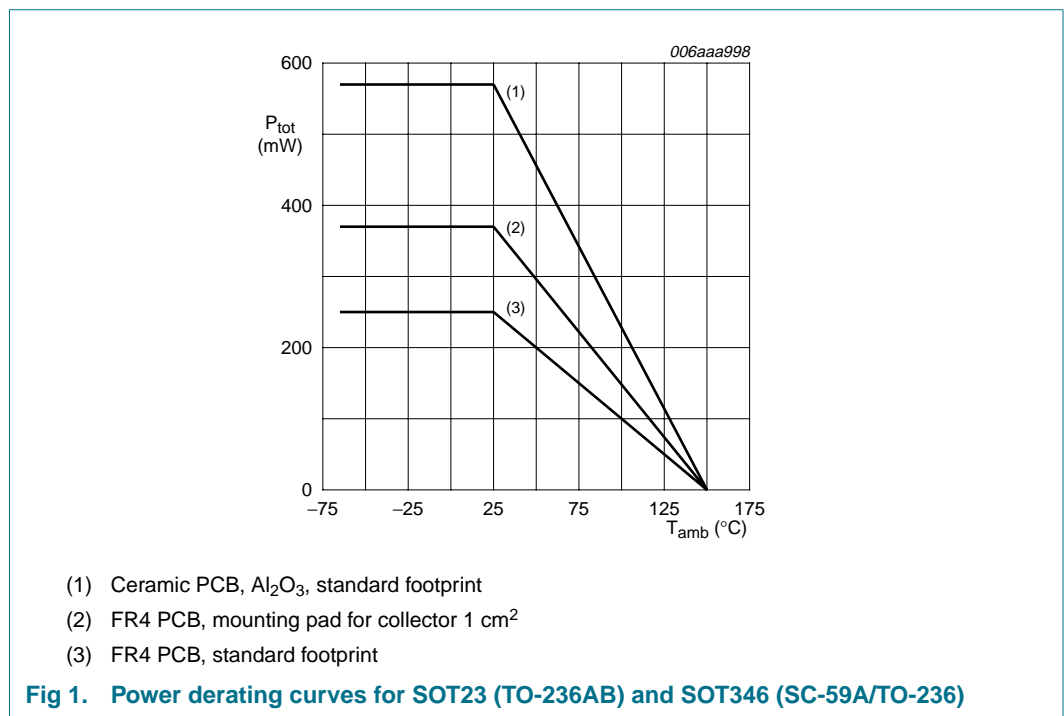
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CBO}$	collector-base voltage	open emitter	-	40	V
$V_{CEO}$	collector-emitter voltage	open base	-	40	V
$V_{EBO}$	emitter-base voltage	open collector	-	10	V
$V_I$	input voltage				
	positive		-	+10	V
	negative		-	-10	V
$I_O$	output current				
	PBRN113EK, PBRN113ET		<sup>[1]</sup> -	600	mA
			<sup>[2][3]</sup> -	700	mA
	PBRN113ES		<sup>[1]</sup> -	800	mA
$I_{ORM}$	repetitive peak output current				
	PBRN113EK, PBRN113ET	$t_p \leq 1$ ms; $\delta \leq 0.33$	-	800	mA

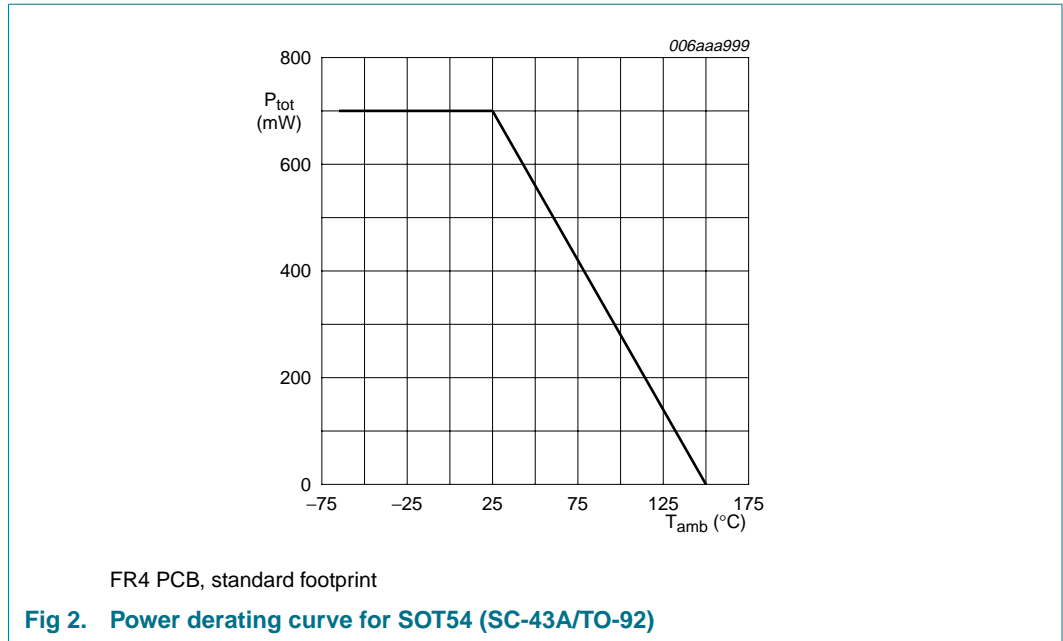
**Table 6. Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit		
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C					
			PBRN113EK, PBRN113ET	[1]	-	250	mW
				[2]	-	370	mW
				[3]	-	570	mW
	PBRN113ES		[1]	-	700	mW	
T <sub>j</sub>	junction temperature		-	150	°C		
T <sub>amb</sub>	ambient temperature		-65	+150	°C		
T <sub>stg</sub>	storage temperature		-65	+150	°C		

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [3] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.





## 6. Thermal characteristics

**Table 7. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit		
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air						
			PBRN113EK, PBRN113ET	[1]	-	-	500	K/W
				[2]	-	-	338	K/W
				[3]	-	-	219	K/W
	PBRN113ES		[1]	-	-	179	K/W	
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point							
		PBRN113EK, PBRN113ET		-	-	105	K/W	

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.

[3] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.

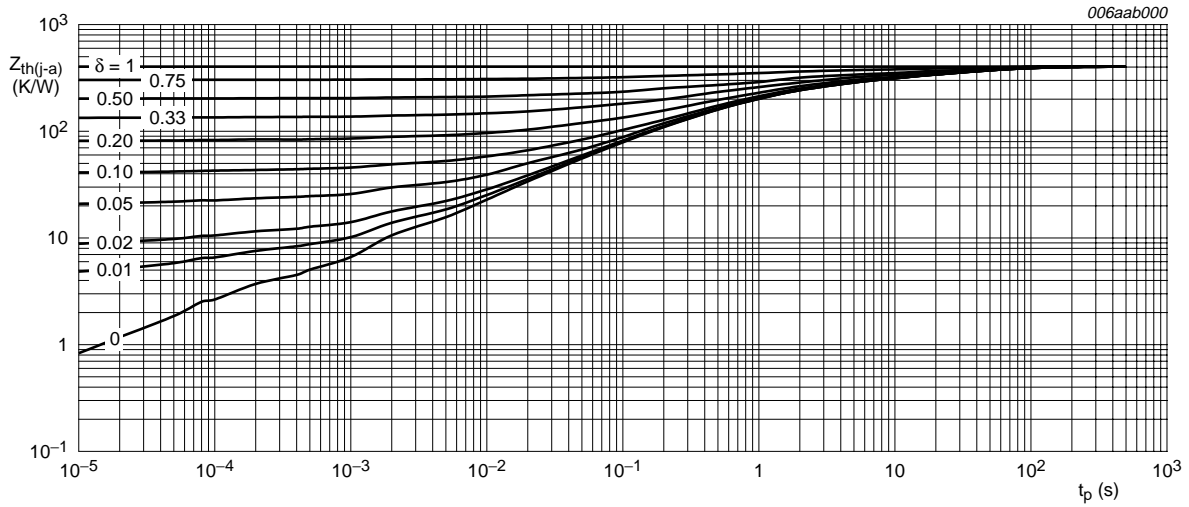


Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration for SOT23 (TO-236AB) and SOT346 (SC-59A/TO-236); typical values

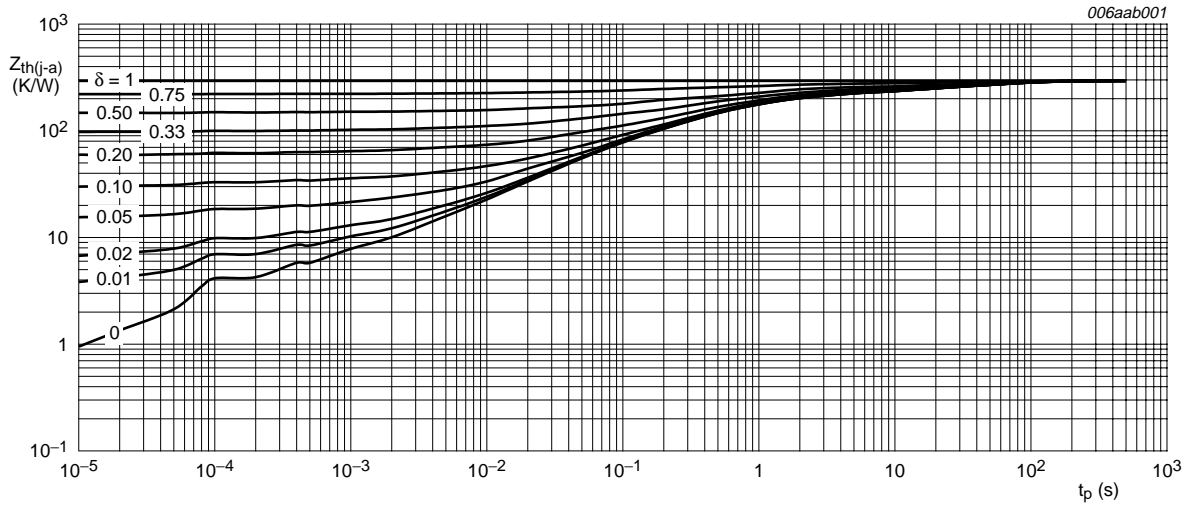
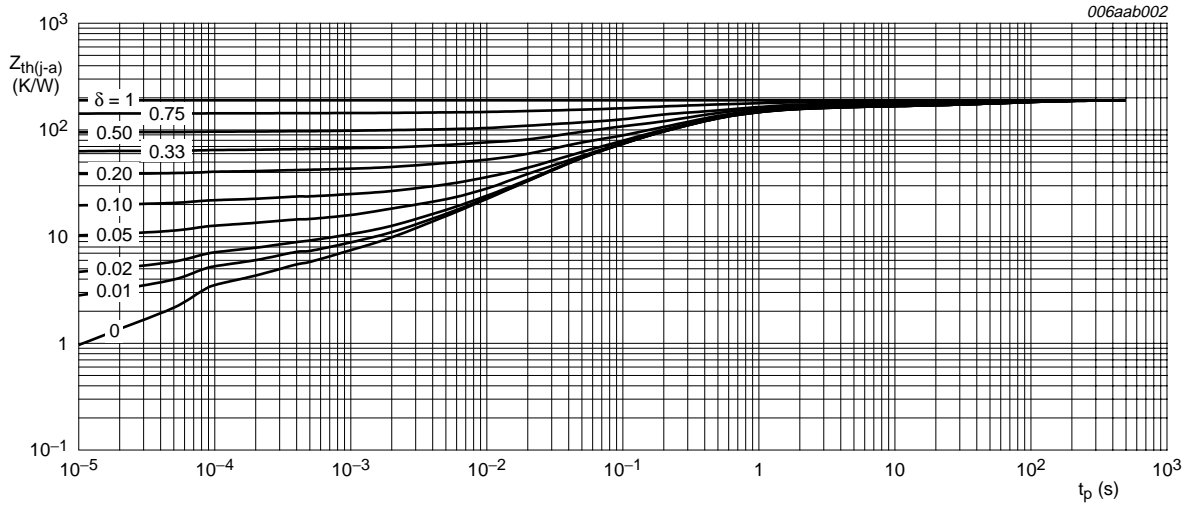
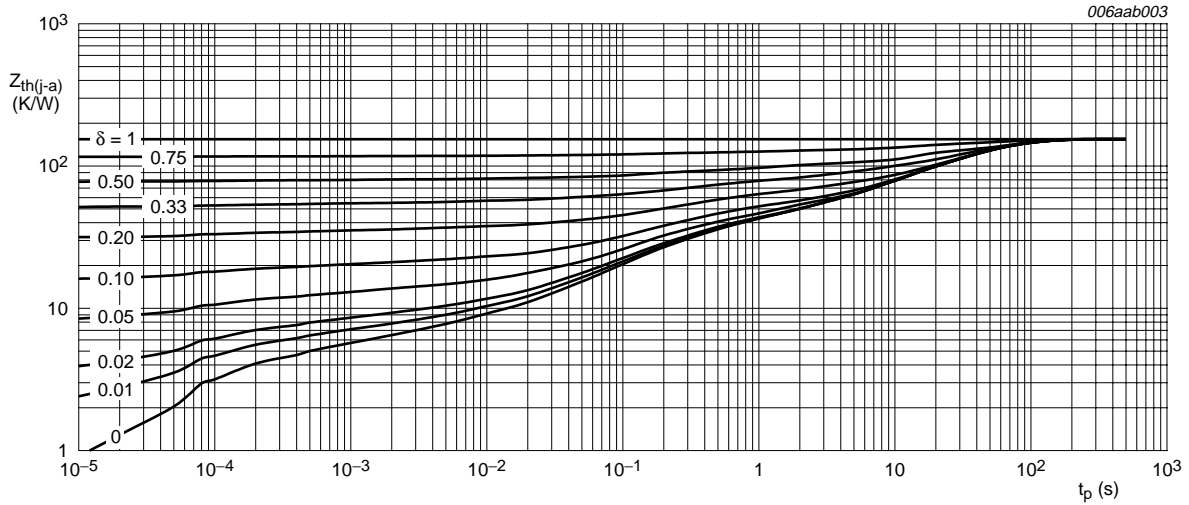


Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration for SOT23 (TO-236AB) and SOT346 (SC-59A/TO-236); typical values



Ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint

**Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration for SOT23 (TO-236AB) and SOT346 (SC-59A/TO-236); typical values**



FR4 PCB, standard footprint

**Fig 6. Transient thermal impedance from junction to ambient as a function of pulse duration for SOT54 (SC-43A/TO-92); typical values**

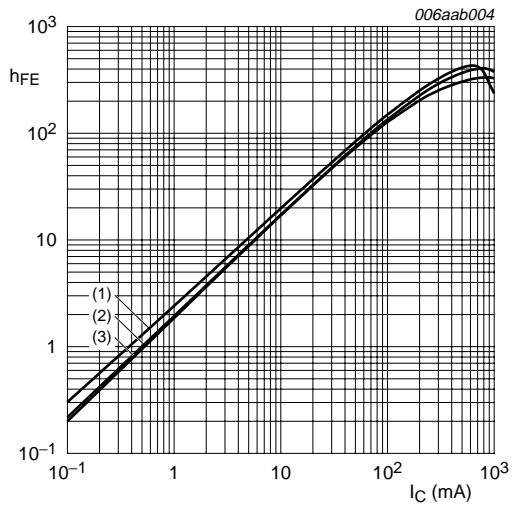
## 7. Characteristics

**Table 8. Characteristics**
*T<sub>amb</sub> = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = 30 V; I <sub>E</sub> = 0 A	-	-	100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0 A	-	-	0.5	$\mu$ A
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 5 V; I <sub>C</sub> = 0 A	-	-	4	mA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 50 mA	40	75	-	
		V <sub>CE</sub> = 5 V; I <sub>C</sub> = 300 mA	[1] 180	300	-	
		V <sub>CE</sub> = 5 V; I <sub>C</sub> = 600 mA	[1] 250	400	-	
		V <sub>CE</sub> = 5 V; I <sub>C</sub> = 800 mA	[1] 270	420	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = 50 mA; I <sub>B</sub> = 2.5 mA	-	25	35	mV
		I <sub>C</sub> = 200 mA; I <sub>B</sub> = 10 mA	-	60	85	mV
		I <sub>C</sub> = 500 mA; I <sub>B</sub> = 10 mA	[1] -	160	220	mV
		I <sub>C</sub> = 600 mA; I <sub>B</sub> = 6 mA	[1] -	320	550	mV
		I <sub>C</sub> = 800 mA; I <sub>B</sub> = 8 mA	[1] -	0.68	1.15	V
V <sub>I(off)</sub>	off-state input voltage	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 100 $\mu$ A	0.6	1	1.5	V
V <sub>I(on)</sub>	on-state input voltage	V <sub>CE</sub> = 0.3 V; I <sub>C</sub> = 20 mA	1	1.3	1.8	V
R1	bias resistor 1 (input)		0.7	1	1.3	k $\Omega$
R2/R1	bias resistor ratio		0.9	1	1.1	
C <sub>c</sub>	collector capacitance	V <sub>CB</sub> = 10 V; I <sub>E</sub> = i <sub>e</sub> = 0 A; f = 1 MHz	-	7	-	pF

[1] Pulse test: t<sub>p</sub>  $\leq$  300  $\mu$ s;  $\delta$   $\leq$  0.02.

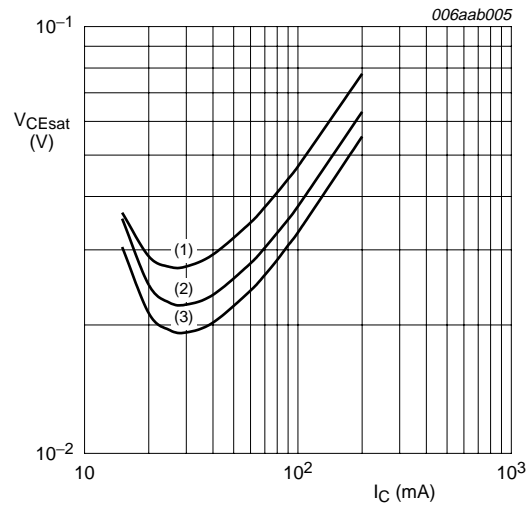




$V_{CE} = 5\text{ V}$

- (1)  $T_{amb} = 100\text{ }^{\circ}\text{C}$
- (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (3)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

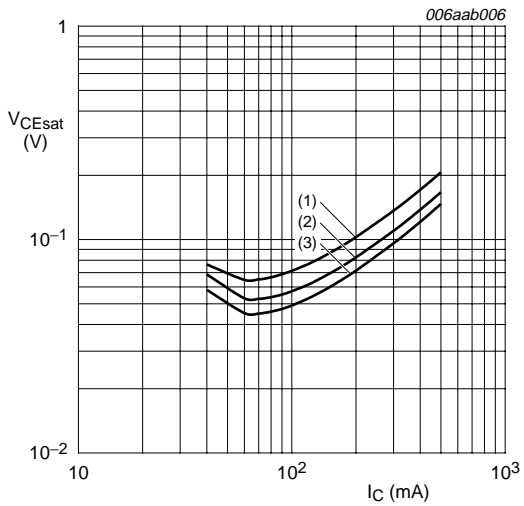
**Fig 7. DC current gain as a function of collector current; typical values**



$I_C/I_B = 20$

- (1)  $T_{amb} = 100\text{ }^{\circ}\text{C}$
- (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (3)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

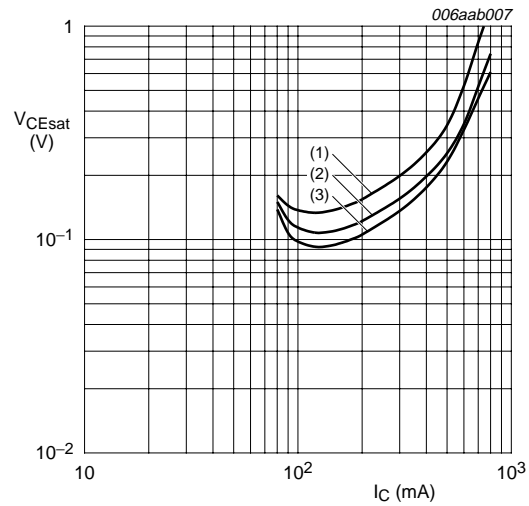
**Fig 8. Collector-emitter saturation voltage as a function of collector current; typical values**



$I_C/I_B = 50$

- (1)  $T_{amb} = 100\text{ }^{\circ}\text{C}$
- (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (3)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

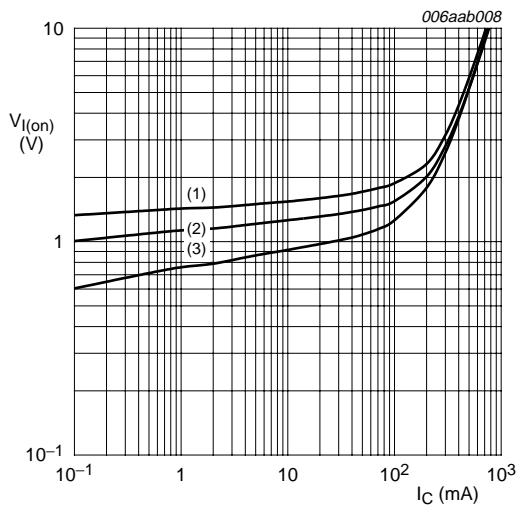
**Fig 9. Collector-emitter saturation voltage as a function of collector current; typical values**



$I_C/I_B = 100$

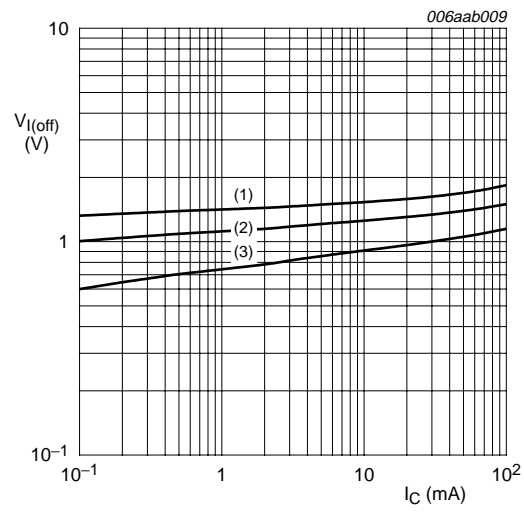
- (1)  $T_{amb} = 100\text{ }^{\circ}\text{C}$
- (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (3)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

**Fig 10. Collector-emitter saturation voltage as a function of collector current; typical values**



$V_{CE} = 0.3 \text{ V}$   
 (1)  $T_{amb} = -40 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100 \text{ }^\circ\text{C}$

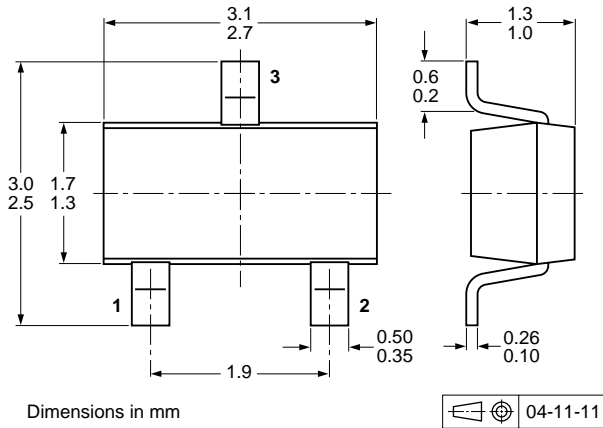
**Fig 11. On-state input voltage as a function of collector current; typical values**



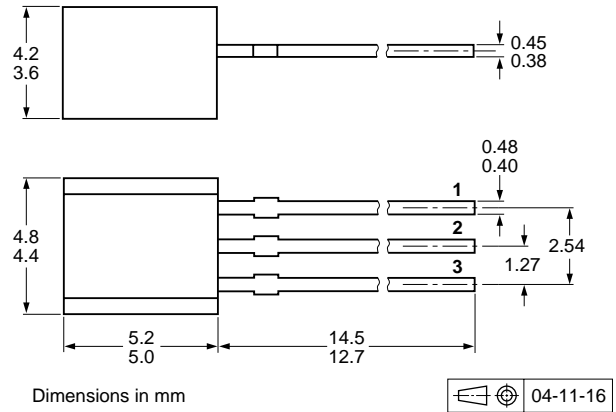
$V_{CE} = 5 \text{ V}$   
 (1)  $T_{amb} = -40 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100 \text{ }^\circ\text{C}$

**Fig 12. Off-state input voltage as a function of collector current; typical values**

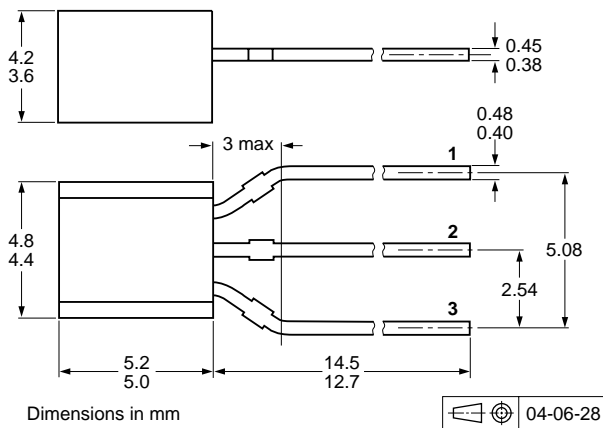
**8. Package outline**



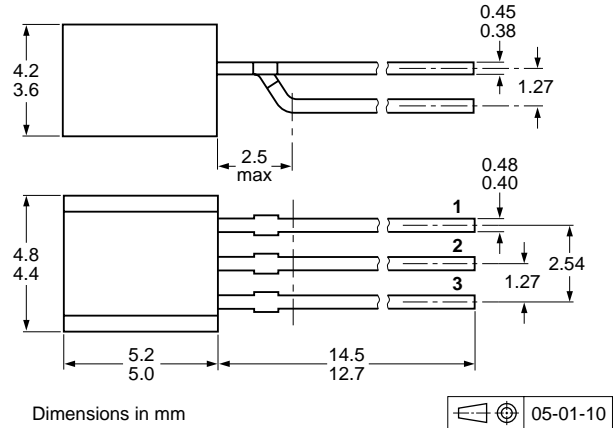
**Fig 13. Package outline SOT346 (SC-59A/TO-236)**



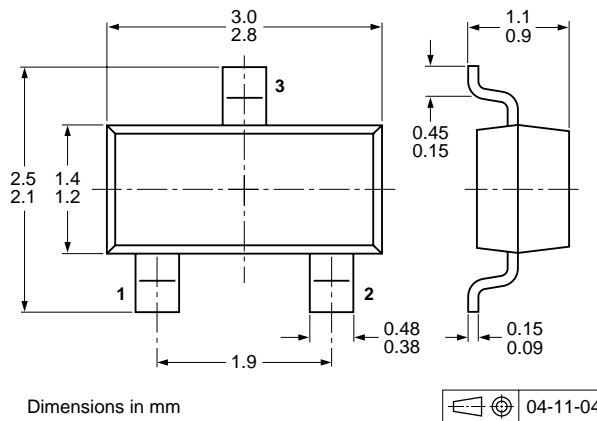
**Fig 14. Package outline SOT54 (SC-43A/TO-92)**



**Fig 15. Package outline SOT54A**



**Fig 16. Package outline SOT54 variant**



**Fig 17. Package outline SOT23 (TO-236AB)**

## 9. Packing information

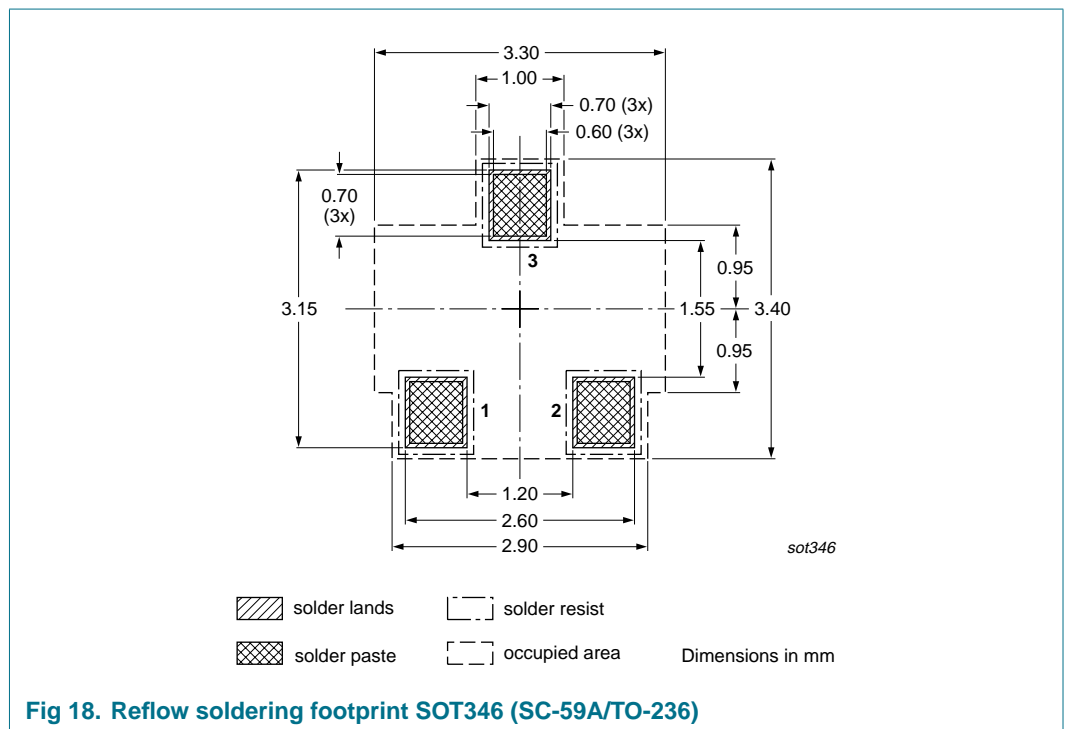
**Table 9. Packing methods**

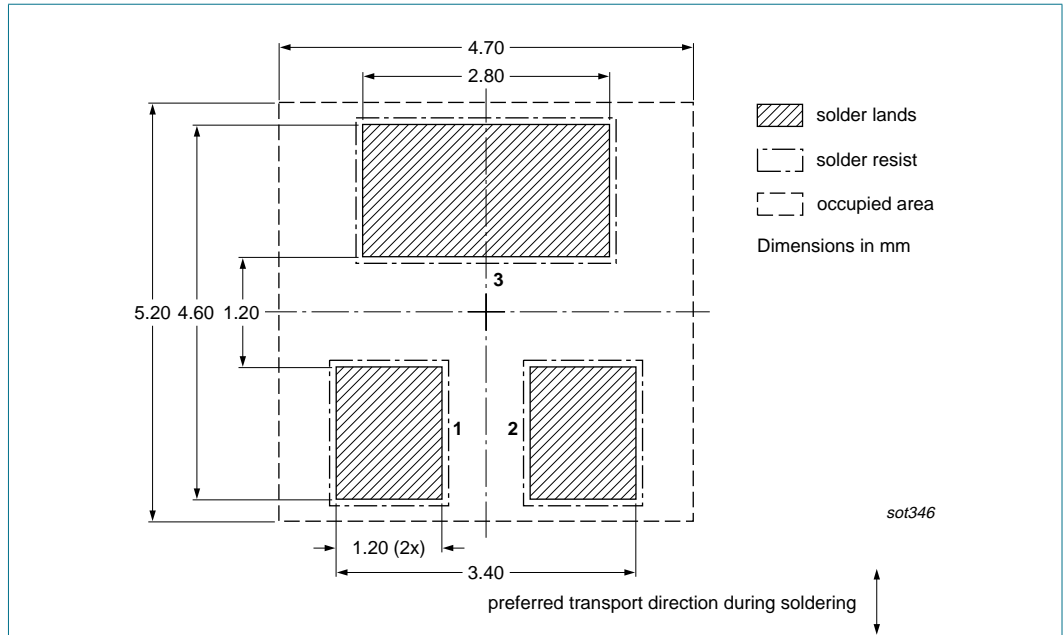
The indicated -xxx are the last three digits of the 12NC ordering code.<sup>[1]</sup>

Type number	Package	Description	Packing quantity		
			3000	5000	10000
PBRN113EK	SOT346	4 mm pitch, 8 mm tape and reel	-115	-	-135
PBRN113ES	SOT54	bulk, straight leads	-	-412	-
	SOT54A	tape and reel, wide pitch	-	-	-116
		tape ammpack, wide pitch	-	-	-126
	SOT54 variant	bulk, delta pinning	-	-112	-
PBRN113ET	SOT23	4 mm pitch, 8 mm tape and reel	-215	-	-235

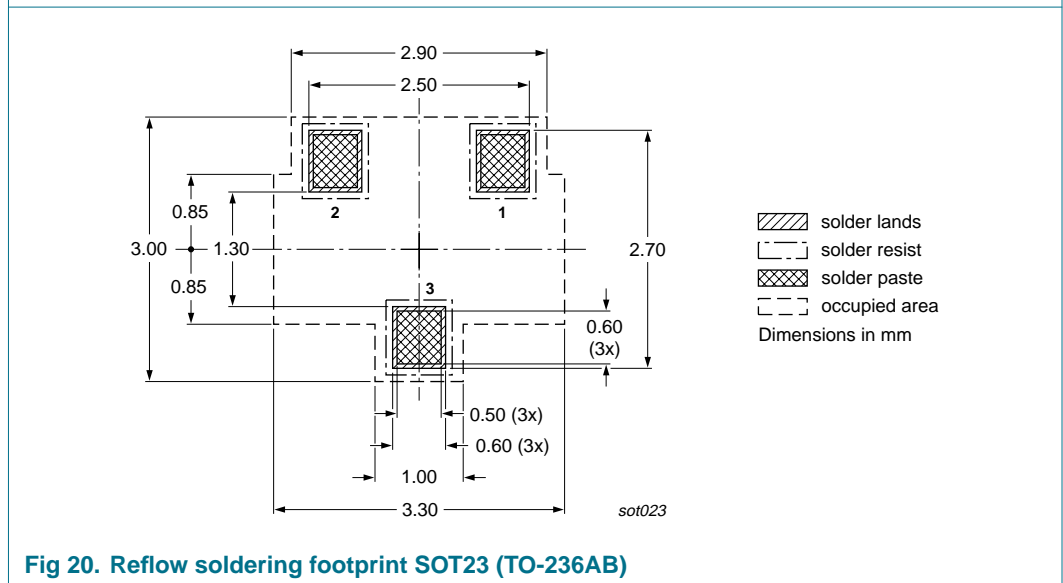
[1] For further information and the availability of packing methods, see [Section 13](#).

## 10. Soldering

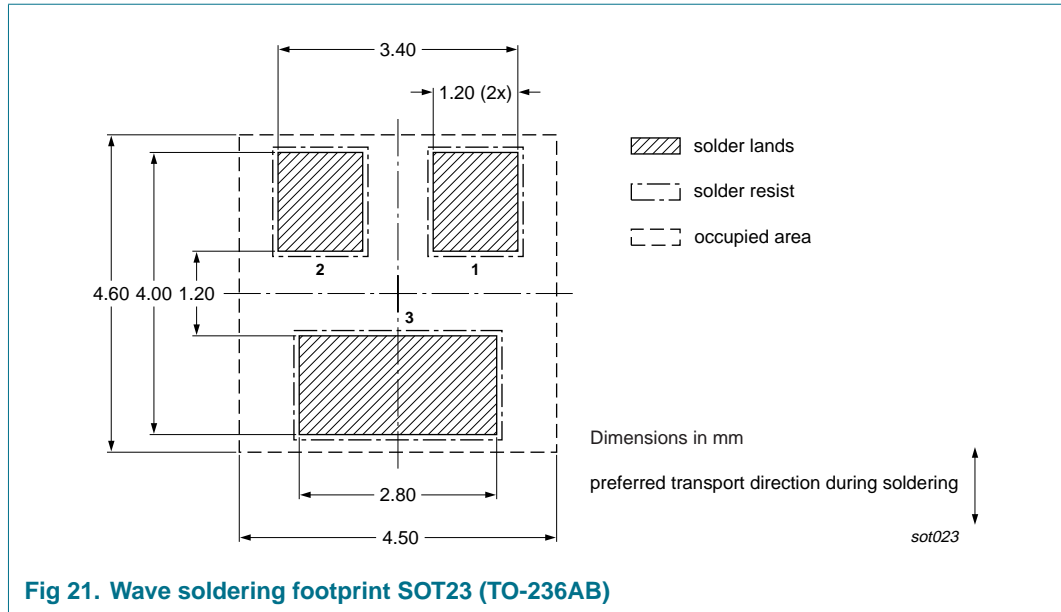




**Fig 19. Wave soldering footprint SOT346 (SC-59A/TO-236)**



**Fig 20. Reflow soldering footprint SOT23 (TO-236AB)**



## 11. Revision history

**Table 10. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBRN113E_SER_1	20070301	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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