9. High-Speed Differential Signaling in Cyclone Devices

C51009-1.5

Introduction

From high-speed backplane applications to high-end switch boxes, low-voltage differential signaling (LVDS) is the technology of choice. LVDS is a low-voltage differential signaling standard, allowing higher noise immunity than single-ended I/O technologies. Its low-voltage swing allows for high-speed data transfers, low power consumption, and less electromagnetic interference (EMI). LVDS I/O signaling is a data interface standard defined in the TIA/EIA-644 and IEEE Std. 1596.3 specifications.

The reduced swing differential signaling (RSDS) standard is a derivative of the LVDS standard. The RSDS I/O standard is similar in electrical characteristics to LVDS, but has a smaller voltage swing and therefore provides further power benefits and reduced EMI. National Semiconductor Corporation introduced the RSDS specification and now many vendors use it for flat panel display (FPD) links between the controller and the drivers that drive the display column drivers. Cyclone® devices support the RSDS I/O standard at speeds up to 311 megabits per second (Mbps).

Altera® Cyclone devices allow you to transmit and receive data through LVDS signals at a data rate up to 640 Mbps. For the LVDS transmitter and receiver, the Cyclone device's input and output pins support serialization and deserialization through internal logic.

This chapter describes how to use Cyclone I/O pins for LVDS and RSDS signaling and contains the following topics:

- Cyclone I/O Banks
- Cyclone High-Speed I/O Interface
- LVDS Receiver & Transmitter
- RSDS I/O Standard Support in Cyclone Devices
- Cyclone Receiver & Transmitter Termination
- Implementing Cyclone LVDS & RSDS I/O Pins in the Quartus® II Software
- Design Guidelines

Cyclone High-Speed I/O Banks

Cyclone devices offer four I/O banks, as shown in Figure 9–1. A subset of pins in each of the four I/O banks (on both rows and columns) support the high-speed I/O interface. Cyclone pin tables list the pins that support the high-speed I/O interface. The EP1C3 device in the 100-pin thin quad flat pack (TQFP) package does not support the high-speed I/O interface.

Figure 9–1. Cyclone I/O Banks

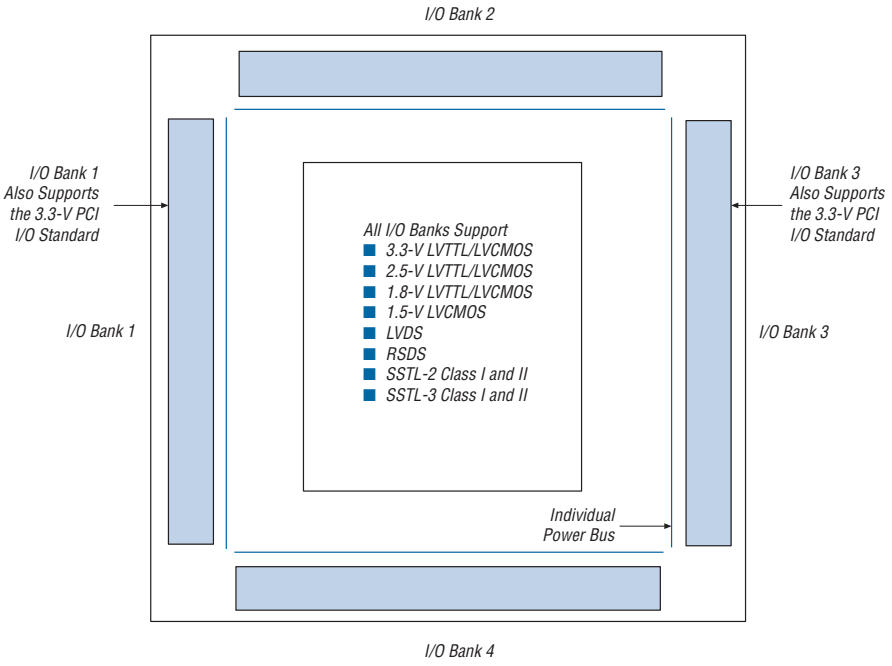


Table 9–1 shows the total number of supported high-speed I/O channels in each Cyclone device. You can use each channel as a receiver or transmitter.

Cyclone devices support different modes (× 1, × 2, × 4, × 7, × 8, and × 10) of operation with a maximum internal clock frequency of 405 MHz (-6 speed grade), 320 MHz (-7 speed grade), or 275 MHz (-8 speed grade), and a maximum data rate of 640 Mbps (-6 speed grade).

Table 9–1. Number of High-Speed I/O Channels Per Cyclone Device

Device	Pin Count	Total Number of High-Speed I/O Channels
EP1C3	144	34
EP1C4	324	103
	400	129
EP1C6	144	29
	240	72
	256	72
EP1C12	240	66
	256	72
	324	103
EP1C20	324	95
	400	129

For more information on I/O standards supported by Cyclone devices, see Chapter 8, Using Selectable I/O Standards in Cyclone Devices.

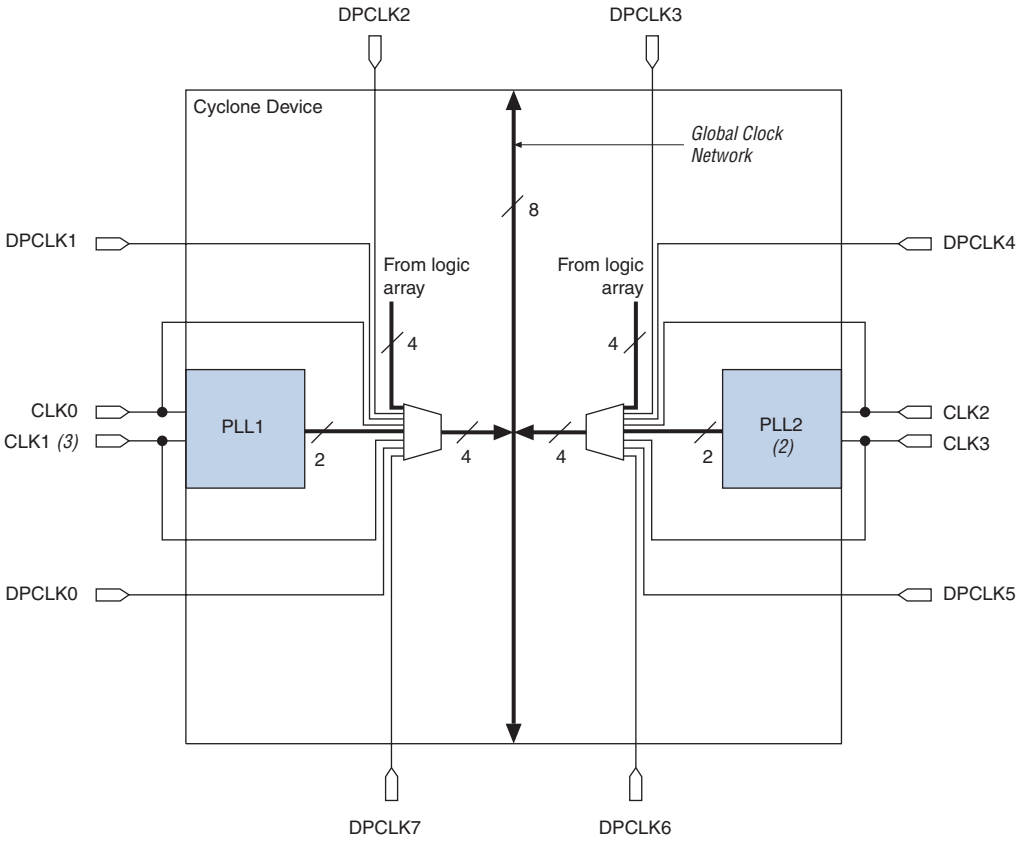
Cyclone High-Speed I/O Interface

You can use the I/O pins and internal logic to implement an high-speed I/O receiver and transmitter in Cyclone devices. Cyclone devices do not contain dedicated serialization or deserialization circuitry; therefore, shift registers, internal global phase-locked loops (PLLs), and I/O cells are used to perform serial-to-parallel conversions on incoming data and parallel-to-serial conversion on outgoing data.

Clock Domains

Cyclone devices provide a global clock network and two PLLs (the EP1C3 device only contains one PLL). The global clock network consists of eight global clock lines that drive through the entire device (see Figure 9–2). There are four dedicated clock pins that feed the PLL inputs (two dedicated clocks for each PLL). PLL pins can also act as LVDS input pins. Cyclone PLLs provide general-purpose clocking with clock multiplication and phase shifting as well as external outputs for high-speed differential I/O support. Altera recommends that designers use a data channel for the high-speed clock output for better balanced skew on the transmitter data pins with respect to the output clock.

Figure 9–2. Cyclone Global Clock Network *Note (1)*



Notes to Figure 9–2:

(1) The EP1C3 device in the 100-pin TQFP package has five DPCLK pins (DPCLK2, DPCLK3, DPCLK4, DPCLK6, and DPCLK7).

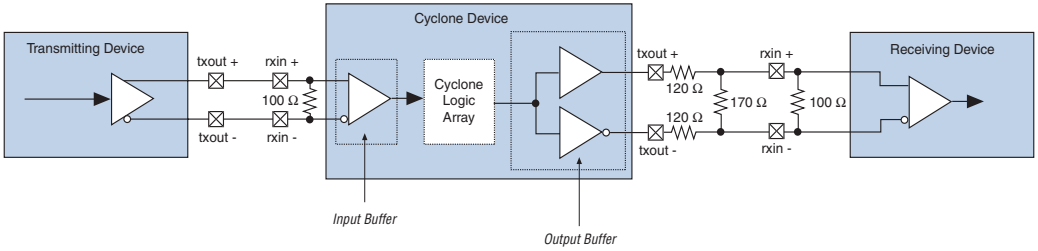
(2) EP1C3 devices only contain one PLL (PLL1).

(3) EP1C3 devices in the 100-pin TQFP package do not support differential clock inputs or outputs.

LVDS Receiver & Transmitter

Figure 9–3 shows a simple point-to-point LVDS application where the source of the data is a LVDS transmitter. These LVDS signals are typically transmitted over a pair of printed circuit board (PCB) traces, but a combination of a PCB trace, connectors, and cables is a common application setup.

Figure 9–3. Typical LVDS Application



The Cyclone LVDS I/O pins meet the IEEE 1596 LVDS specification. Figures 9–4 and 9–5 show the signaling levels for LVDS receiver inputs and transmitter outputs.

Figure 9–4. Receiver Input Waveform for the Differential I/O Standard

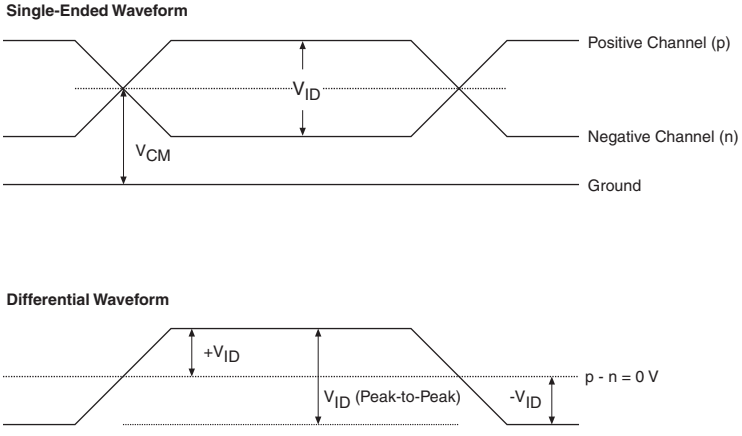


Figure 9–5. Transmitter Output Waveform for Differential I/O Standard

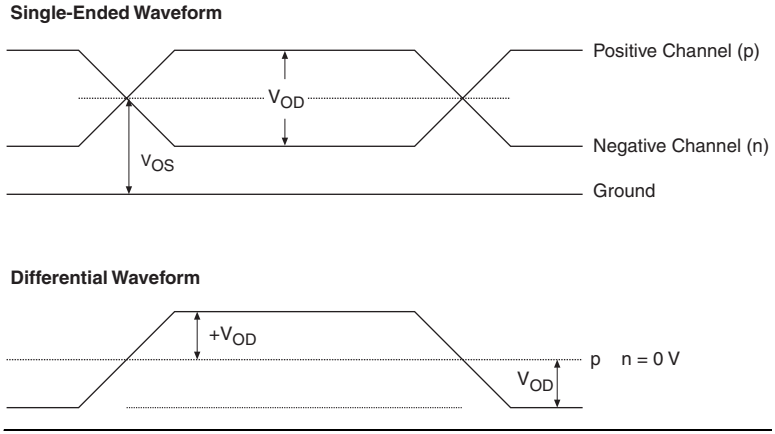


Table 9–2 lists the LVDS I/O specifications.

Table 9–2. LVDS I/O Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCINT}	Supply Voltage		1.425	1.5	1.575	V
V_{CCIO}	I/O Supply Voltage		2.375	2.5	2.625	V
V_{OD}	Differential Output Voltage	R_L = 100 Ω	250	350	550	mV
Δ V_{OD}	Change in V_{OD} between H and L	R_L = 100 Ω			50	mV
V_{OS}	Output Offset Voltage	R_L = 100 Ω	1.125	1.25	1.375	V
Δ V_{OS}	Change in V_{OS} between H and L	R_L = 100 Ω			50	mV
V_{ID}	Input differential voltage swing (single-ended)	0.1 V ≤V_{CM} ≤ 2.0 V	100		650	mV
V_{IN}	Receiver input voltage range		0		2.4	V

Table 9–2. LVDS I/O Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CM}	Receiver input common mode voltage	100 mV ≤V_{ID} ≤ 650 mV	100		2,000	mV
R_L	Receiver Differential Input Resistor		90	100	110	W

RSDS I/O Standard Support in Cyclone Devices

The RSDS specification defines its use in chip-to-chip applications between the timing controller and the column drivers on display panels. The Cyclone characterization and simulations were performed to meet the National Semiconductor Corp. RSDS Interface Specification. Table 9–3 shows the RSDS electrical characteristics for Cyclone devices.

Table 9–3. RSDS Electrical Characteristics for Cyclone Devices

Symbol	Parameter	Min	Typ	Max	Units
V_{CCIO}	I/O supply voltage	2.375	2.5	2.625	V
V_{OD}	Differential output voltage	100	200	600	mV
V_{OS}	Output offset voltage	0.5	1.2	1.5	V
V_{TH}	Differential threshold			±100	mV
V_{CM}	Input common mode voltage	0.3		1.5	V

Figures 9–6 and 9–7 show the RSDS receiver and transmitter signal waveforms.

Figure 9–6. Receiver Input Signal Level Waveforms for RSDS

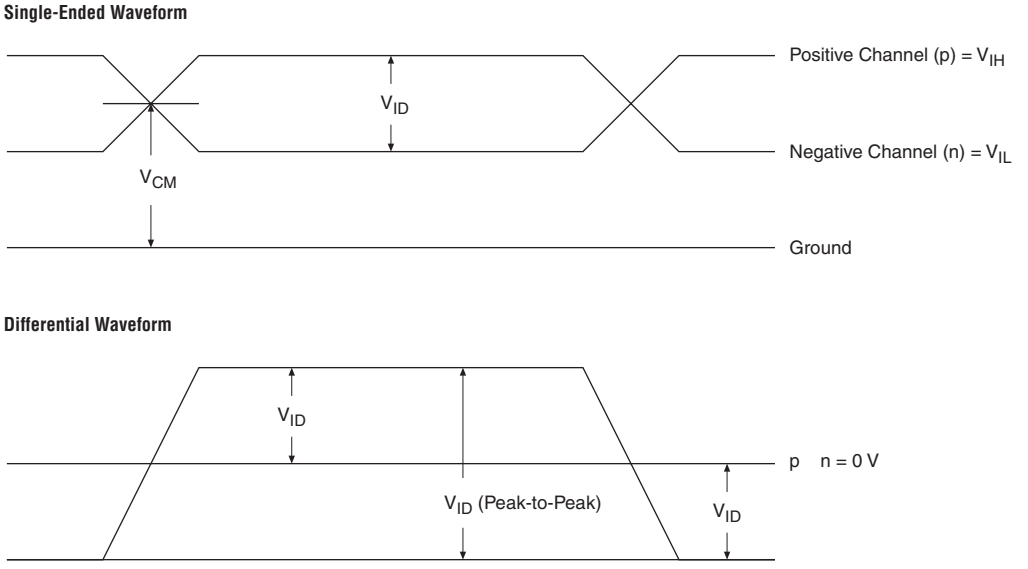
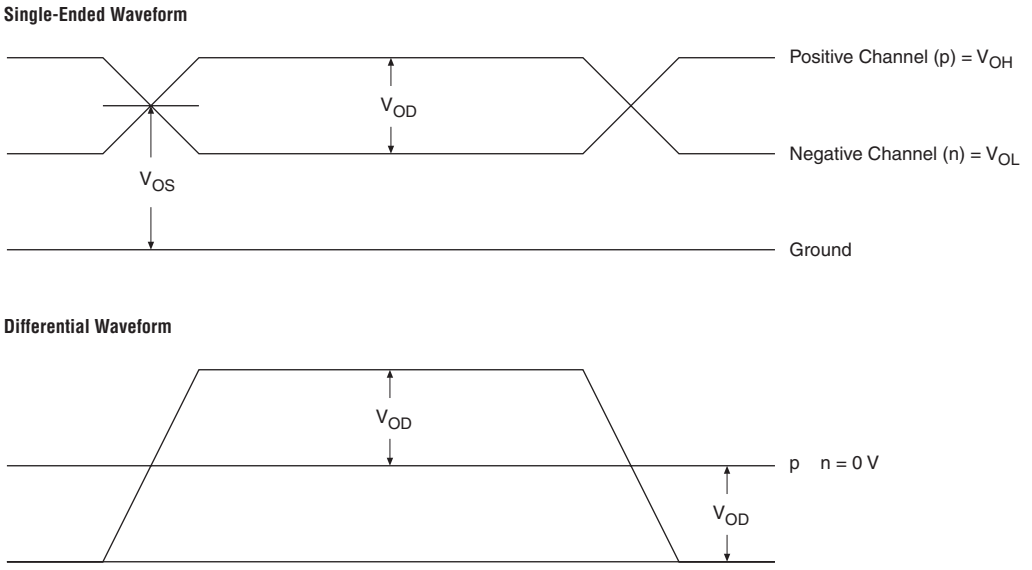


Figure 9–7. Transmitter Output Signal Level Waveforms for RSDS



Cyclone FPGA devices support all three bus configuration types as defined by the RSDS specification:

- Multi-drop bus with double termination
- Multi-drop bus with single end termination
- Double multi-drop bus with single termination

Designing with RSDS

Cyclone devices support the RSDS standard using the LVDS I/O buffer types. For receivers, the LVDS input buffer can be used without any changes. For transmitters, the LVDS output buffer can be used with the external resistor network shown in Figure 9–8.

Figure 9–8. RSDS Resistor Network

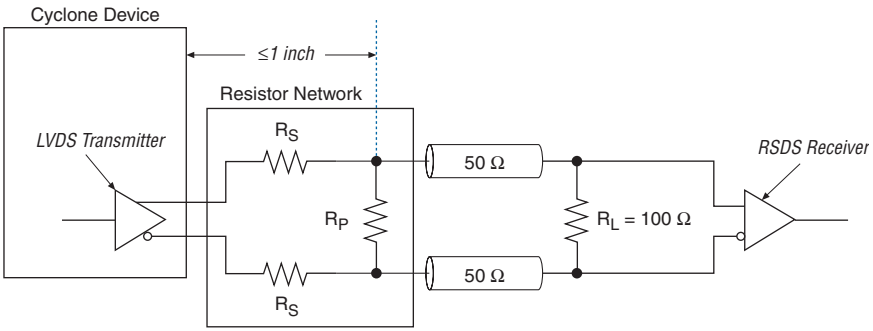


Table 9–4 shows the resistor values recommended for each RSDS bus configuration type.

Table 9–4. Recommended Resistor Values

Bus Configuration Type	R_S (Ω)	R_P (Ω)
Multi-drop bus with double termination	160	145
Multi-drop bus with single end termination	226	124
Double multi-drop bus with single termination	226	124

For more information on RSDS bus configuration types, see the RSDS specification from the National Semiconductor web site (**www.national.com**).

A resistor network is required to attenuate the LVDS output voltage swing to meet the RSDS specifications. The resistor network values can be modified to reduce power or improve the noise margin. The resistor values chosen should satisfy the following equation:

$$\frac{R_S \times \frac{R_P}{2}}{R_S + \frac{R_P}{2}} = 50\ \Omega$$

For example, in the multi-drop bus with single end termination or double multi-drop bus with single termination bus configuration, the resistor values can be modified to $R_S = 200\ \Omega$ and $R_P = 130\ \Omega$ to increase the V_{OD} or voltage swing of the signal.

Additional simulations using the IBIS models should be performed to validate that custom resistor values meet the RSDS requirements.

RSDS Software Support

When designing for the RSDS I/O standard, assign the LVDS I/O standard to the I/O pins intended for RSDS in the Quartus II software. Contact Altera Applications for reference designs.

High-Speed I/O Timing in Cyclone Devices

Since LVDS and RSDS data communication is source synchronous, timing analysis is different than other I/O standards. You must understand how to analyze timing for the high-speed I/O signal, which is based on skew between the data and the clock signal.

You should also consider board skew, cable skew, and clock jitter in your calculation. This section provides details on high-speed I/O standards timing parameters in Cyclone devices.

Table 9–5 defines the parameters of the timing diagram shown in Figure 9–9.

Table 9–5. High-Speed I/O TIming Definitions *Note (1)*

Parameter	Symbol	Description
High-speed clock frequency	f_{HSCLK}	High-speed receiver/transmitter input clock frequency.
High-speed I/O data rate	HSIODR	High-speed receiver/transmitter input and output data rate.
High-speed external output clock	$f_{HSCLKOUT}$	High-speed transmitter external output clock frequency using an LVDS data channel.
Channel-to-channel skew	TCCS	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window	SW	The period of time during which the data must be valid in order for you to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window. SW = t_{SW} (max) – t_{SW} (min).
Receiver input skew margin	RSKM	RSKM is defined by the total margin left after accounting for the sampling window and TCCS. The RSKM equation is: RSKM = (TUI – SW – TCCS) / 2
Input jitter tolerance (peak-to-peak)		Allowed input jitter on the input clock to the PLL that is tolerable while maintaining PLL lock.
Output jitter (peak-to-peak)		Peak-to-peak output jitter from the PLL.
Rise time	t_{RISE}	Low-to-high transmission time.
Fall time	t_{FALL}	High-to-low transmission time.
Duty cycle	t_{DUTY}	Duty cycle on LVDS transmitter output clock.
PLL lock time	t_{LOCK}	Lock time for the PLL

Note to Table 9–5:

(1) The TCCS specification applies to the whole bank of LVDS as long as the SERDES logic is placed within the LAB adjacent to the output pins.

Figure 9–9. High-Speed I/O Timing Diagram

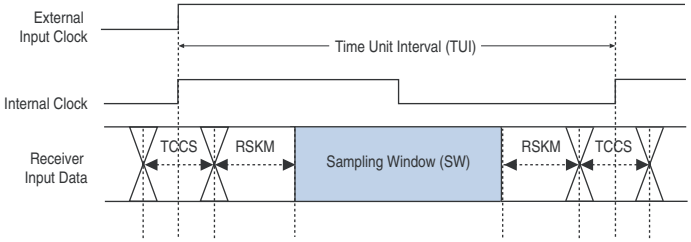
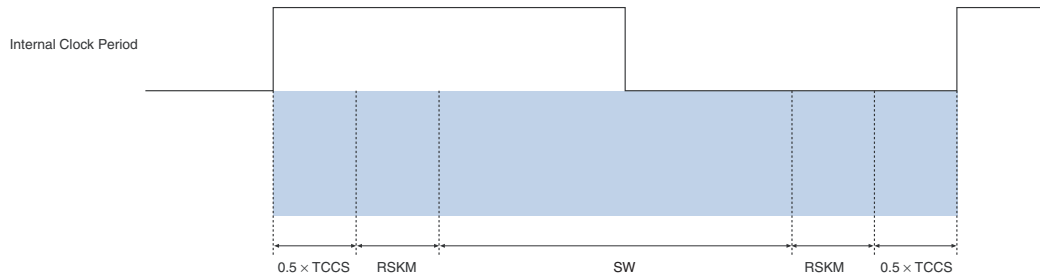


Figure 9–10 shows the high-speed I/O timing budget.

Figure 9–10. Cyclone High-Speed I/O Timing Budget *Note (1)*



Note to Figure 9–10:

(1) The equation for the high-speed I/O timing budget is: Period = 0.5 × TCCS + RSKM + SW + RSKM + 0.5 × TCCS.

Table 9–6 shows the RSDS timing budget for Cyclone devices at 311 Mbps.

Table 9–6. RSDS Timing Specification for Cyclone Devices (Part 1 of 2)

Symbol	Conditions	-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	×10	15.625	NA	31.1	15.625	NA	31.1	15.625	NA	31.1	MHz
	×8	15.625	NA	38.875	15.625	NA	38.875	15.625	NA	38.875	MHz
	×7	17.857	NA	44.429	17.857	NA	44.429	17.857	NA	44.429	MHz
	×4	15.625	NA	77.75	15.625	NA	77.75	15.625	NA	77.75	MHz
	×2	15.625	NA	155.5	15.625	NA	155.5	15.625	NA	155.5	MHz
	×1 *(1)*	15.625	NA	275	15.625	NA	275	15.625	NA	275	MHz

Table 9–6. RSDS Timing Specification for Cyclone Devices (Part 2 of 2)

Symbol	Conditions	-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
HSIODR	×10	156.25	NA	311	156.25	NA	311	156.25	NA	311	Mbps
	×8	125	NA	311	125	NA	311	125	NA	311	Mbps
	×7	125	NA	311	125	NA	311	125	NA	311	Mbps
	×4	62.5	NA	311	62.5	NA	311	62.5	NA	311	Mbps
	×2	31.25	NA	311	31.25	NA	311	31.25	NA	311	Mbps
	×1 *(1)*	15.625	NA	275	15.625	NA	275	15.625	NA	275	Mbps
$f_{HSCLKOUT}$		15.625	NA	275	15.625	NA	275	15.625	NA	275	MHz
TCCS		NA	NA	±150	NA	NA	±150	NA	NA	±150	ps
SW		NA	NA	500	NA	NA	550	NA	NA	550	ps
Input jitter tolerance (peak-to-peak)		NA	NA	400	NA	NA	400	NA	NA	400	ps
Output jitter (peak-to-peak)		NA	NA	400	NA	NA	400	NA	NA	400	ps
t_{RISE}		150	200	250	150	200	250	150	200	250	ps
t_{FALL}		150	200	250	150	200	250	150	200	250	ps
t_{DUTY}		45	50	55	45	50	55	45	50	55	%
t_{LOCK}		NA	NA	100	NA	NA	100	NA	NA	100	µs

Note to Table 9–6:

(1) The PLL must divide down the input clock frequency to have the internal clock frequency meet the specification shown in Tables 4–19 and 4–52 from Chapter 4, DC & Switching Characteristics.

Table 9–7 shows the LVDS timing budget for Cyclone devices at 640 Mbps.

Table 9–7. LVDS Timing Specification for Cyclone Devices

Symbol	Conditions	-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK}	×10	15.625	NA	64	15.625	NA	64	15.625	NA	55	MHz
	×8	15.625	NA	80	15.625	NA	80	15.625	NA	68.75	MHz
	×7	17.857	NA	91.429	17.857	NA	91.429	17.857	NA	78.571	MHz
	×4	15.625	NA	160	15.625	NA	160	15.625	NA	137.5	MHz
	×2	15.625	NA	320	15.625	NA	320	15.625	NA	275	MHz
	×1 *(1)*	15.625	NA	567	15.625	NA	549	15.625	NA	531	MHz
HSIODR	×10	156.25	NA	640	156.25	NA	640	156.25	NA	550	Mbps
	×8	125	NA	640	125	NA	640	125	NA	550	Mbps
	×7	125	NA	640	125	NA	640	125	NA	550	Mbps
	×4	62.5	NA	640	62.5	NA	640	62.5	NA	550	Mbps
	×2	31.25	NA	640	31.25	NA	640	31.25	NA	550	Mbps
	×1 *(1)*	15.625	NA	320	15.625	NA	320	15.625	NA	275	Mbps
$f_{HSCLKOUT}$		15.625	NA	320	15.625	NA	320	15.625	NA	275	MHz
TCCS		NA	NA	±150	NA	NA	±150	NA	NA	±150	ps
SW		NA	NA	500	NA	NA	500	NA	NA	550	ps
Input jitter tolerance (peak-to-peak)		NA	NA	400	NA	NA	400	NA	NA	400	ps
Output jitter (peak-to-peak)		NA	NA	400	NA	NA	400	NA	NA	400	ps
t_{RISE}		150	200	250	150	200	250	150	200	250	ps
t_{FALL}		150	200	250	150	200	250	150	200	250	ps
t_{DUTY}		45	50	55	45	50	55	45	50	55	%
t_{LOCK}		NA	NA	100	NA	NA	100	NA	NA	100	µs

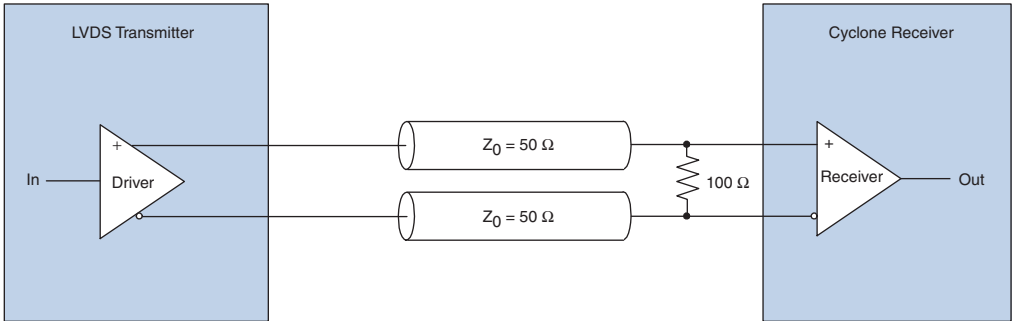
Note to Table 9–7:

(1) The PLL must divide down the input clock frequency to have the internal clock frequency meet the specification shown in Tables 4–19 and 4–52 from Chapter 4, DC & Switching Characteristics.

LVDS Receiver & Transmitter Termination

Receiving LVDS signals on Cyclone I/O pins is straightforward, and can be done by assigning LVDS to desired pins in the Quartus II software. A 100-Ω parallel terminator is required at the receiver input pin, as shown in Figure 9–11.

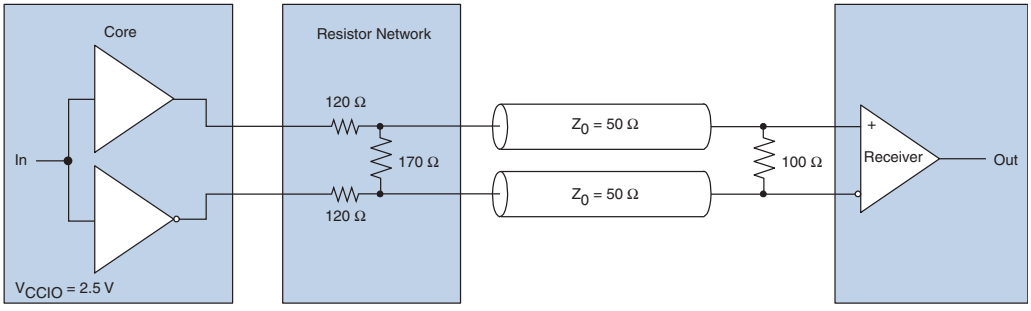
Figure 9–11. Termination Scheme on Cyclone LVDS Receiver



For PCB layout guidelines, refer to *AN 224: High-Speed Board Layout Guidelines*.

Cyclone LVDS transmitter signals are generated using a resistor network, as shown in Figure 9–12 (with R_S = 120 Ω and R_{DIV} = 170 Ω). The resistor network attenuates the driver outputs to levels similar to the LVDS signaling, which is recognized by LVDS receivers with minimal effect on 50-Ω trace impedance.

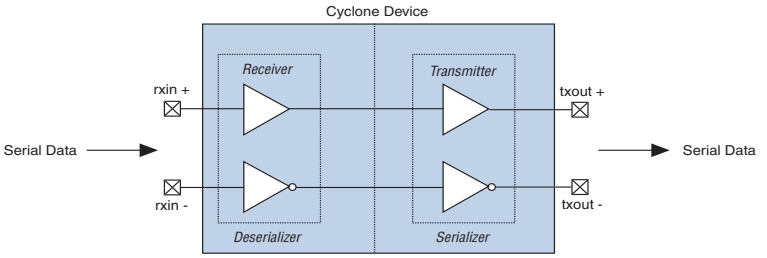
Figure 9–12. Termination Scheme on Cyclone LVDS Transmitter



Implementing Cyclone LVDS & RSDS I/O Pins in the Quartus II Software

For differential signaling, the receiver must deserialize the incoming data and send it to the internal logic as a parallel signal. Accordingly, the transmitter must serialize the parallel data coming from the internal logic to send it off-chip (see Figure 9–13).

Figure 9–13. Deserialization & Serialization at Receiver & Transmitter



Although Cyclone devices do not incorporate a dedicated serializer/deserializer (SERDES), you can incorporate these functions in your design using the Quartus II software. The device implements the SERDES in logic elements (LEs) and requires a PLL.

LVDS in Cyclone devices is implememented using megafunctions in Quartus II software. The `altlvds_rx` megafunction implements a deserialization receiver. The `altlvds_tx` megafunction implements a serialization transmitter.

The placement of the LE registers is handled by the LVDS MegaWizard® in the Quartus II software. The Cyclone device DDIO logic placer in the Quartus II software only places the DDIO output registers according to Altera's recommendation and does not check if it meets the TCCS specification. There is no timing analysis done in the Quartus II software to report the TCCS. Verify timing anaysis by running the Timing Analyzer in the Quartus II software.

Refer to the Quartus II software documenation and the Quartus II Help for more information on these megafunctions. Follow the recommendations in Tables 9–8 and 9–9 for PLL phase shift settings. The operation of these settings are guaranteed by operation.

The required receiver PLL phase settings for top and bottom I/O banks (I/O Bank 2 and 4) based on high-speed I/O data rate and operating mode are shown in Table 9–8.

Table 9–8. Receiver PLL Phase Settings for Top & Bottom I/O Banks

Device	Phase Shift (Degree)			Unit
	0	22.5	45	
EP1C3			300 to 640	Mbps
EP1C4		601 to 640	300 to 600	Mbps
EP1C6		601 to 640	300 to 600	Mbps
EP1C12		451 to 640	300 to 450	Mbps
EP1C20	551 to 640	300 to 550		Mbps

The required receiver PLL phase settings for right and left I/O banks (I/O Bank 1 and 3) based on high-speed I/O data rate and operating mode are shown in Table 9–9.

Table 9–9. Receiver PLL Phase Settingsfor Right & Left I/O Banks

Device	Phase Shift (Degree)				Unit
	–22.5	0	22.5	45	
EP1C3			451 to 640	300 to 450	Mbps
EP1C4		551 to 640	300 to 550		Mbps
EP1C6			451 to 640	300 to 450	Mbps
EP1C12	601 to 640	451 to 600	300 to 450		Mbps
EP1C20	501 to 640	300 to 500			Mbps

Design Guidelines

To implement LVDS in Cyclone devices, adhere to the following design guidelines in the Quartus II software.

- Route LVDS `CLKOUT` to pins through regular user LVDS pins. This routing provides better TCCS margin.
- To meet the t_{SU} and t_{CO} timing requirement between serial and parallel registers, use the I/O registers of the input and output pins.
- f_{MAX} is limited by the delay between the IOE and the next logic element (LE) register. To achieve an f_{MAX} of 320 MHz, the delay between the IOE and the next LE register at the receiver and transmitter side must not be more than 3.125 ns.
- The best location to implement the shift registers is within the LAB adjacent to the input or output pin.
- LVDS data and clock should be aligned at the output pin. If these signals are not aligned, use a phase shift to align them.

Differential Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply, there are restrictions on placement of single-ended I/O pins in relation to differential pads. Refer to the guidelines in Chapter 8, Using Selectable I/O Standards in Cyclone Devices for placing single-ended pads with respect to differential pads in Cyclone devices.

Board Design Considerations

This section explains how to get the optimal performance from the Cyclone I/O block and ensure first-time success in implementing a functional design with optimal signal quality. The critical issues of controlled impedance of traces and connectors, differential routing, and termination techniques must all be considered to get the best performance from the integrated circuit (IC). Use this chapter together with Section I, Cyclone FPGA Family Data Sheet.

The Cyclone device generates signals that travel over the media at frequencies as high as 640 Mbps. Use the following general guidelines:

- Base board designs on controlled differential impedance. Calculate and compare all parameters such as trace width, trace thickness, and the distance between two differential traces.
- Maintain equal distance between traces in LVDS pairs, as much as possible. Routing the pair of traces close to each other will maximize the common-mode rejection ratio (CMRR)
- Longer traces have more inductance and capacitance. These traces should be as short as possible to limit signal integrity issues.
- Place termination resistors as close to receiver input pins as possible.
- Use surface mount components.

- Avoid 90° or 45° corners.
- Use high-performance connectors.
- Design backplane and card traces so that trace impedance matches the connector's and/or the termination's impedance.
- Keep equal number of vias for both signal traces.
- Create equal trace lengths to avoid skew between signals. Unequal trace lengths result in misplaced crossing points and decrease system margins as the TCCS value increases.
- Limit vias because they cause discontinuities.
- Use the common bypass capacitor values such as 0.001 µF, 0.01 µF, and 0.1 µF to decouple the high-speed PLL power and ground planes.
- Keep switching TTL signals away from differential signals to avoid possible noise coupling.
- Do not route TTL clock signals to areas under or above the differential signals.
- Analyze system-level signals.

Conclusion

Cyclone LVDS I/O capabilities enable you to keep pace with increasing design complexity while offering the lowest-cost FPGA on the market. Support for I/O standards including LVDS allows Cyclone devices to fit into a wide variety of applications. Taking advantage of these I/O standards and Cyclone pricing allows you to lower your design costs while remaining on the cutting edge of technology.

Document Revision History

Table 9–10 shows the revision history for this document.

Table 9–10. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
January 2007 v1.5	Added document revision history.	
August 2005 v1.4	Updated minimum LVDS LOD value listed in Table 9-2.	
February 2005 v1.3	Minor updates.	
October 2003 v1.2	• Added RSDS information. • Removed V_{SS} from Figure 9–5. • Added RSDS and LVDS timing information in Tables 9–6 and 9–7, respectively. • Updated Implementing Cyclone LVDS & RSDS I/O Pins in the Quartus II Software section, including addition of the PLL Circuit section.	
September 2003 v1.1	Updated LVDS data rates to 640 Mbps from 311 Mbps.	
May 2003 v1.0	Added document to Cyclone Device Handbook.	