LTspice Version

Clock Controlled Unipolar Stepping Motor Driver

TB67S149FTG (Device Modeling Report)

MARUTSU ELEC CO.,LTD.
http://www.marutsu.co.jp/pc/i/593537/

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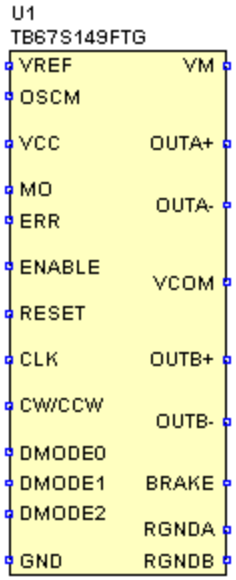
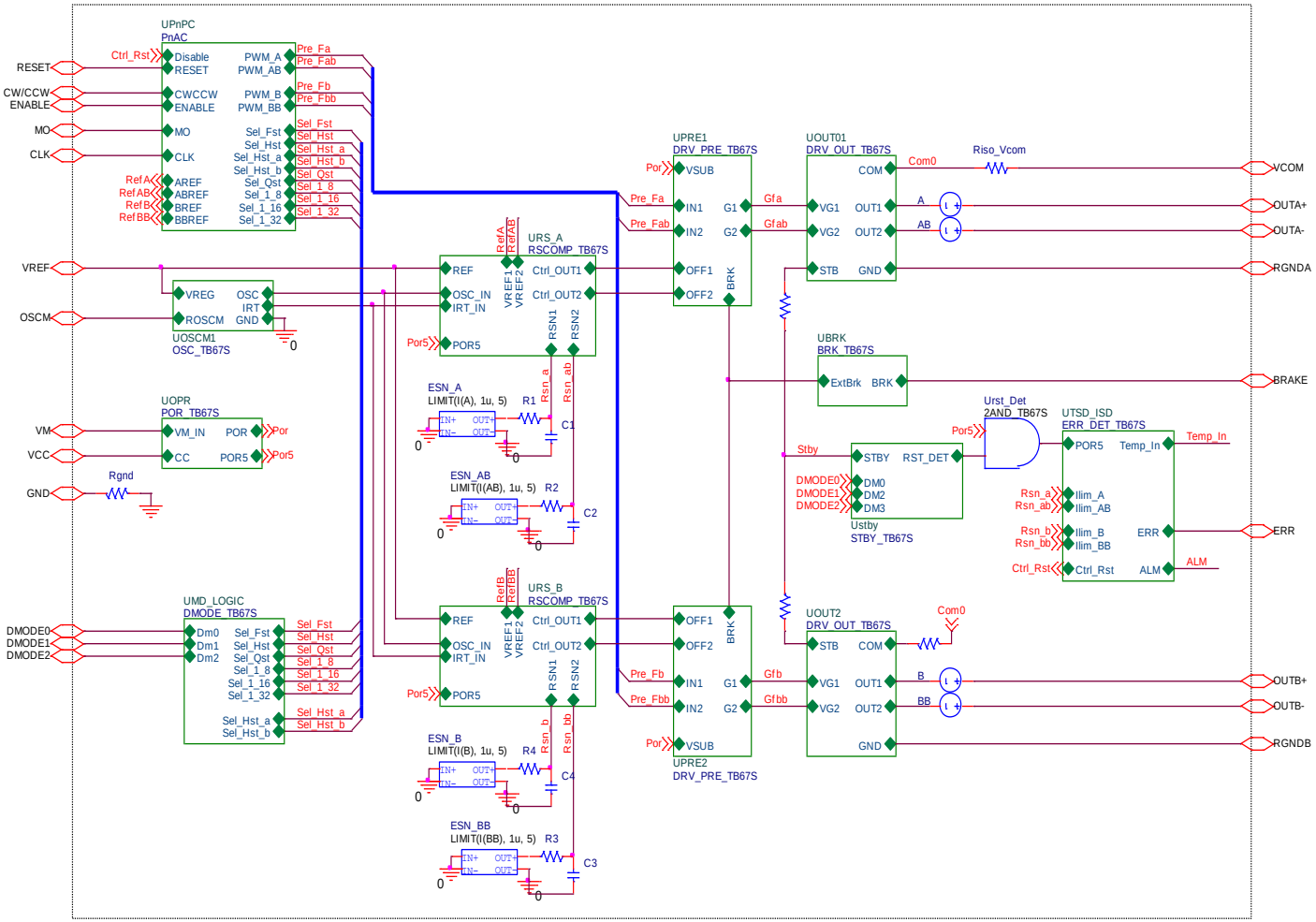
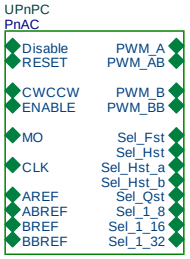
TB67S149FTG (Equivalent Circuit)

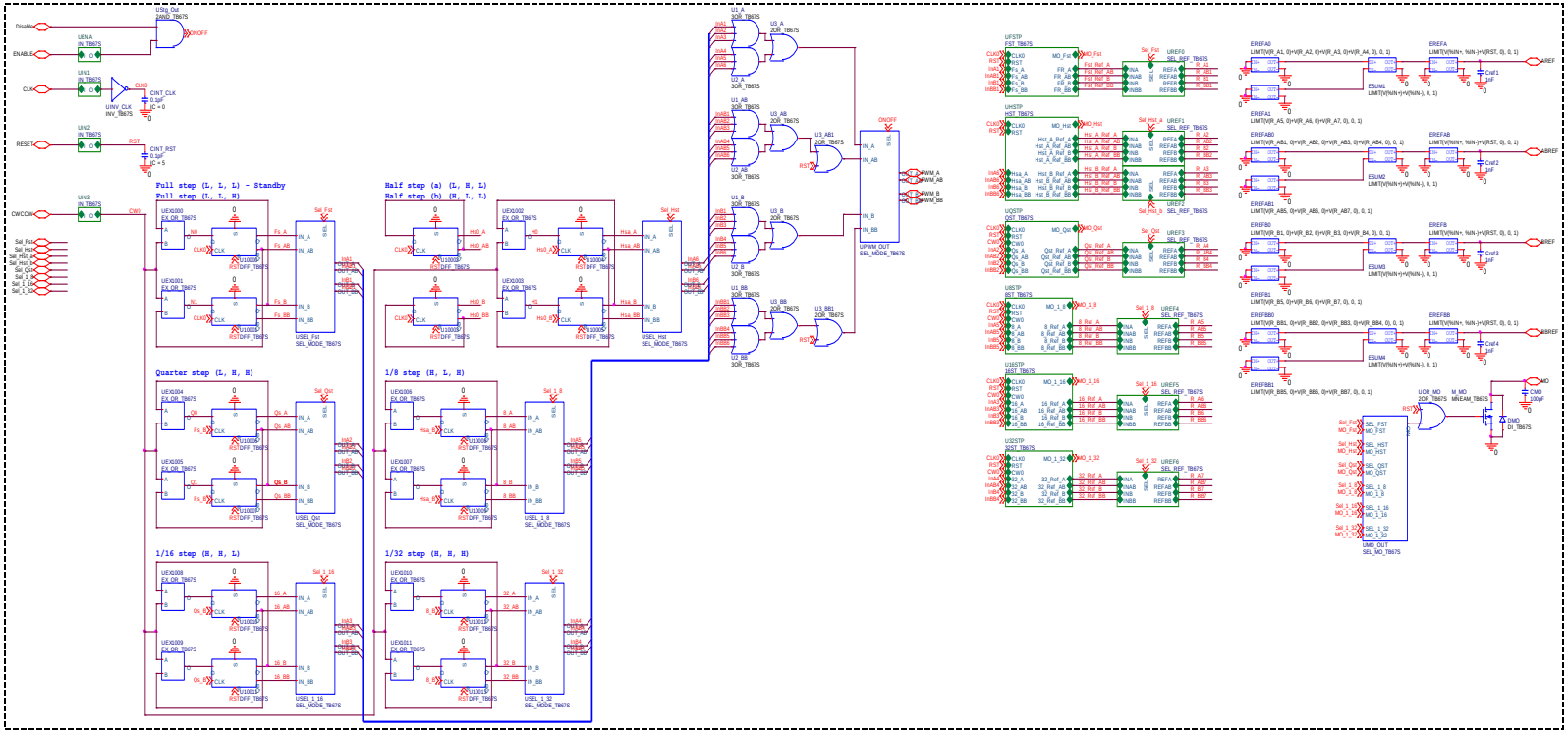


Pin Configuration

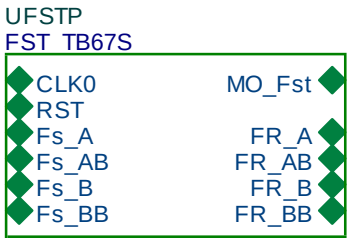


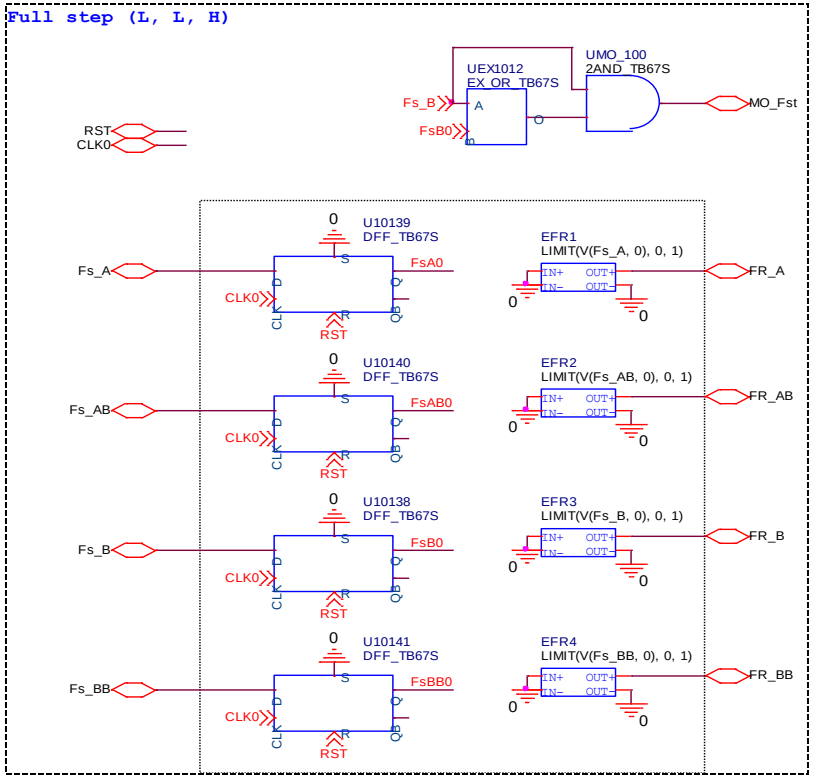
UPnPC Block (Equivalent Circuit)





UPnPC-UFSTP Block (Equivalent Circuit)





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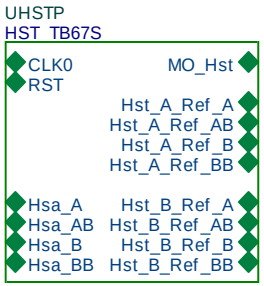
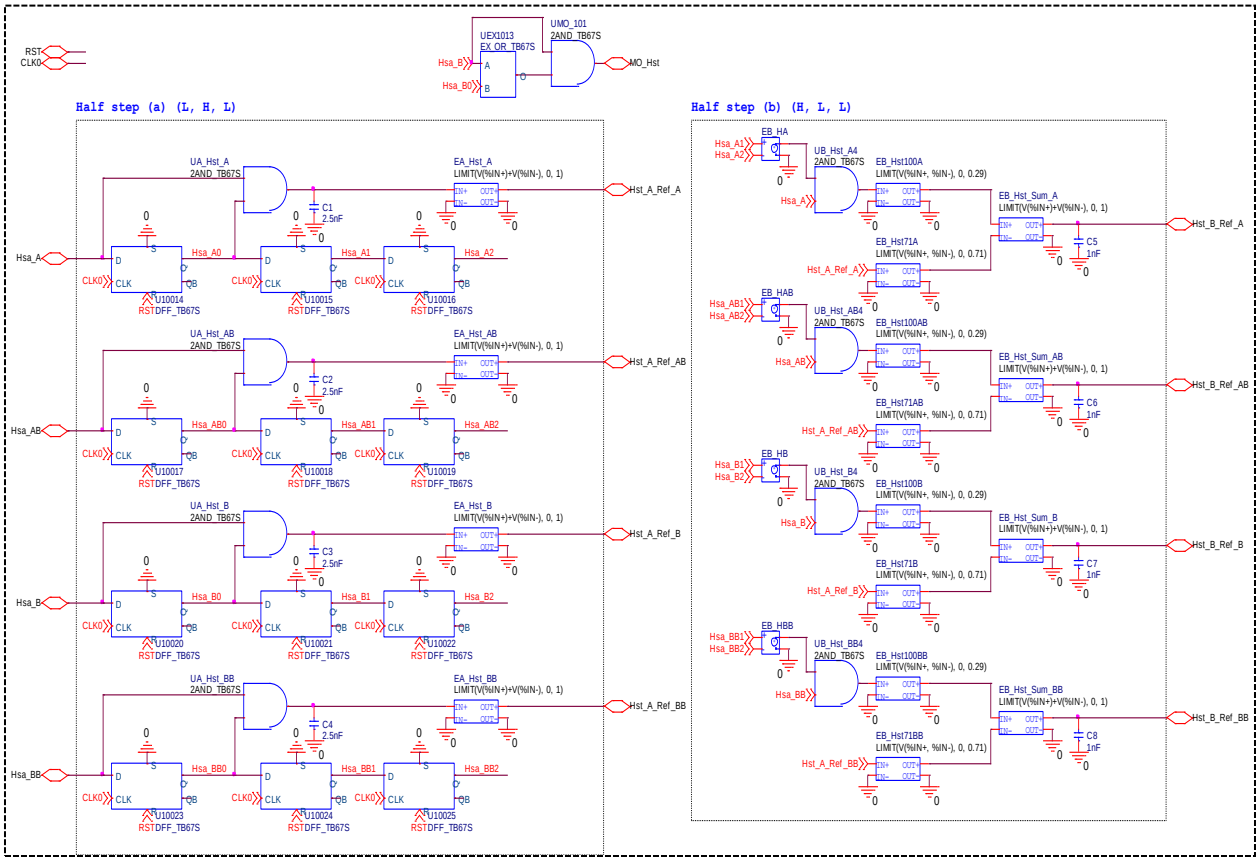
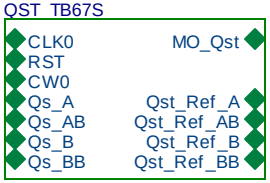
UPnPC-UHSTP Block (Equivalent Circuit)

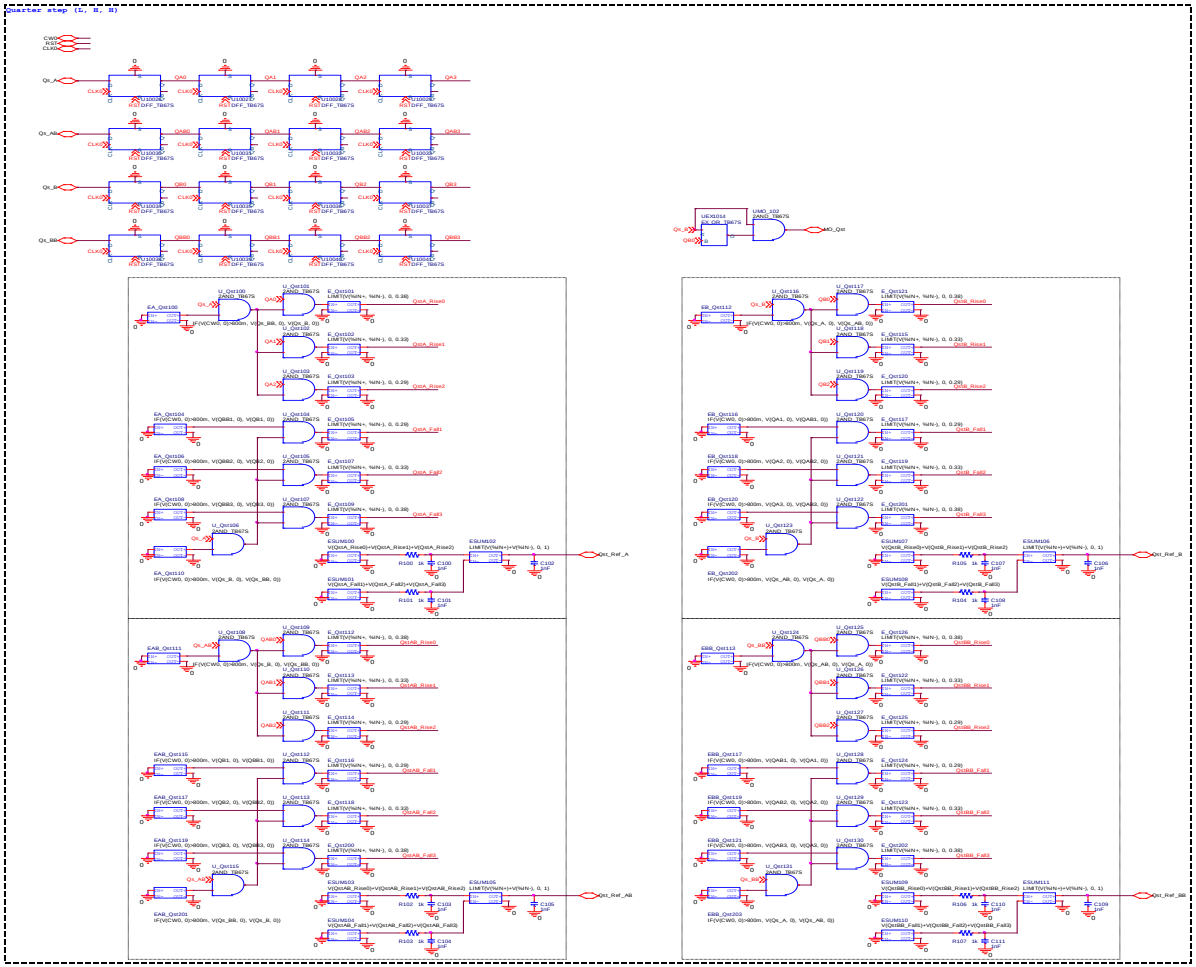




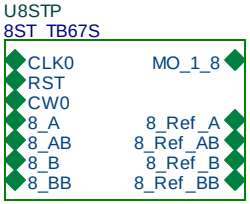
UPnPC-UQSTP Block (Equivalent Circuit)

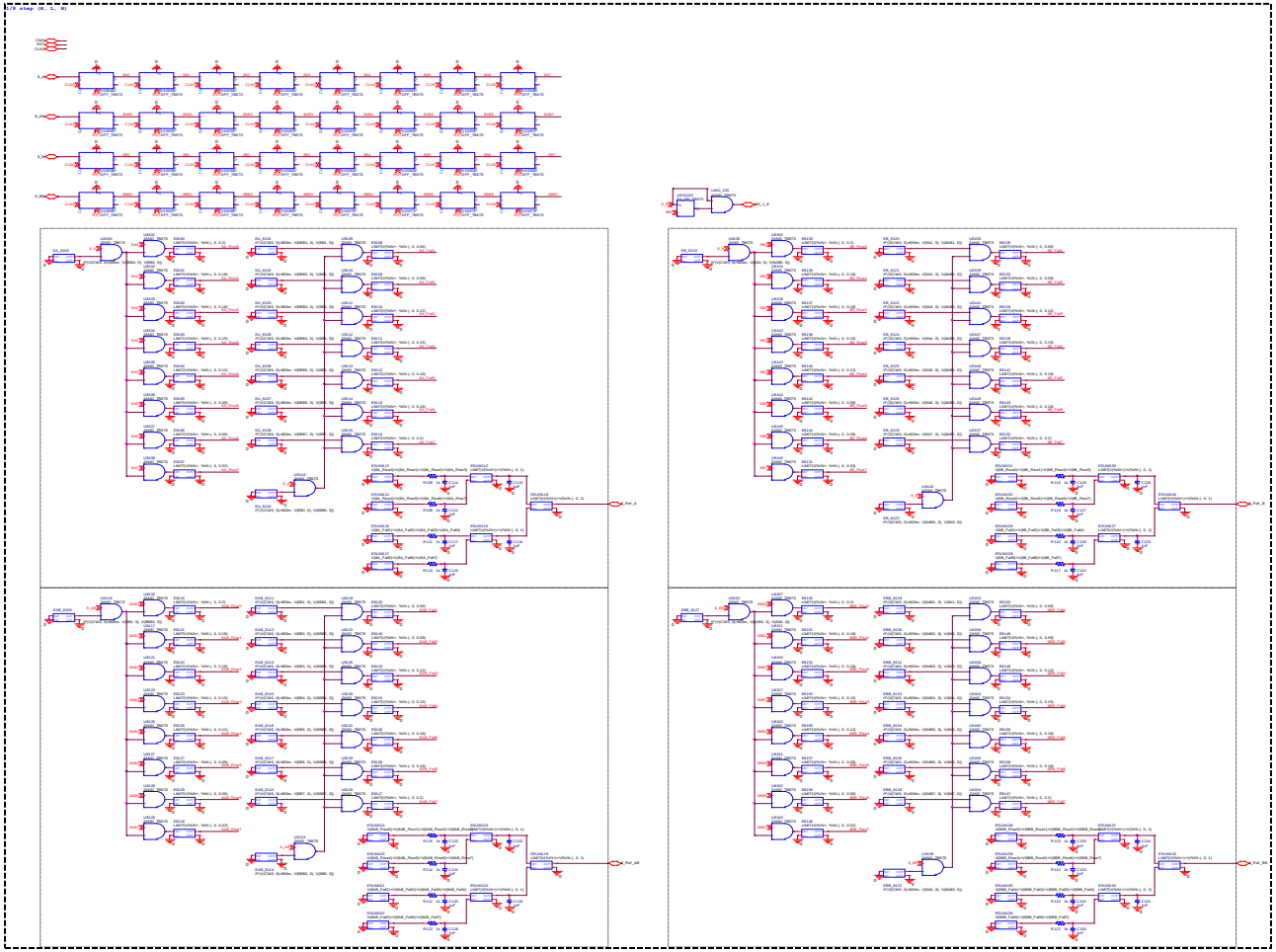
UQSTP
QST_TB67S



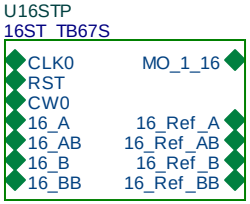


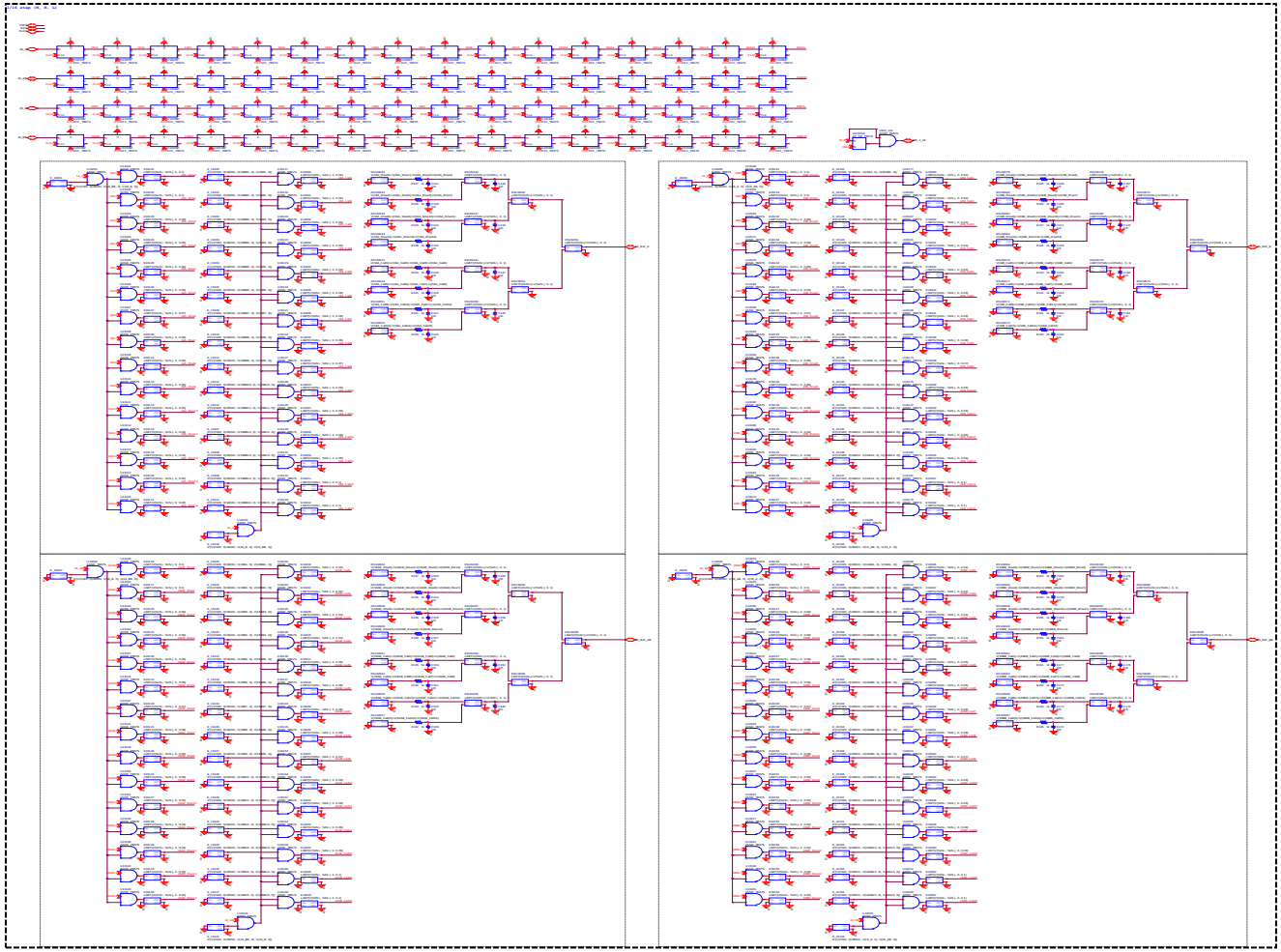
UPnPC-U8STP Block (Equivalent Circuit)



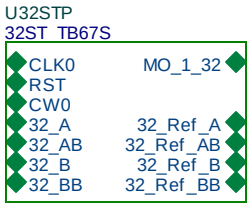


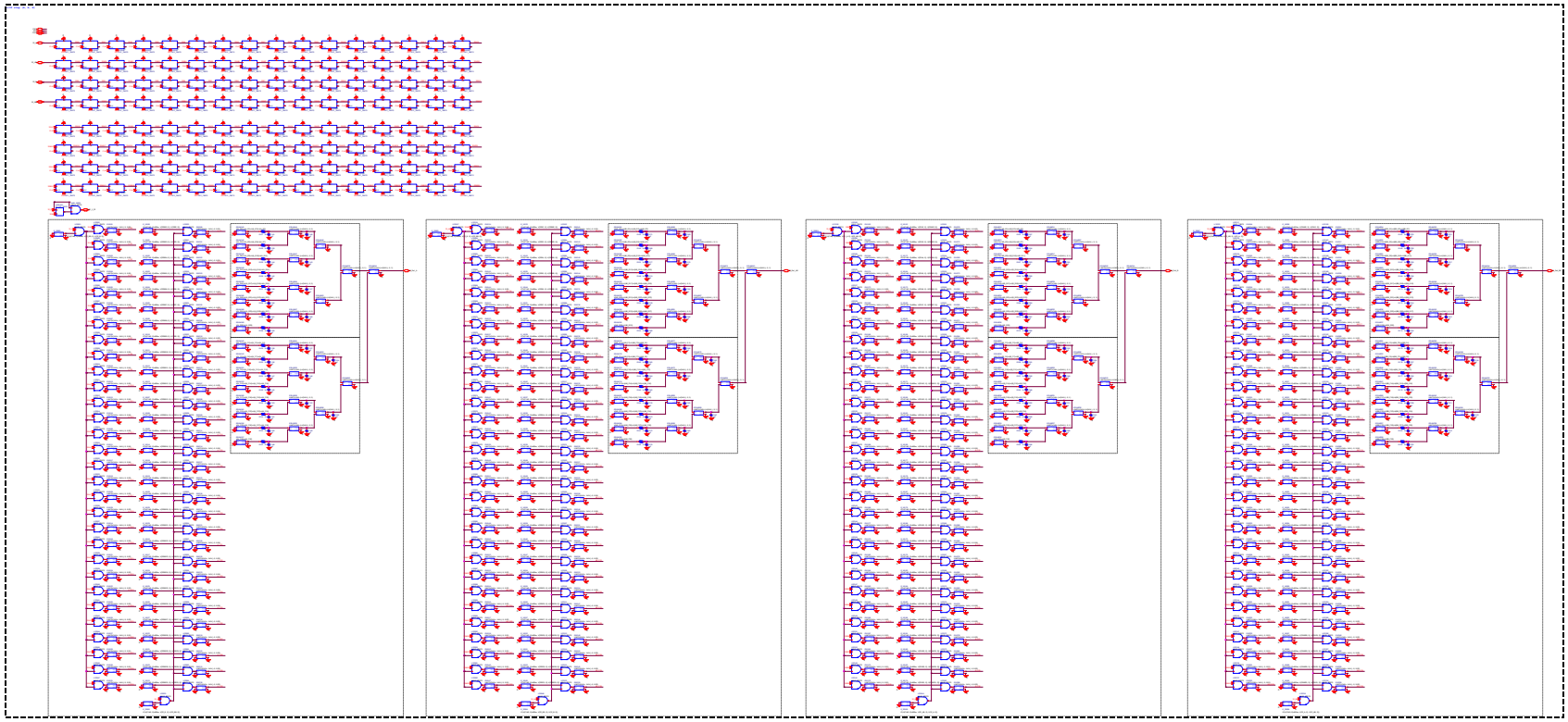
UPnPC-U16STP Block (Equivalent Circuit)





UPnPC-U32STP Block (Equivalent Circuit)





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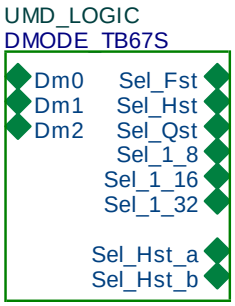
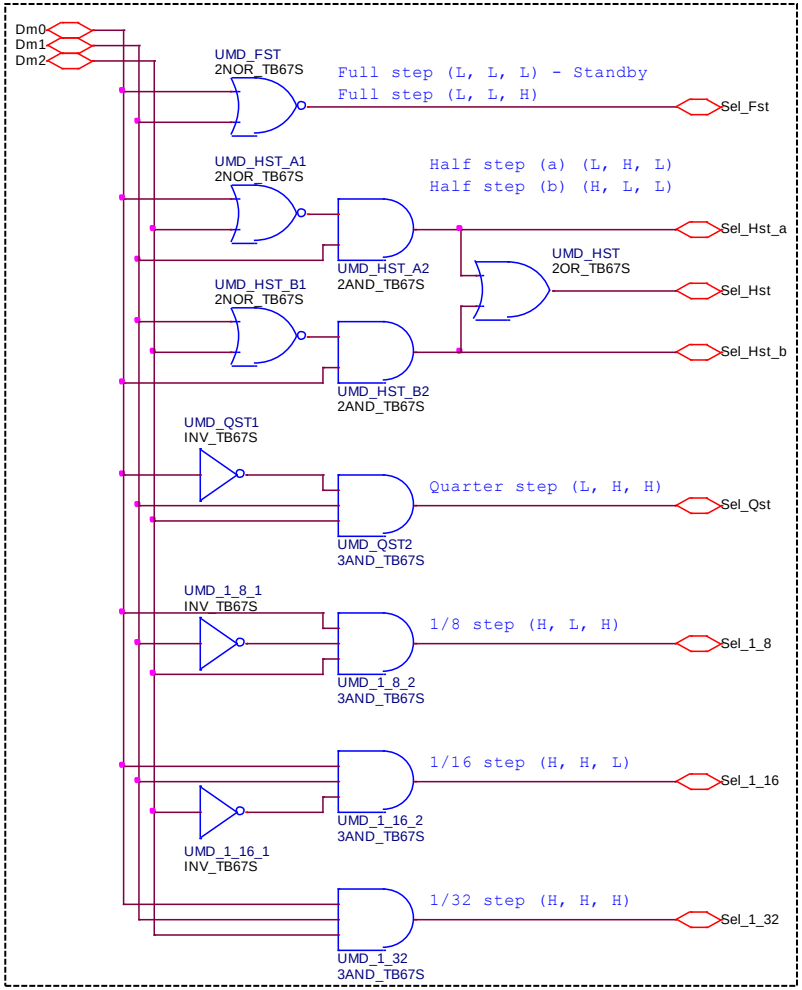
UMD_LOGIC Block (Equivalent Circuit)





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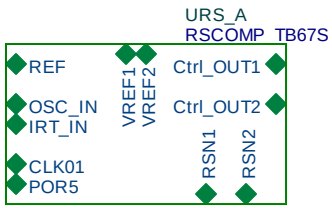
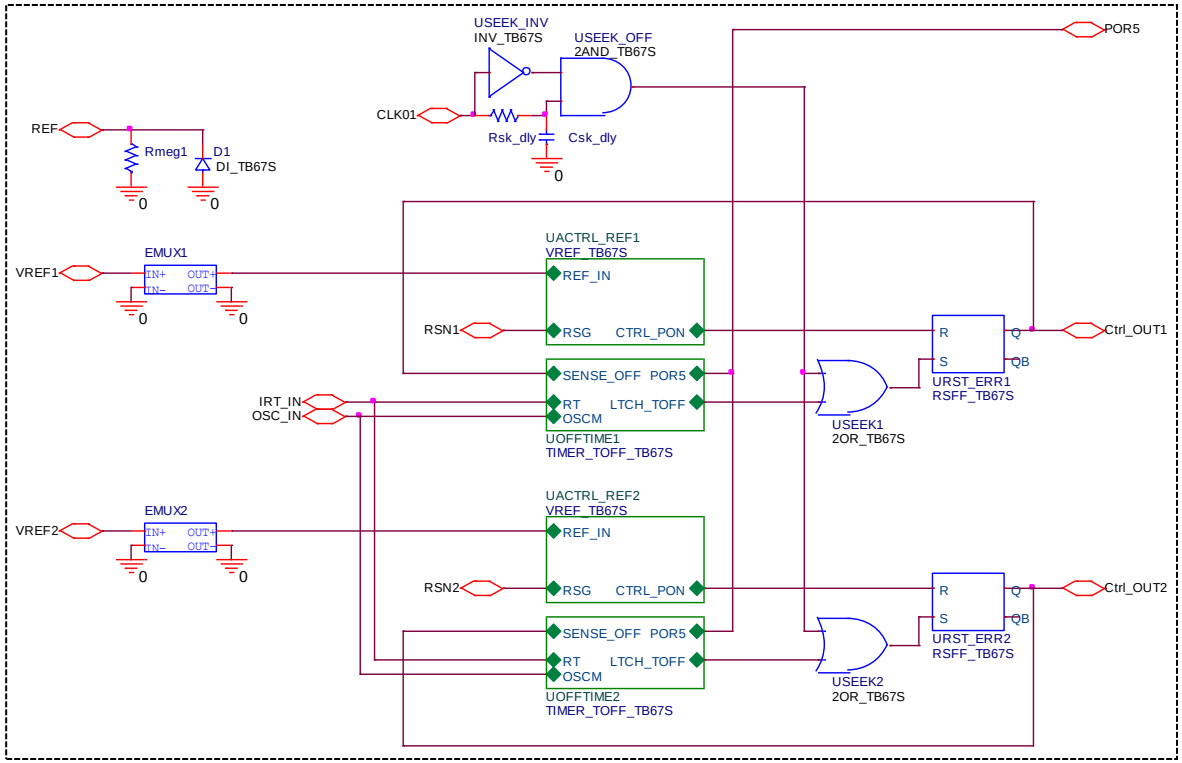
URS_A, URS_B Block (Equivalent Circuit)





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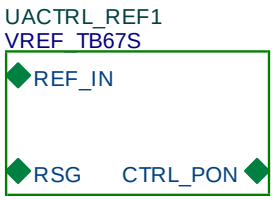
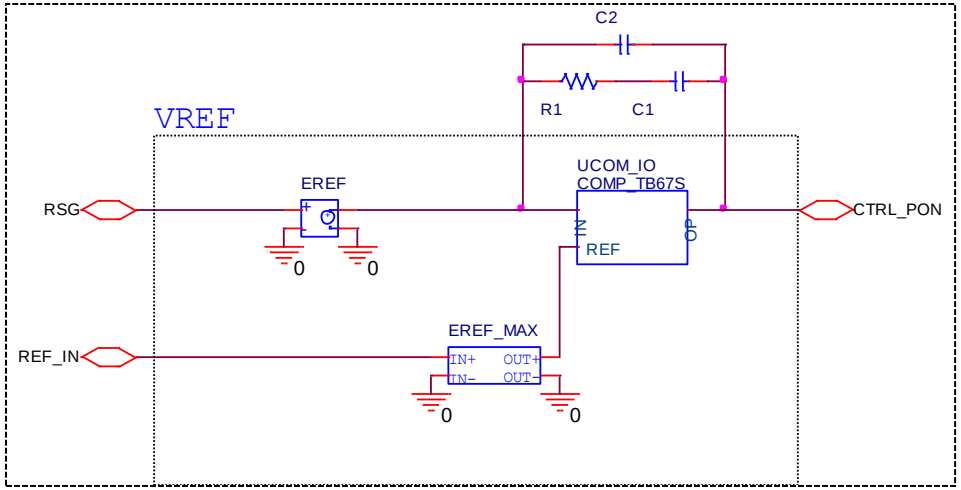
URS_A, URS_B-UACTRL_REF1, 2 Block (Equivalent Circuit)





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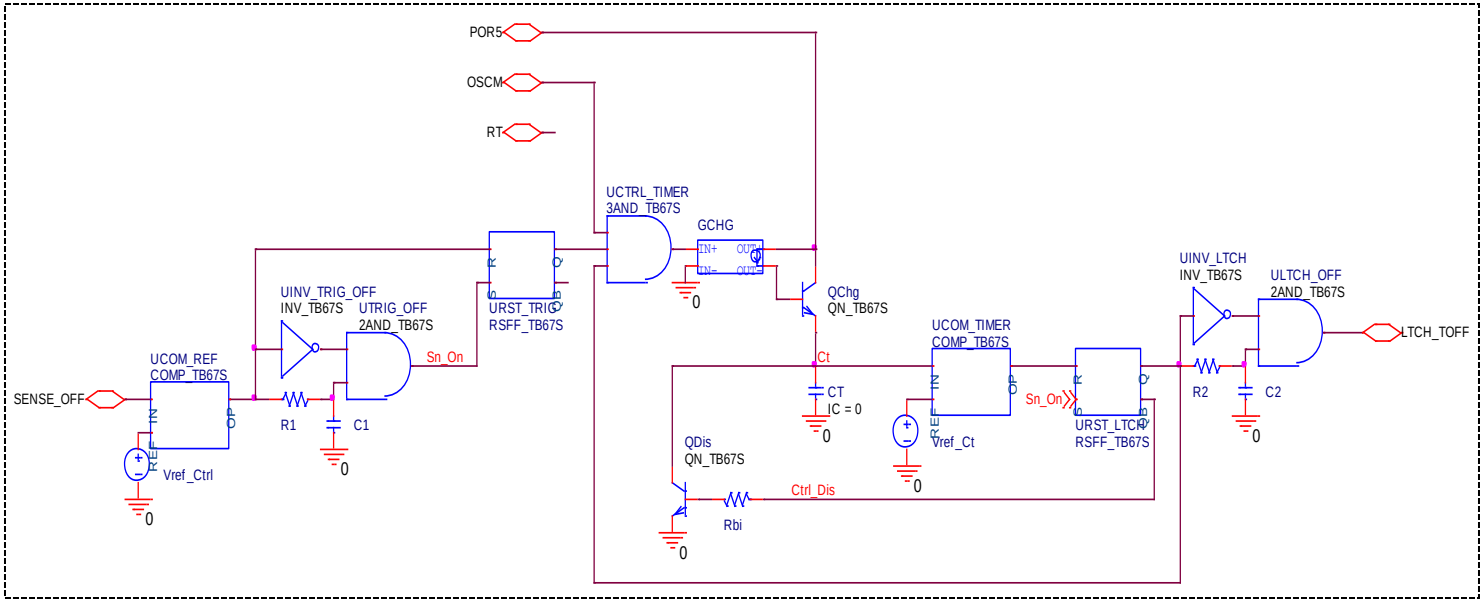
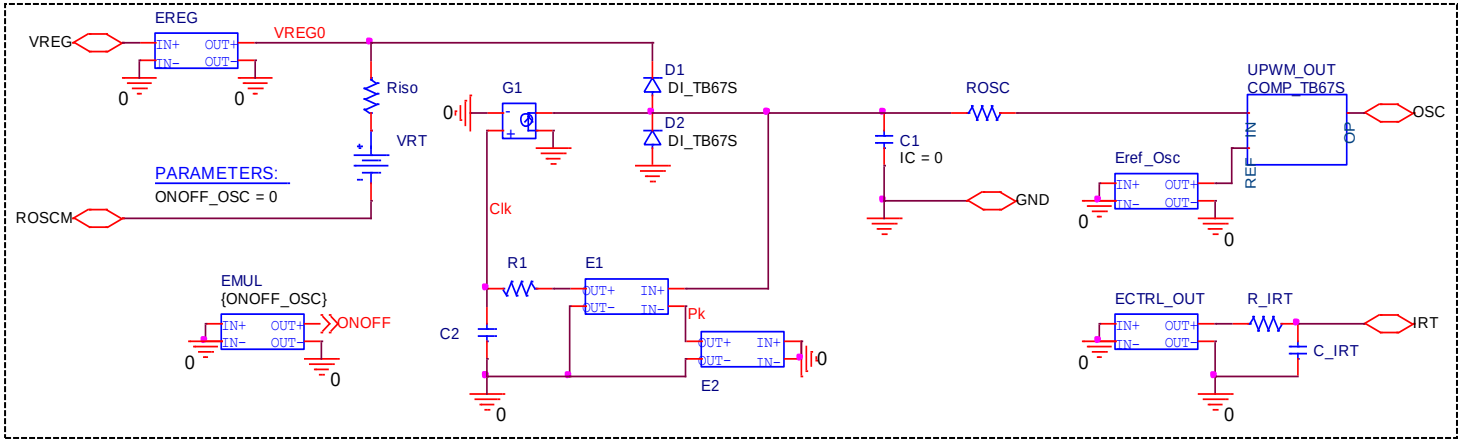
URS_A, URS_B-UOFFTIME1, 2 Block (Equivalent Circuit)

UOFFTIME1
TIMER_TOFF_TB67S

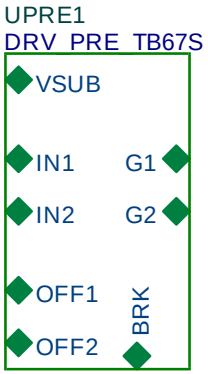


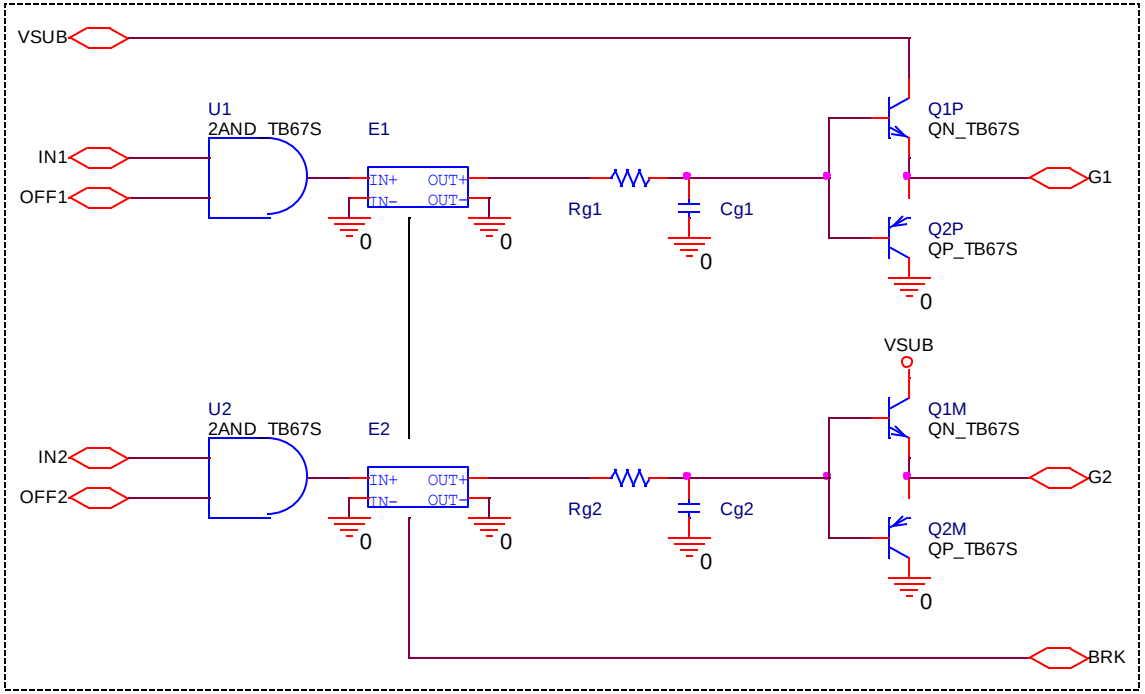
UOSCM1 Block (Equivalent Circuit)

UOSCM1
OSC_TB67S



UPRE1, 2 Block (Equivalent Circuit)





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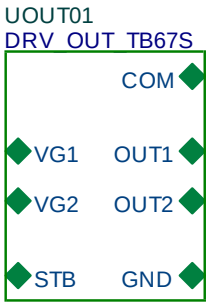
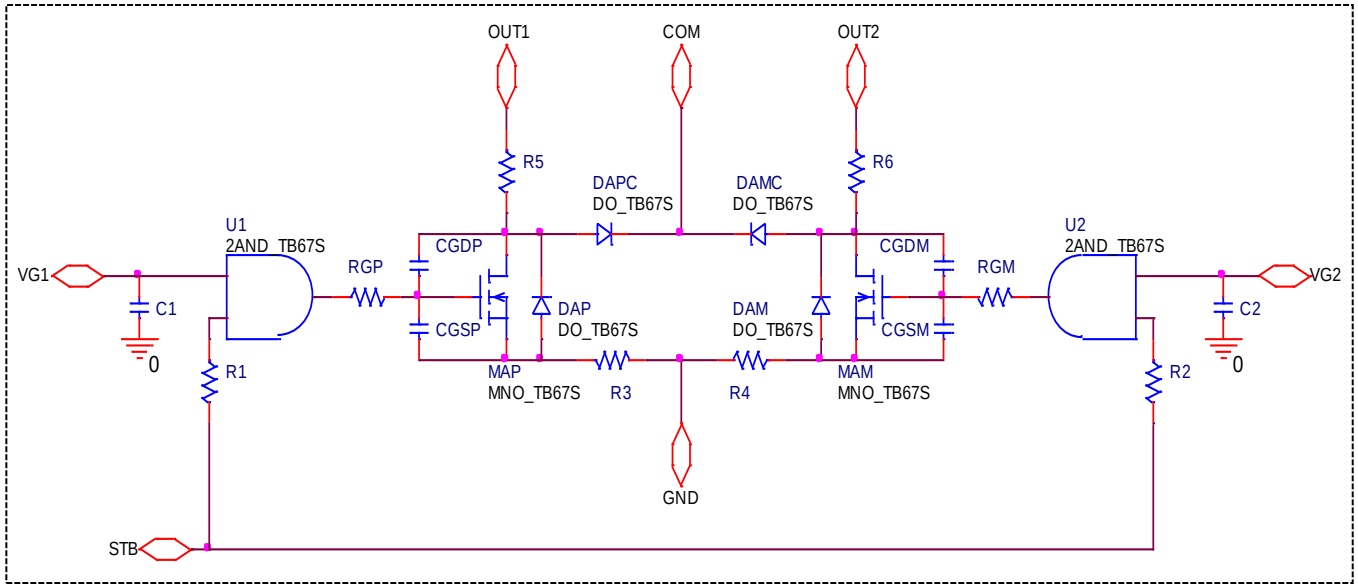
UOUT1, 2 Block (Equivalent Circuit)





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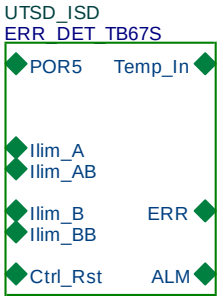
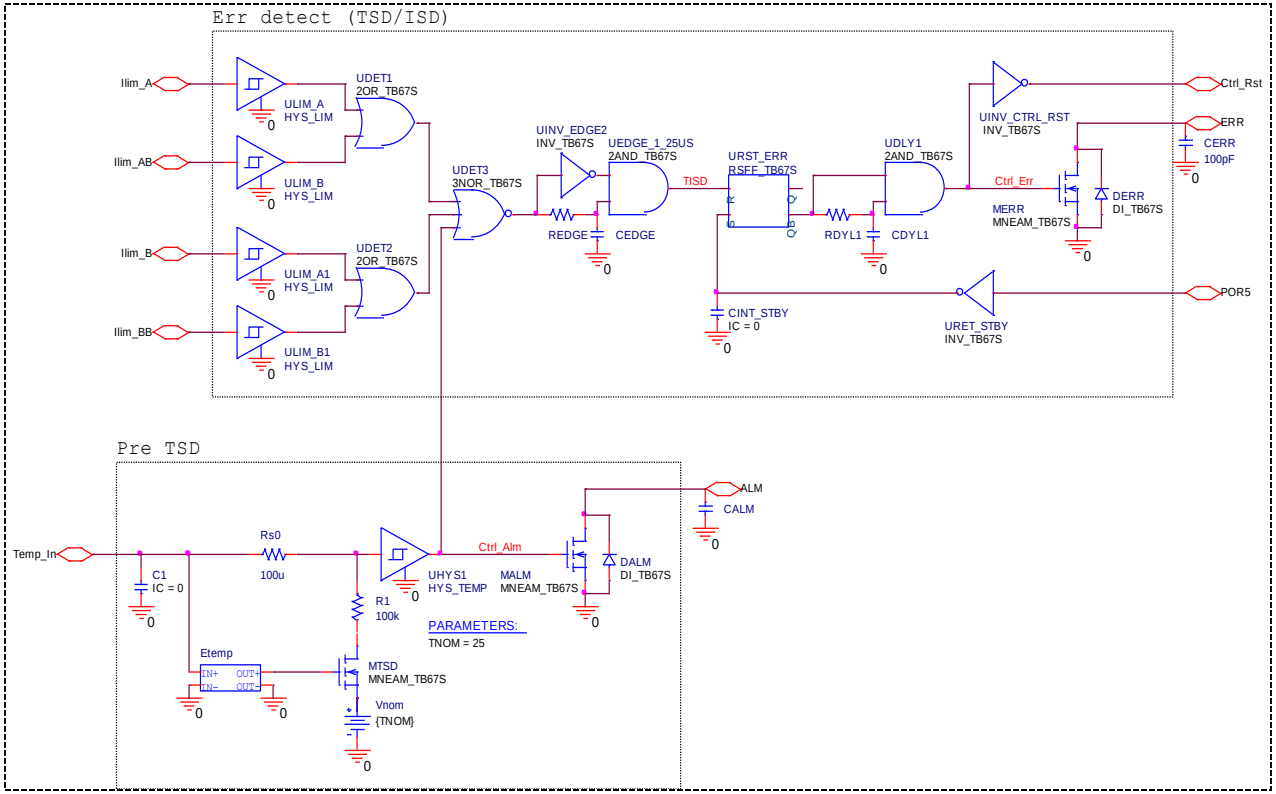
UTSD_ISD Block (Equivalent Circuit)





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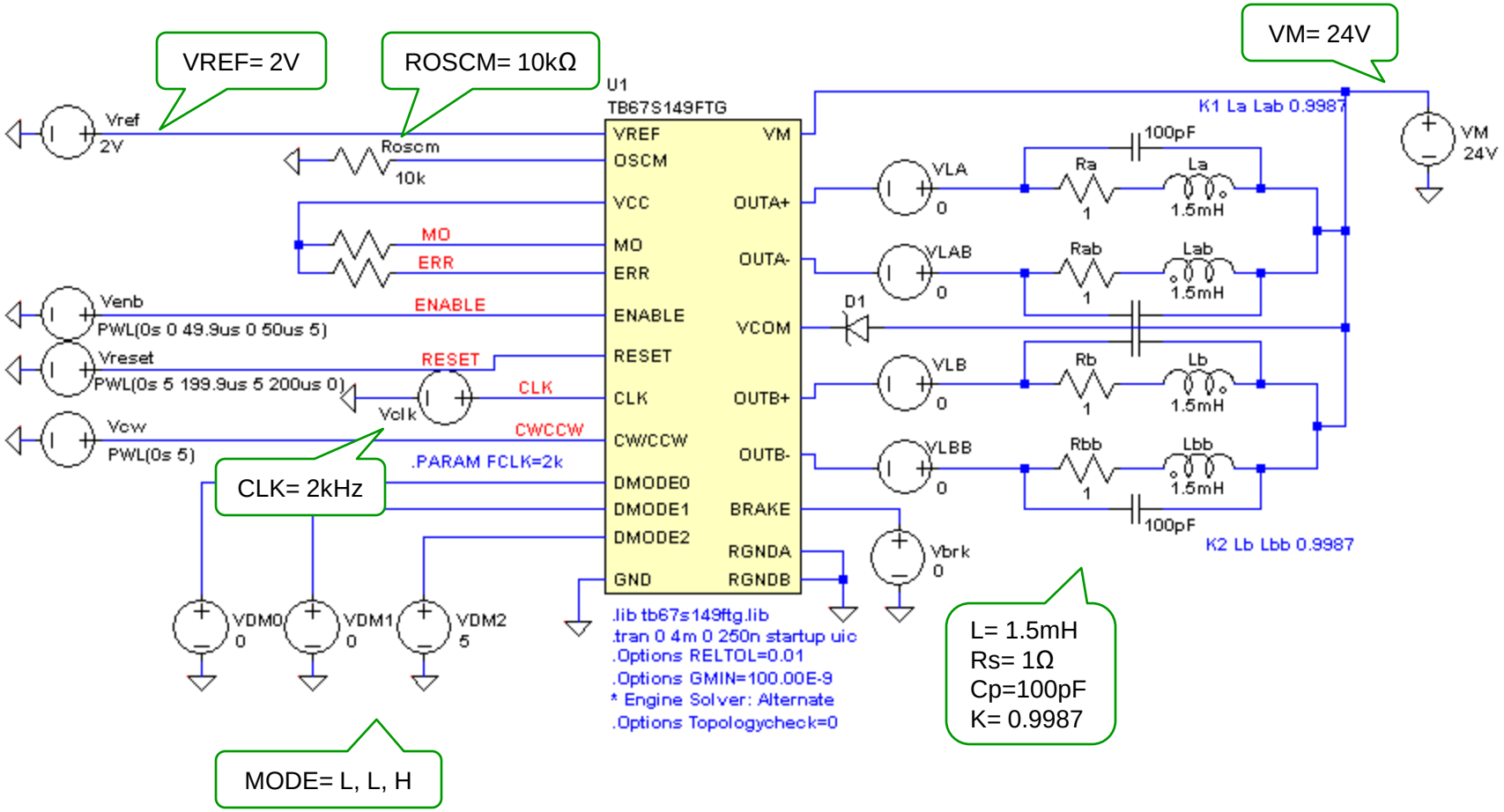
1) Full step (L, L, H)
- Simulation Circuit



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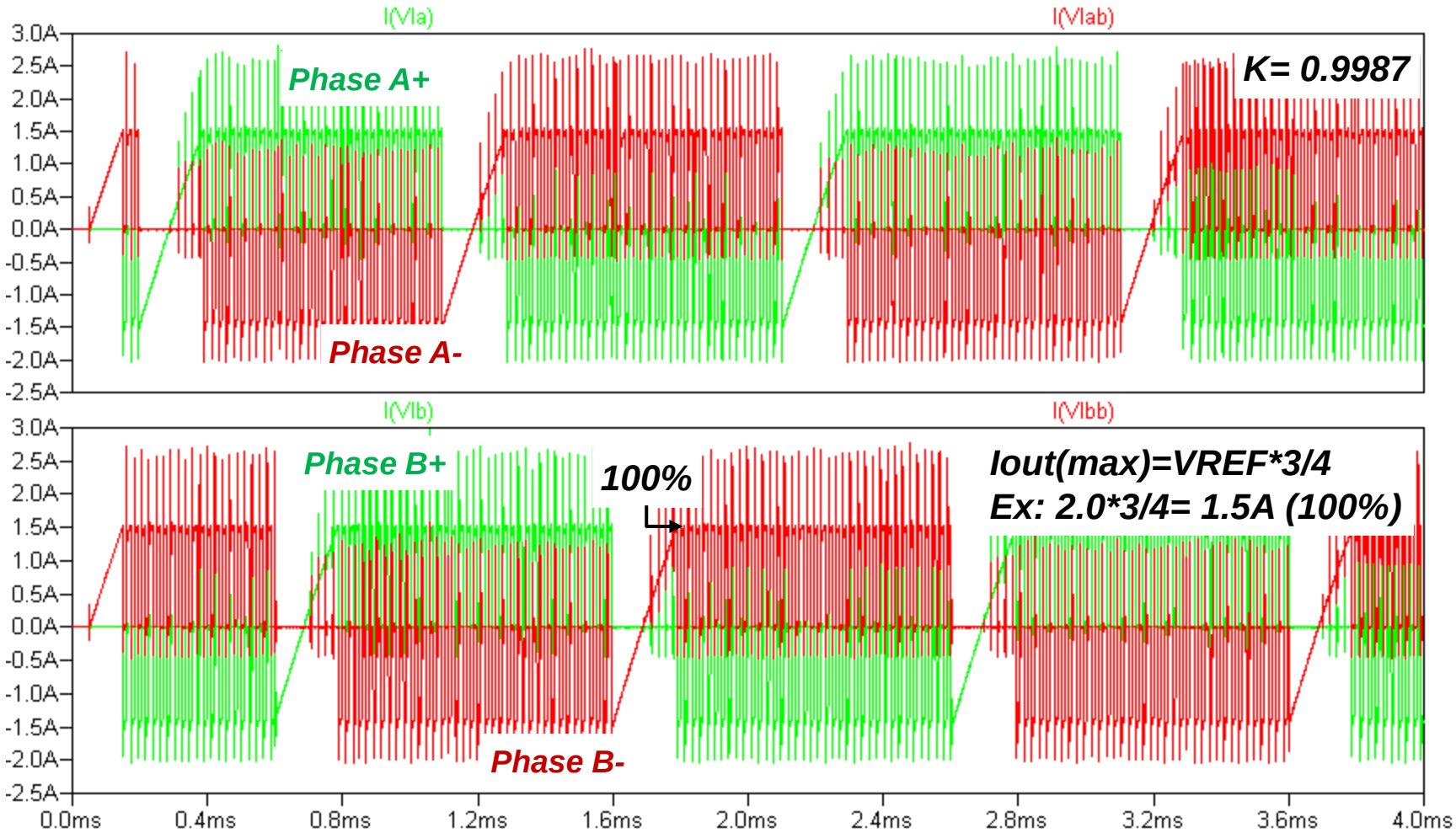
1) Full step (L, L, H)
- Simulation Result



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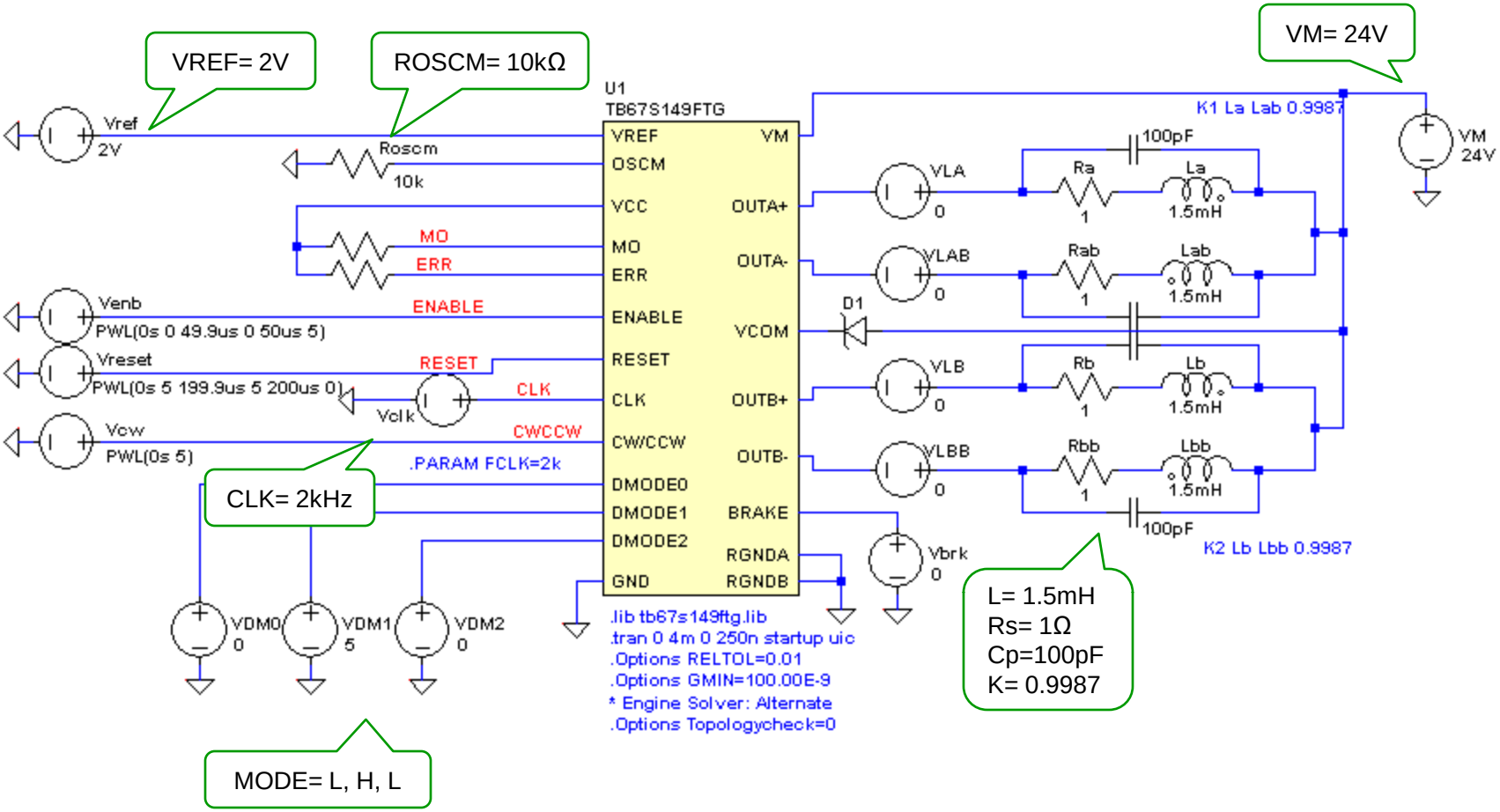
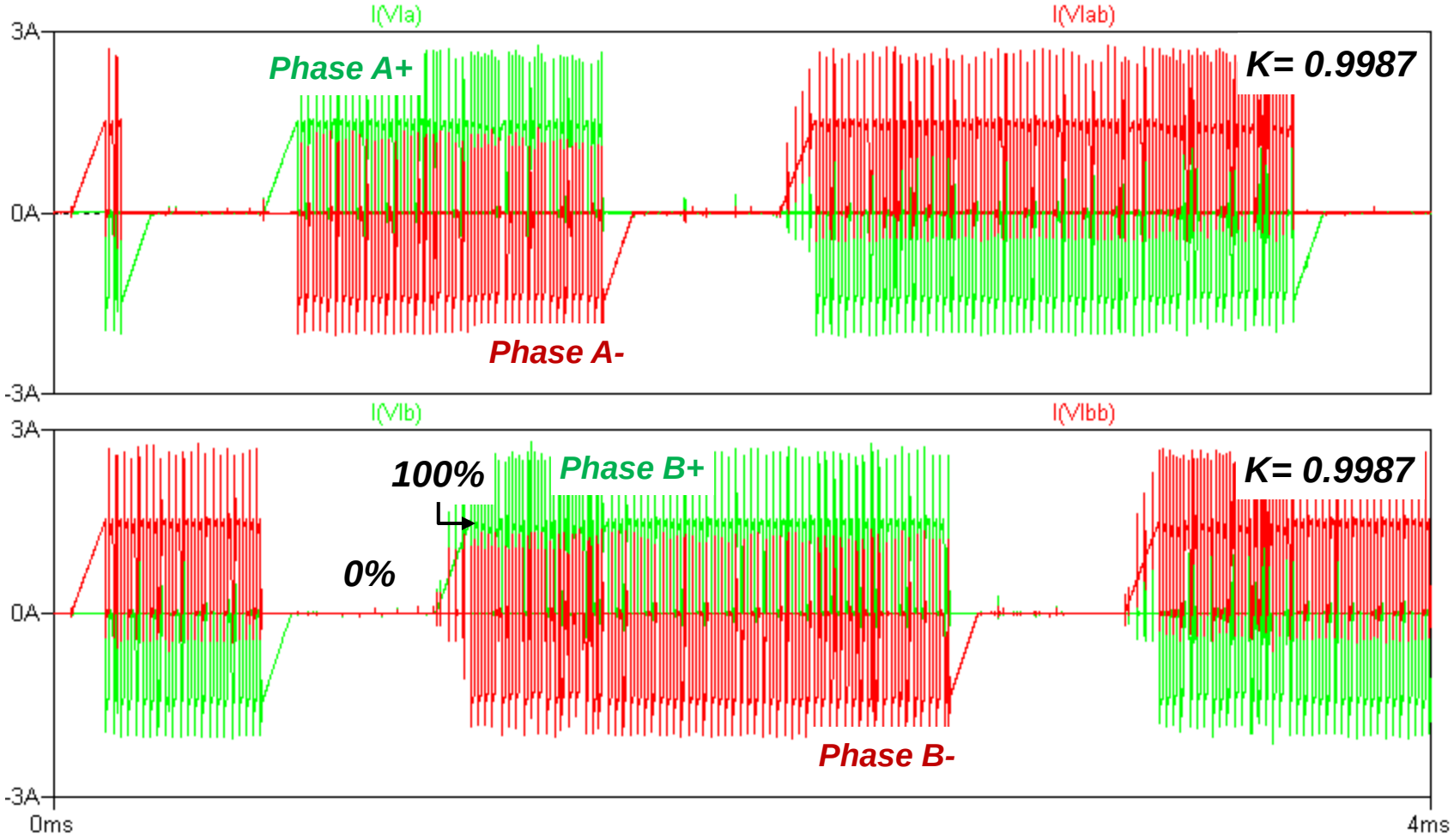
2) Half step (a) (L, H, L)
- Simulation Circuit



2) Half step (a) (L, H, L)
- Simulation Result



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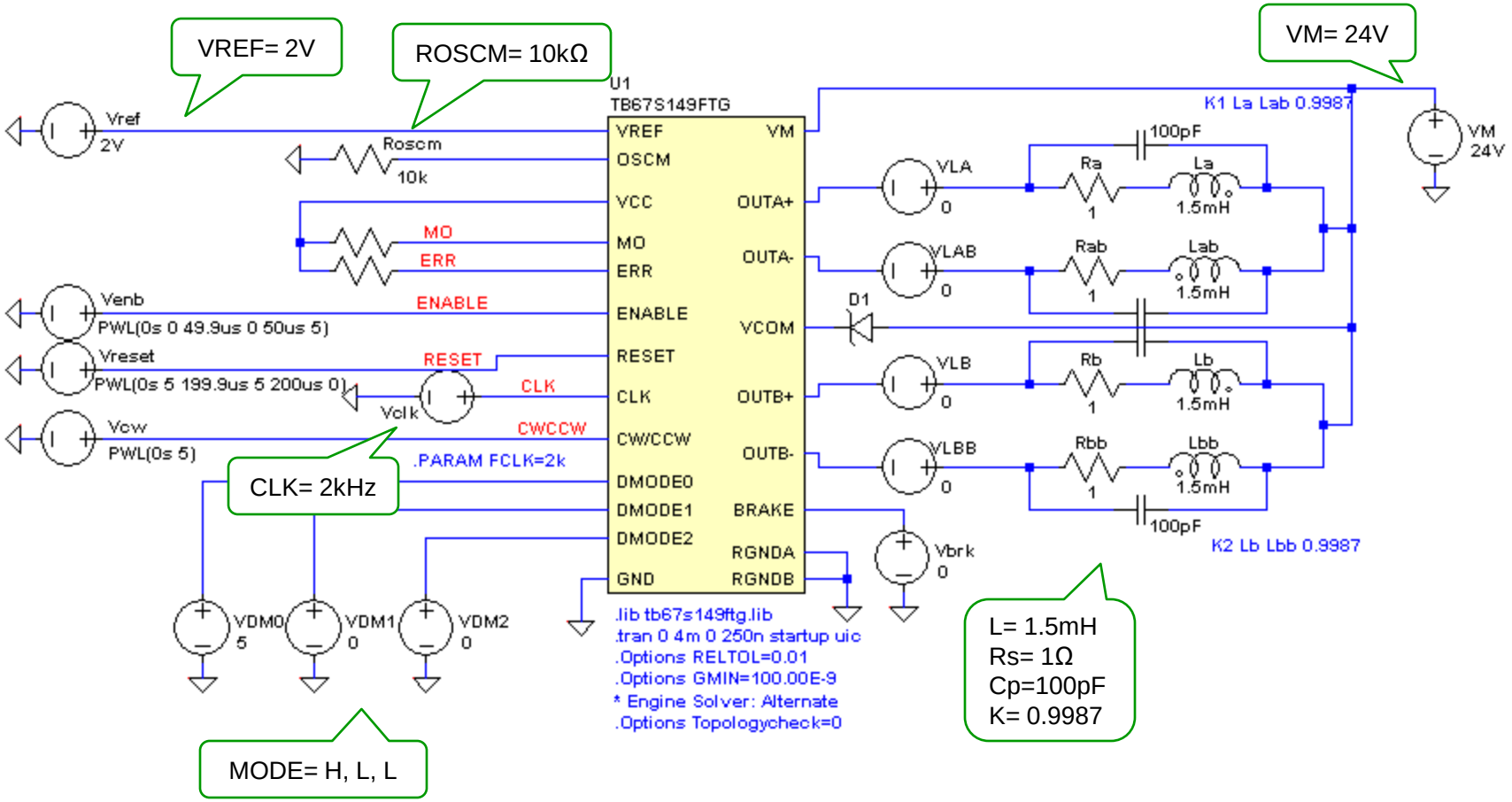
3) Half step (b) (H, L, L)
- Simulation Circuit



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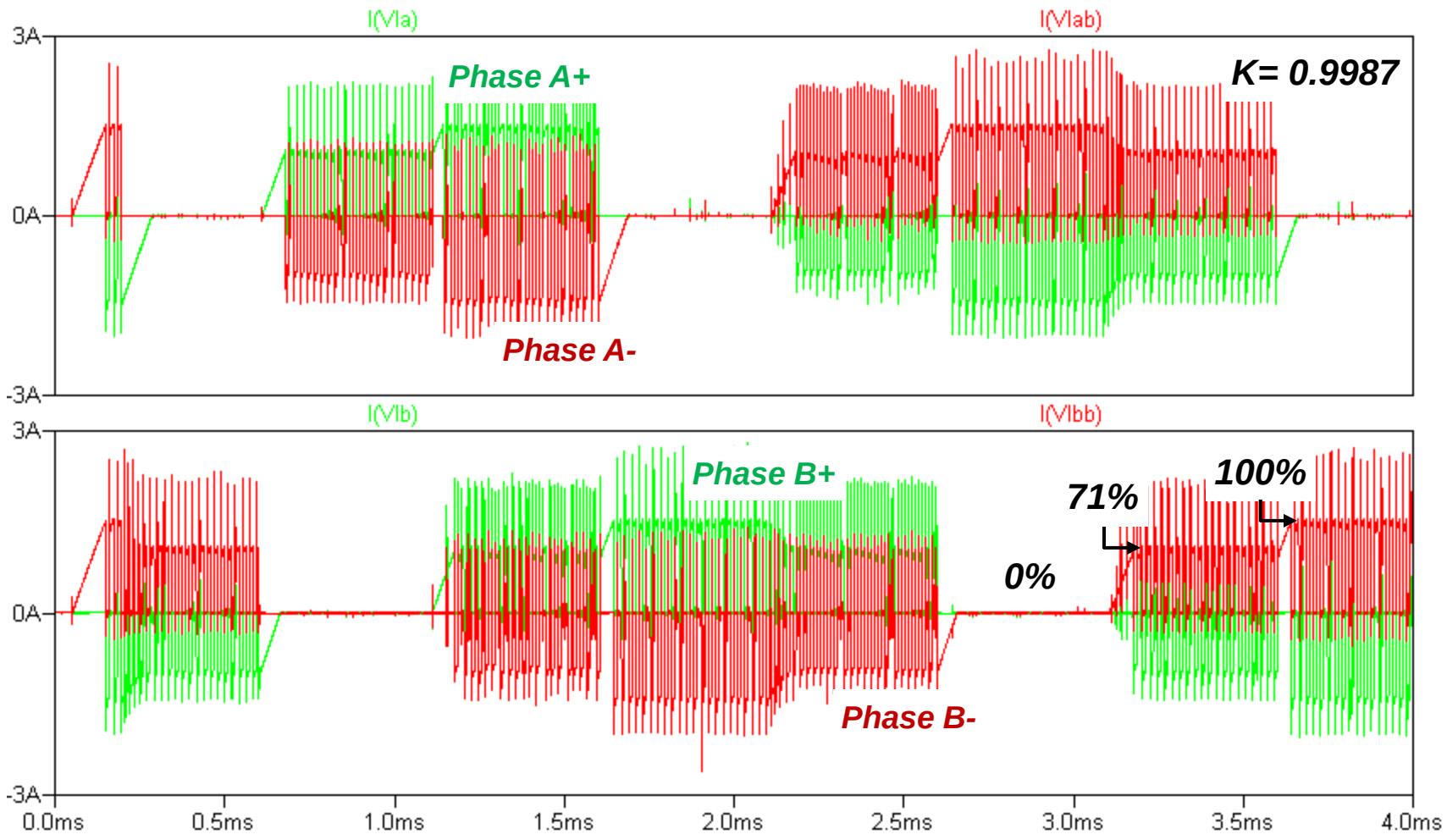
3) Half step (b) (H, L, L)
- Simulation Result



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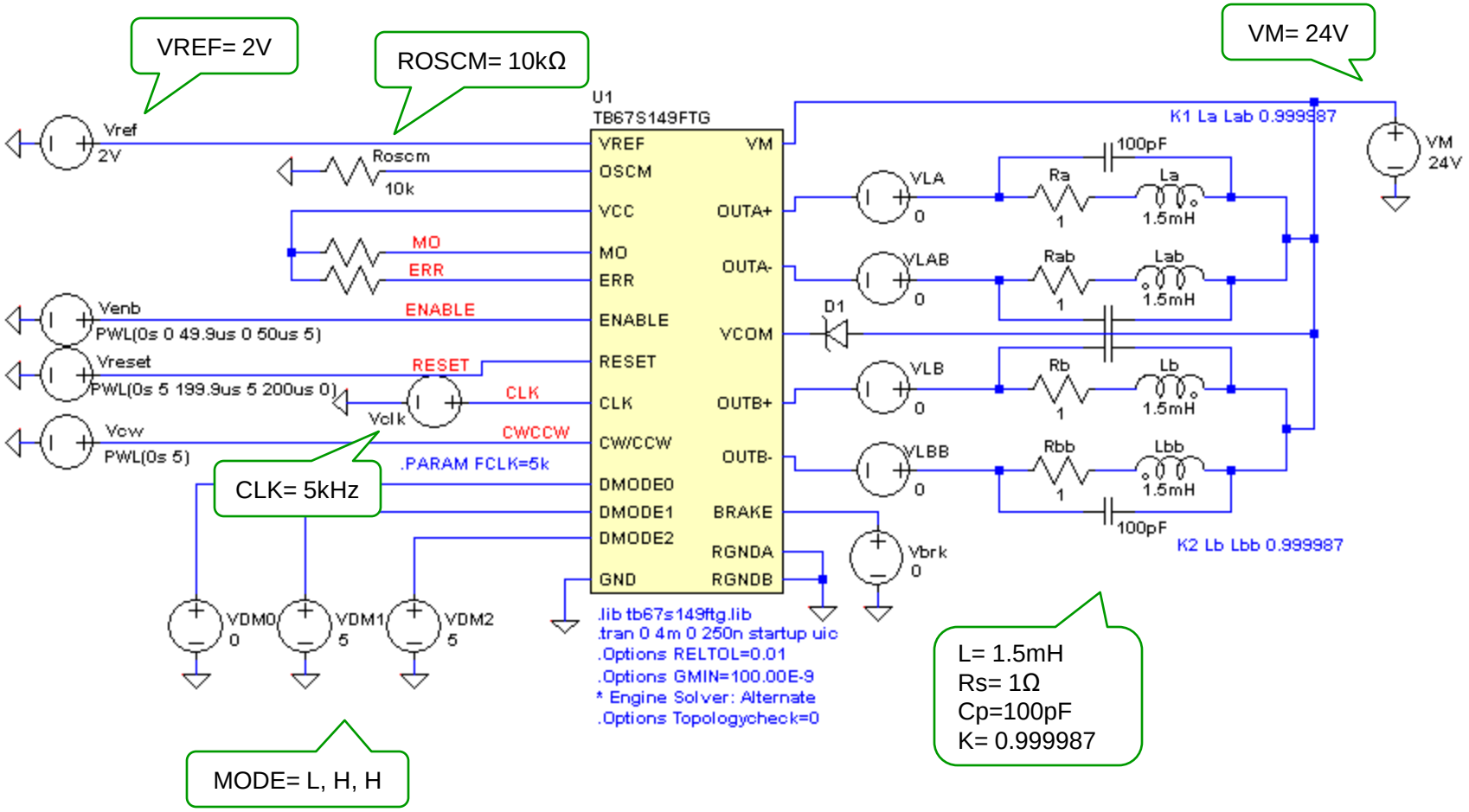
4) Quarter step (L, H, H)
- Simulation Circuit



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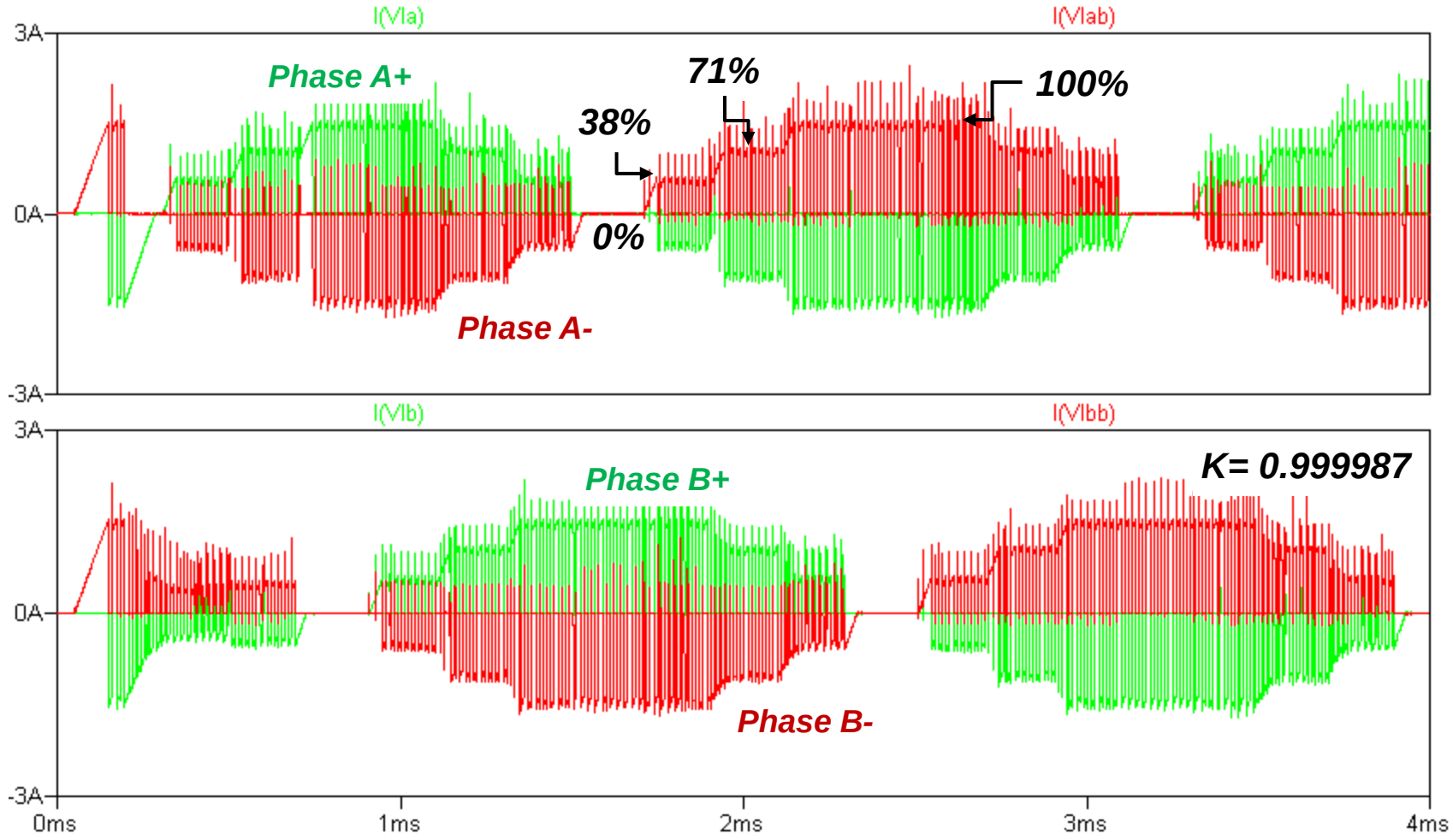
4) Quarter step (L, H, H)
- Simulation Result



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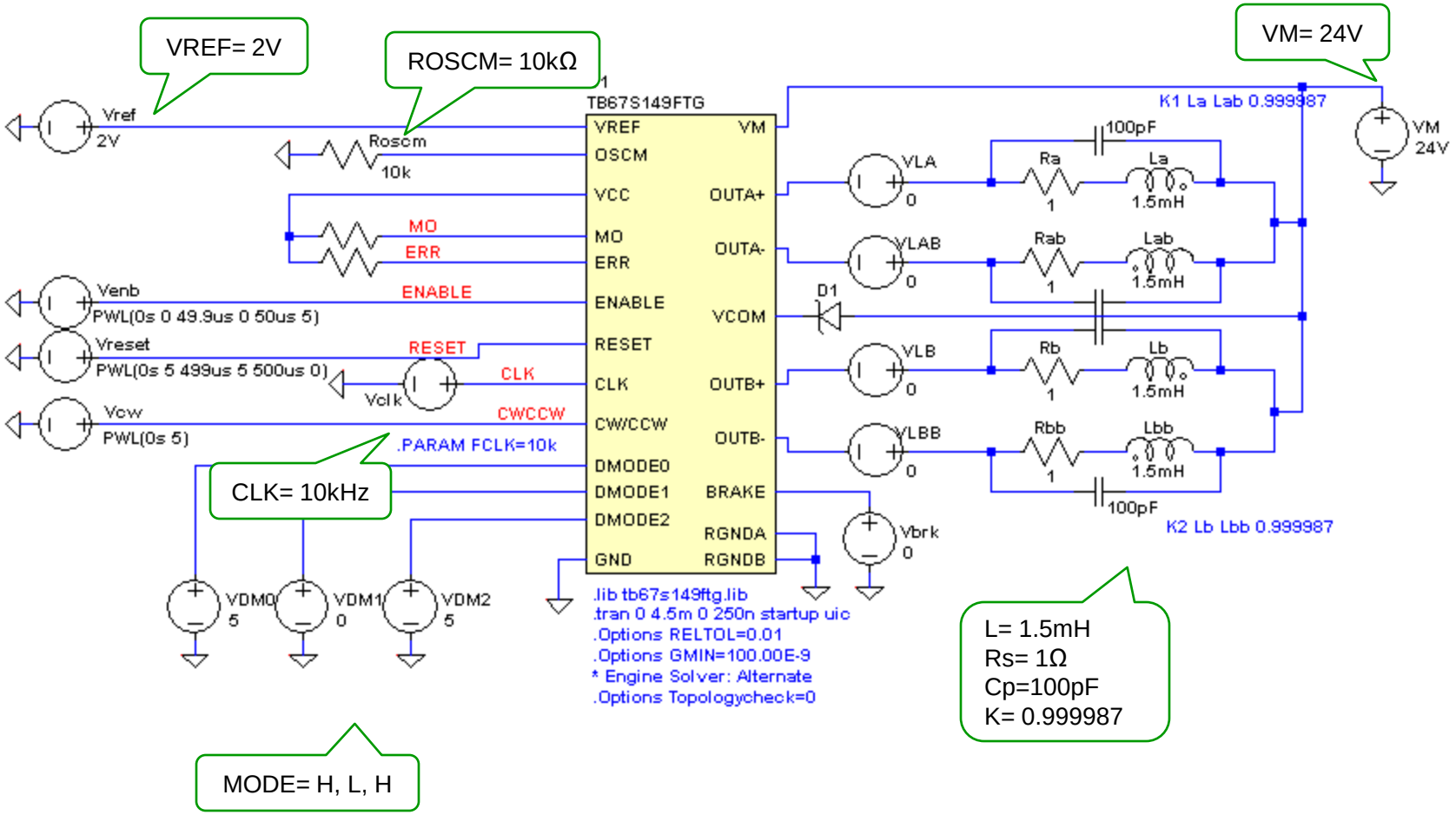
5) 1/8 step (H, L, H)
- Simulation Circuit



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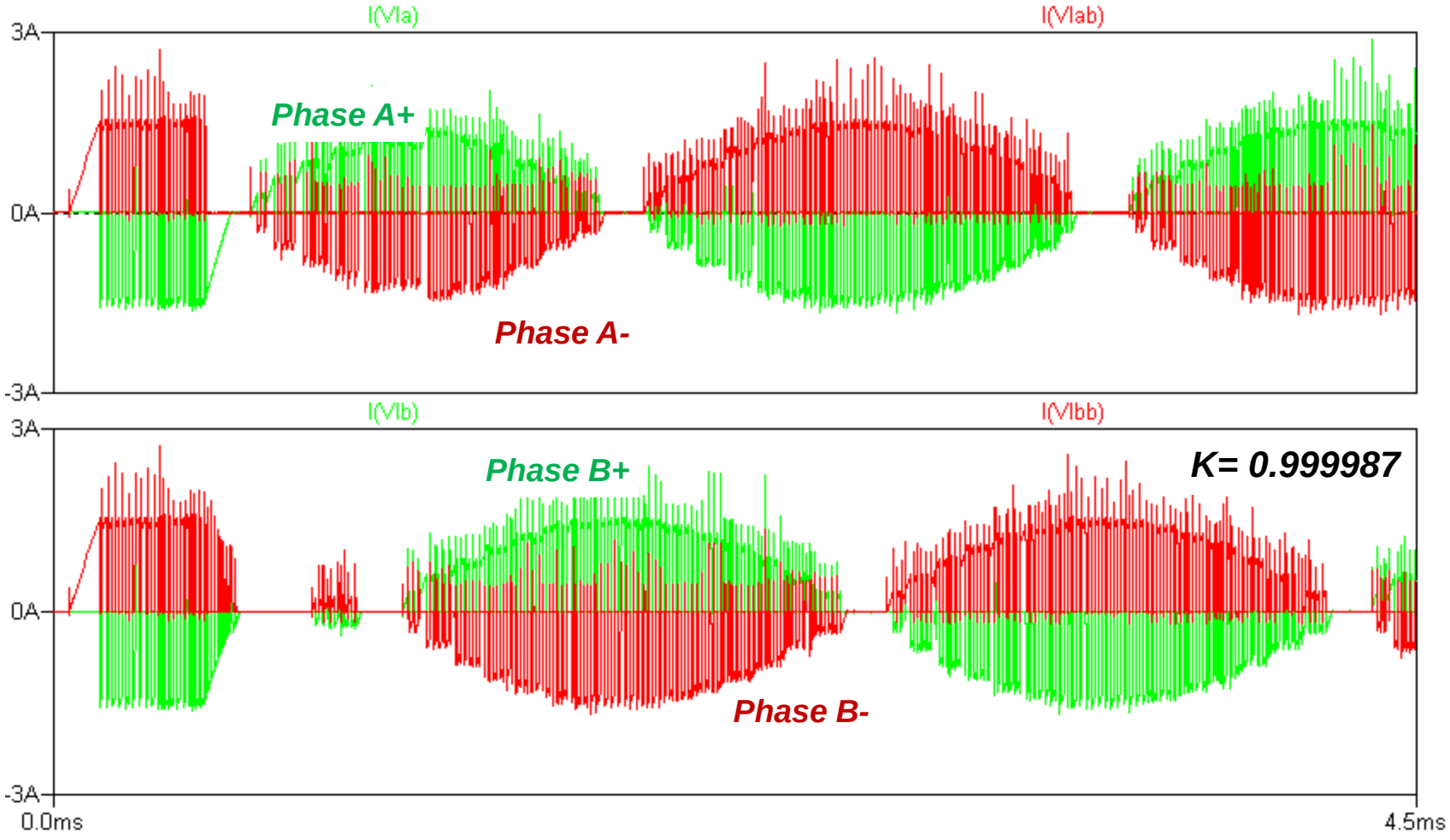
5) 1/8 step (H, L, H)
- Simulation Result



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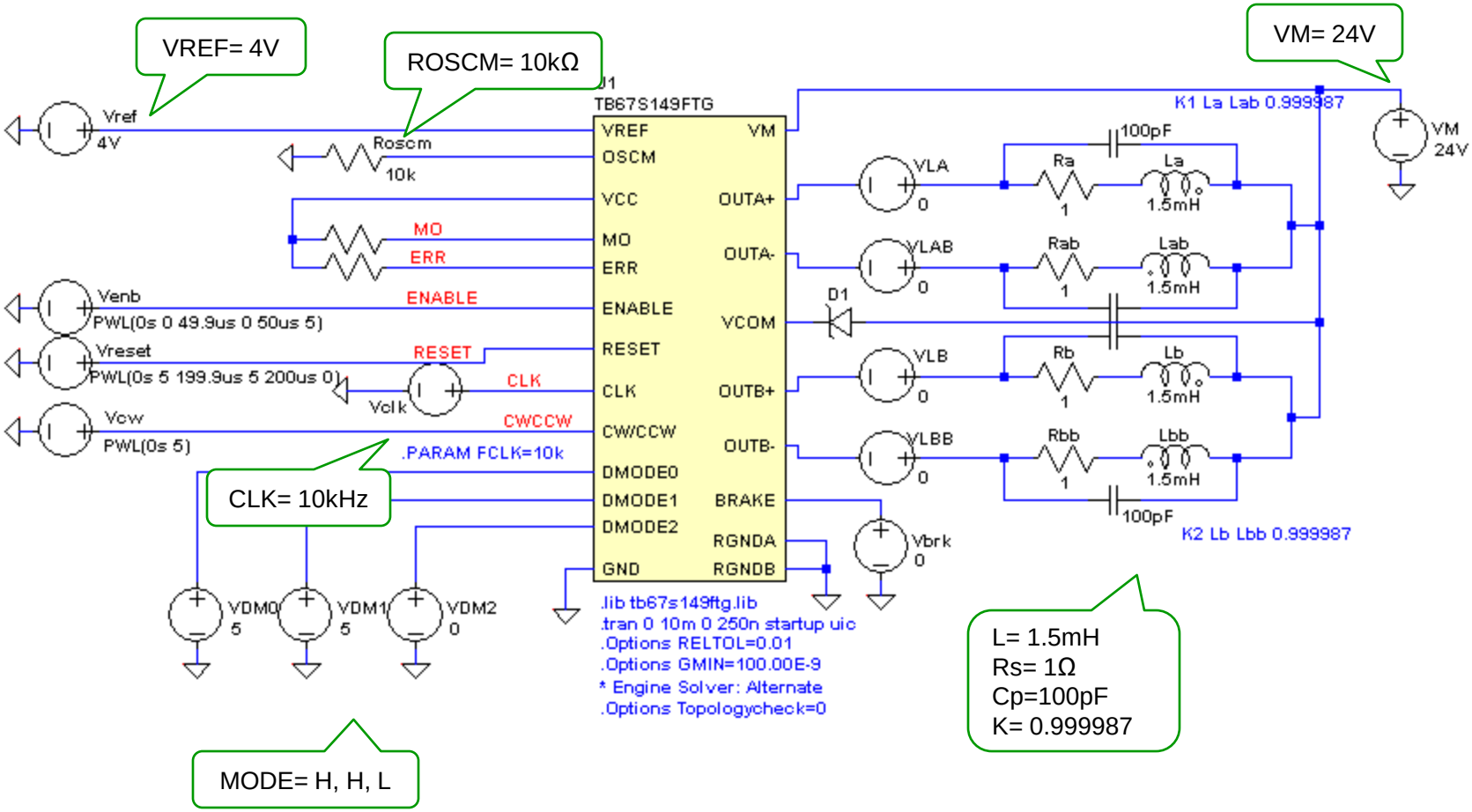
6) 1/16 step (H, H, L)
- Simulation Circuit



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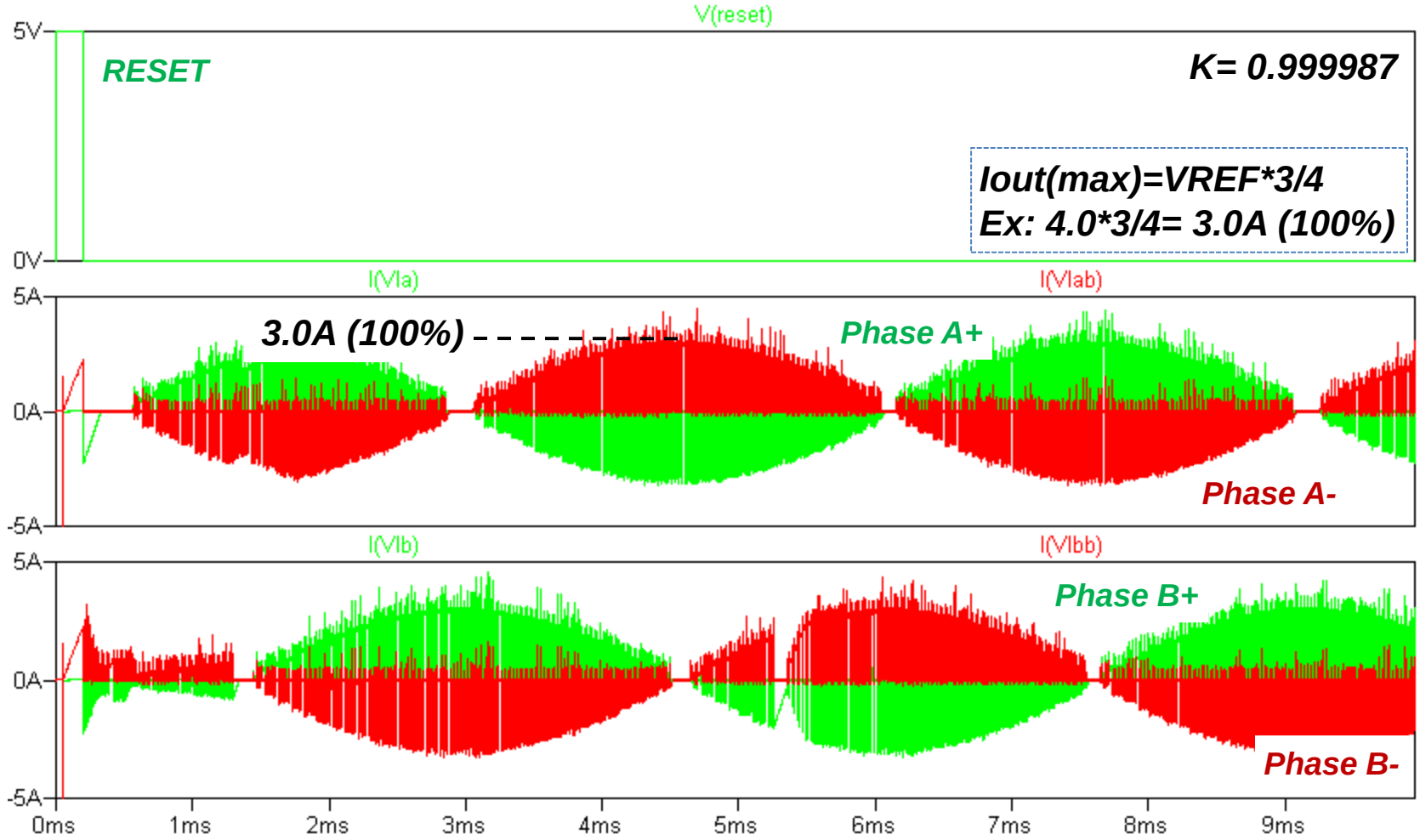
6) 1/16 step (H, H, L)
- Simulation Result



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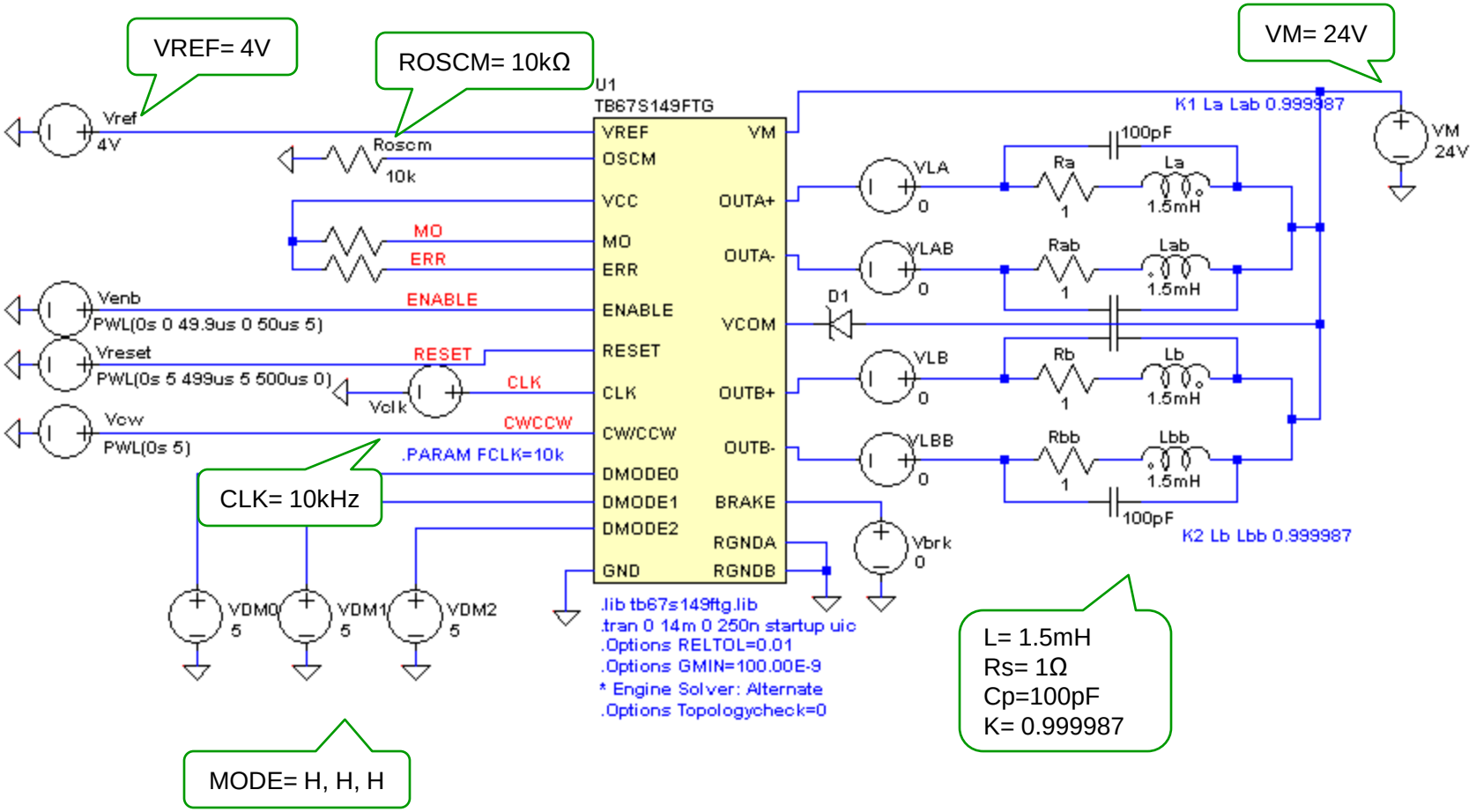
7) 1/32 step (H, H, H)
- Simulation Circuit



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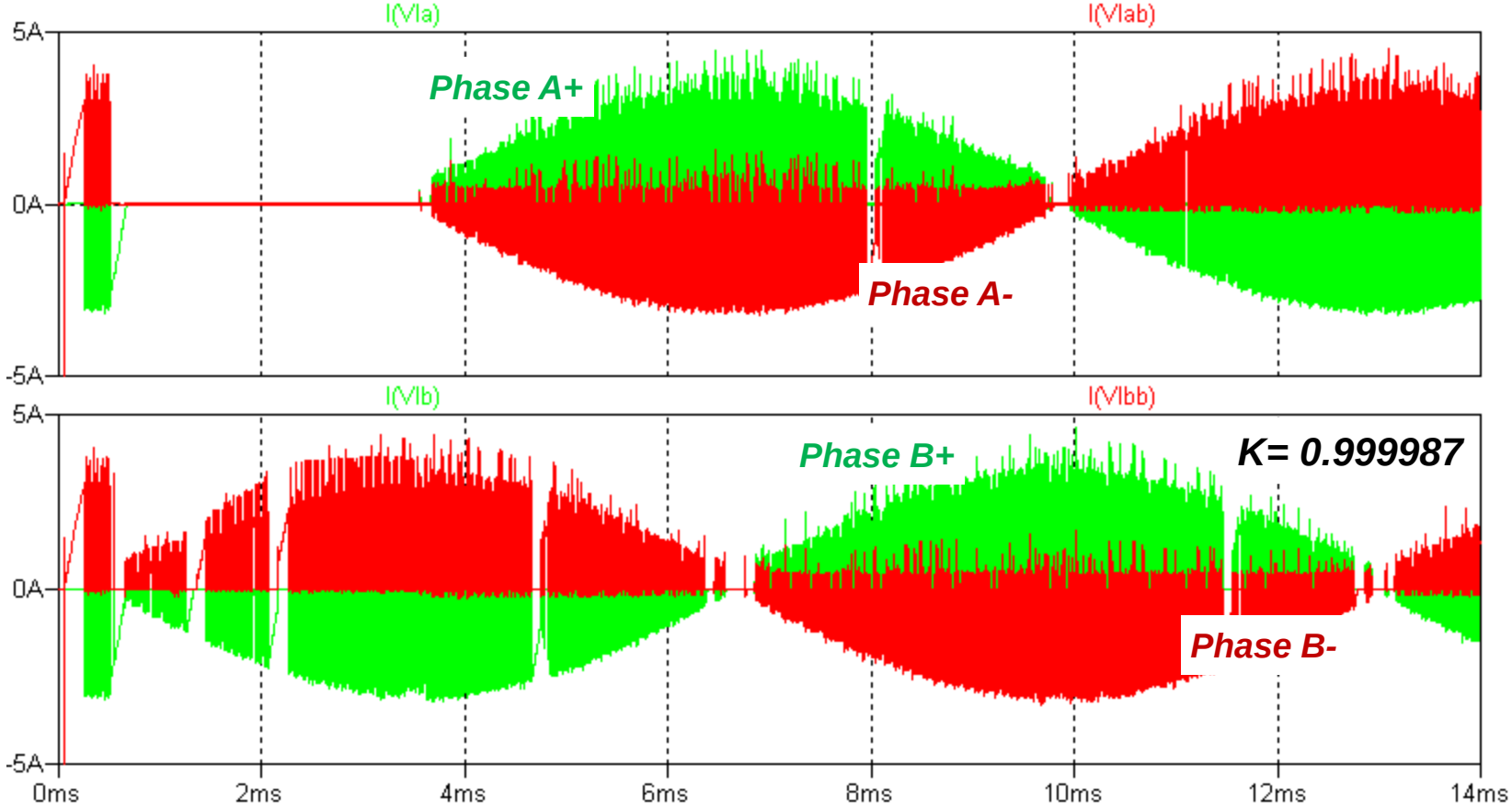
7) 1/32 step (H, H, H)
- Simulation Result



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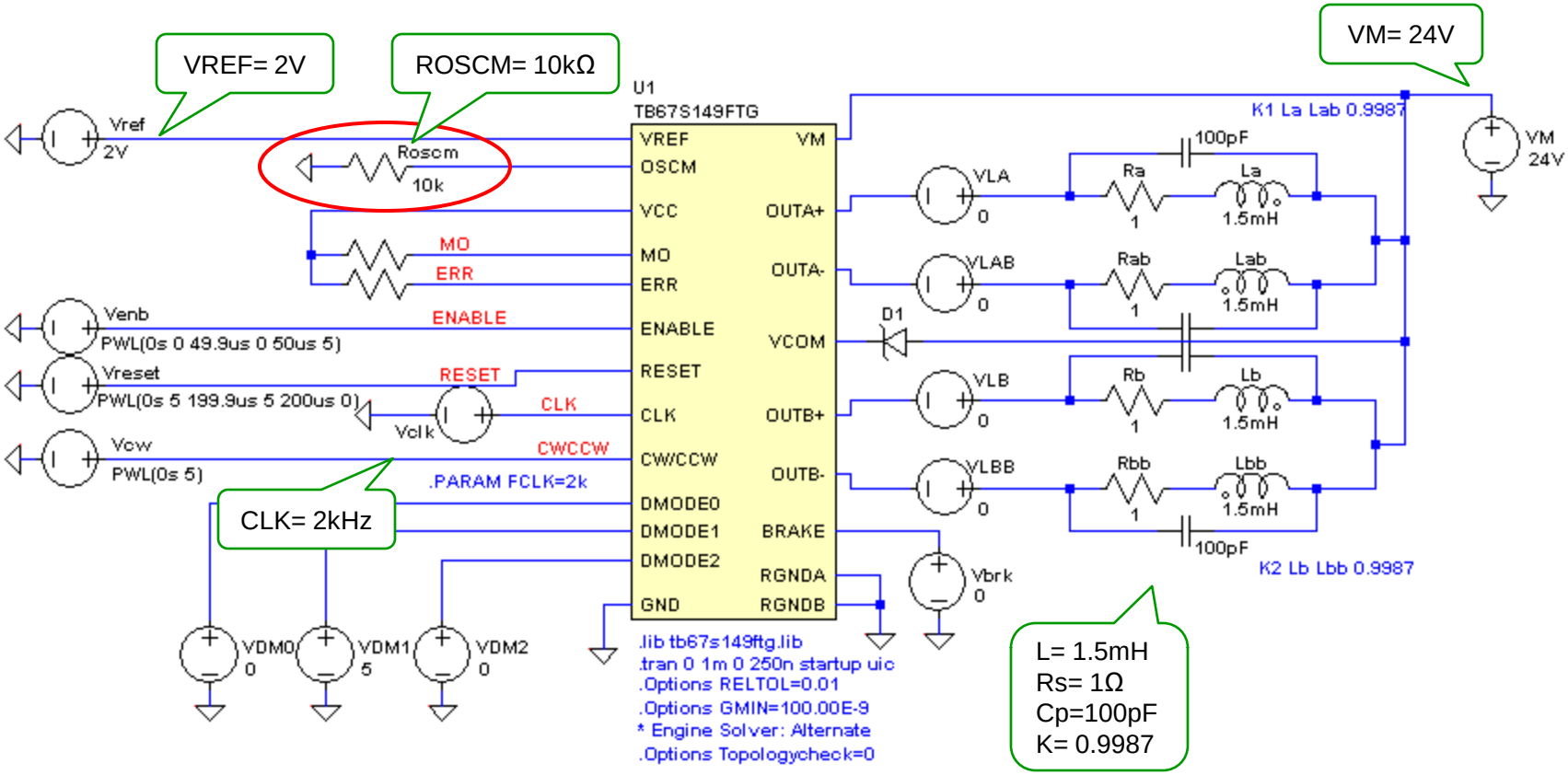
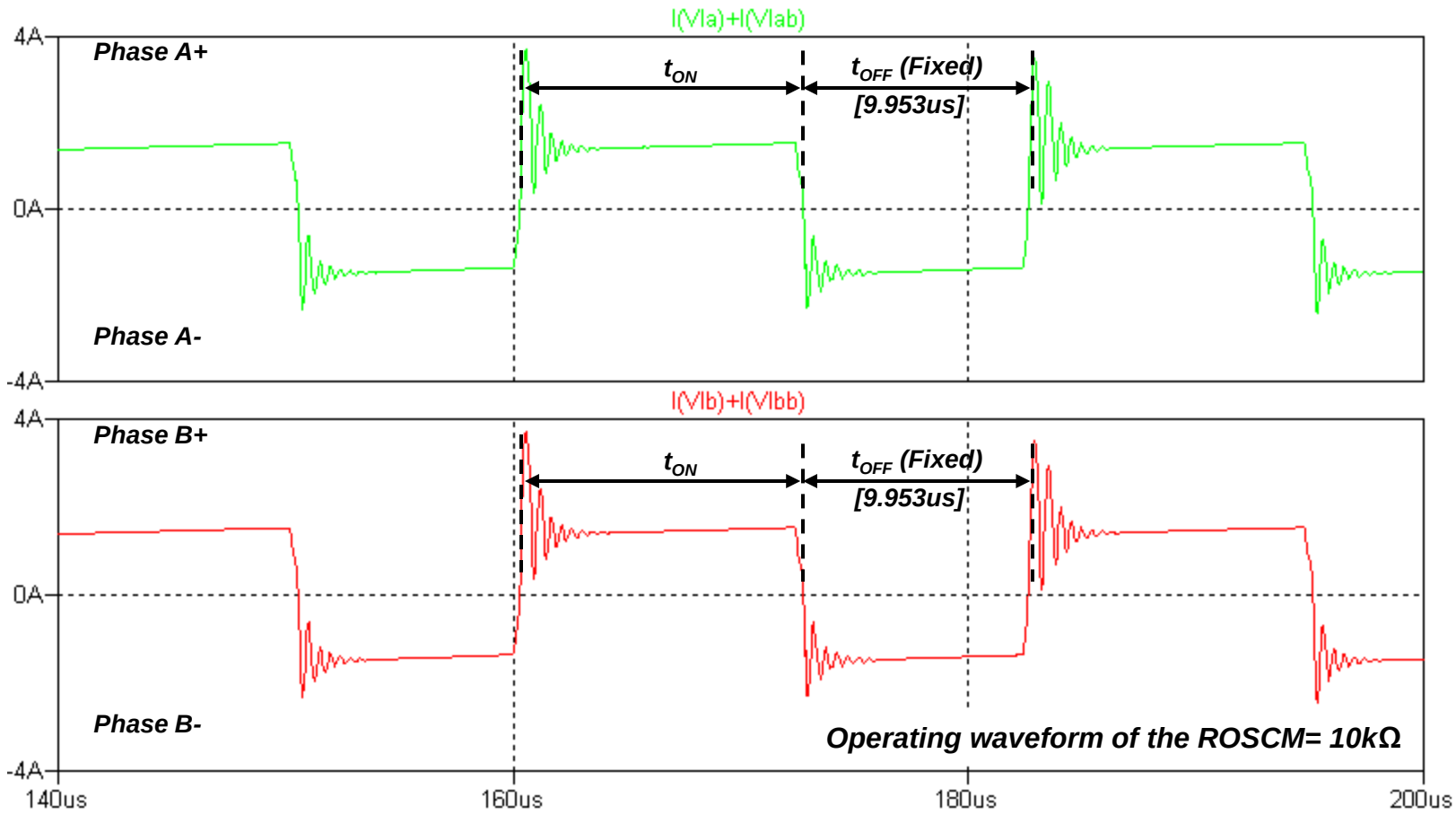
8) Fixed off time setting
- Simulation Circuit



8) Fixed off time setting
- Simulation Result



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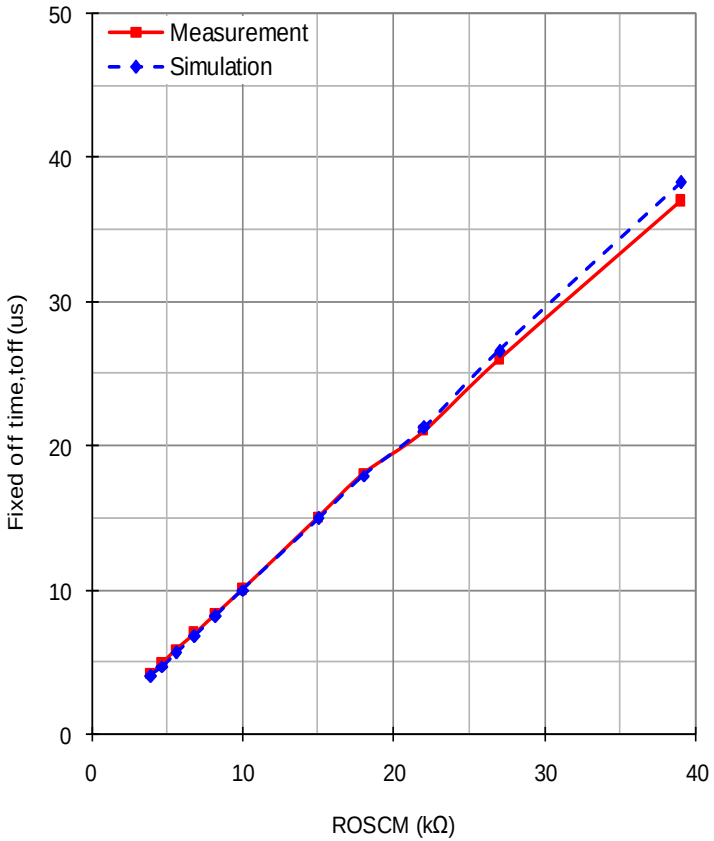
8) Fixed off time setting
- R_{OSCM} vs. t_{OFF}

Comparison table

ROSCM (kΩ)	TOFF (us)		%Error
	Measurement	Simulation	
3.9	4.100	4.014	-2.10
4.7	4.900	4.678	-4.53
5.6	5.800	5.574	-3.90
6.8	7.000	6.768	-3.31
8.2	8.300	8.162	-1.66
10	10.000	9.953	-0.47
15	15.000	14.930	-0.467
18	18.000	17.915	-0.472
22	21.000	21.256	1.219
27	26.000	26.577	2.219
39	37.000	38.245	3.365

Comparison Graph



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Simulation Settings

Analysis directives:

Time Domain (Transient)
 Run to time: 4~15ms
 Start saving data after: 0s
 Maximum step size: 250ns
(*startup uic)

.Options :
.Options RELTOL=0.01
.Options GMIN=100.00E-9
.Options METHOD=GEAR
* Engine Solver: Alternate
.Options Topologycheck=0

Libraries:

.LIB tb67s149ftg.lib

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