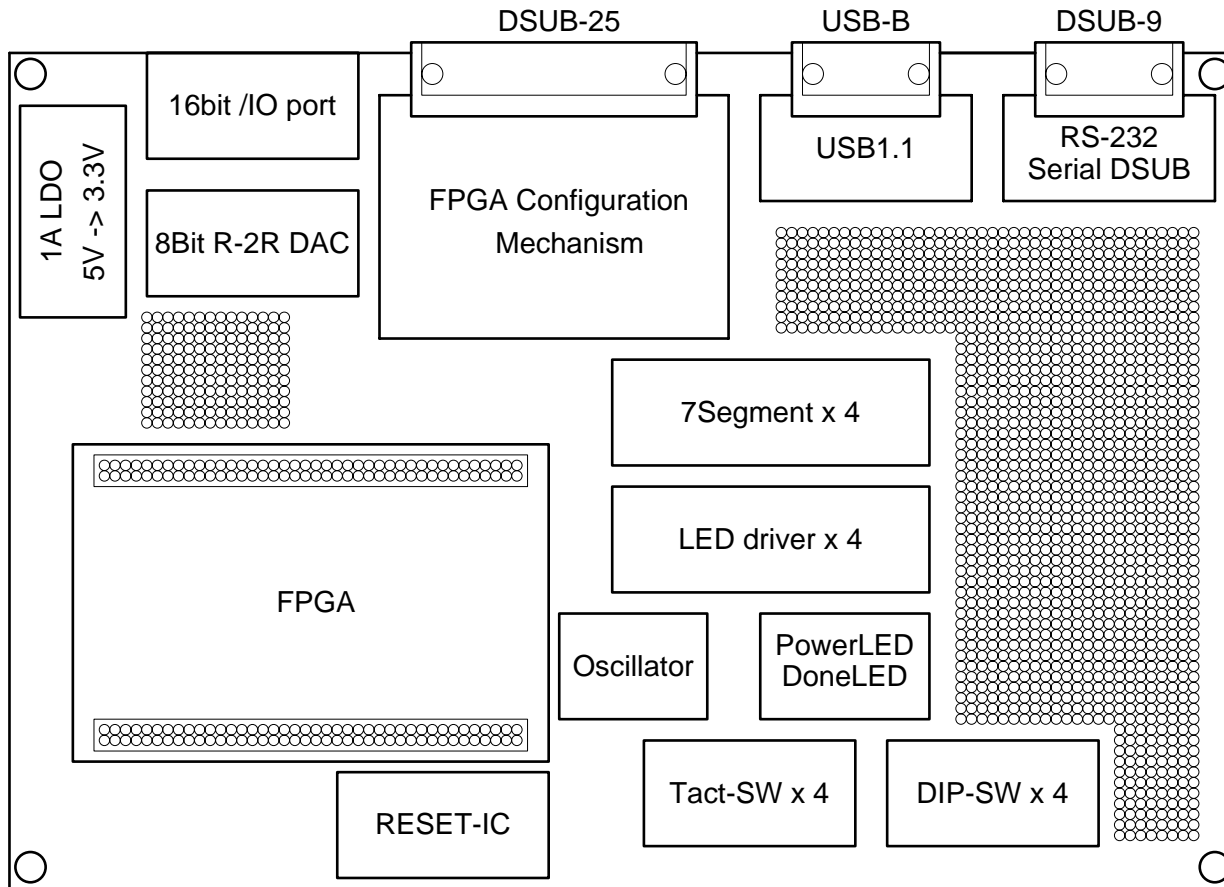


MFPGA-BASE Rev1.0

MARUTSU custom FPGA evaluation mother board.



LATTICE

CLK	1
RESET	1
7Segment	32
Tact-SW	4
DIP-SW	4
GPIO-IN	8
GPIO-OUT	8
DAC-ENB	1
UART	2
USB1.1	3

64

XILINX

CLK	1
RESET	1
7Segment	32
Tact-SW	4
DIP-SW	4
GPIO-IN	4
GPIO-OUT	6
DAC-ENB	1
UART	2
USB1.1	3

58

ALTERA

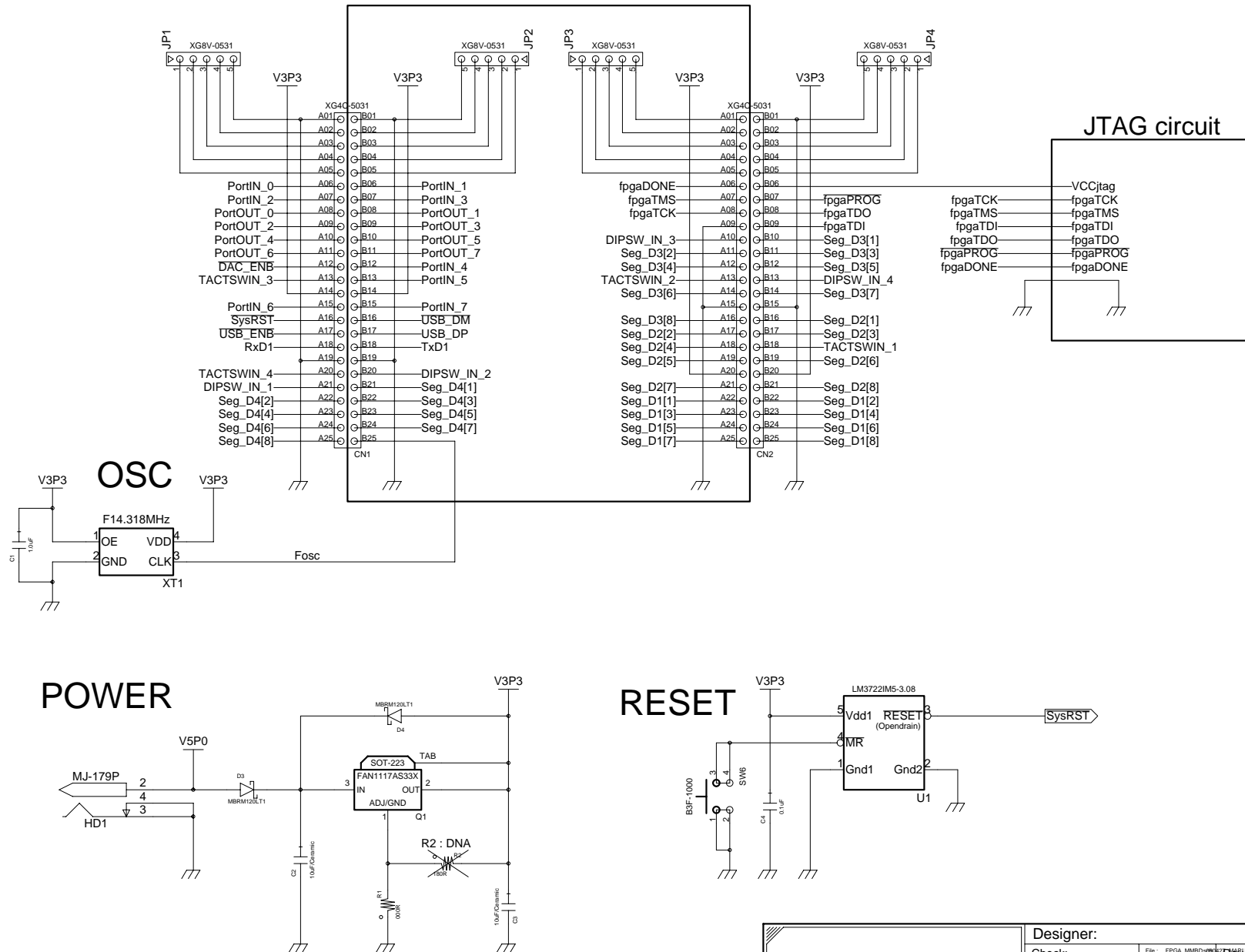
CLK	1
RESET	1
7Segment	32
Tact-SW	4
DIP-SW	4
GPIO-IN	4
GPIO-OUT	8
DAC-ENB	1
UART	2
USB1.1	3

60

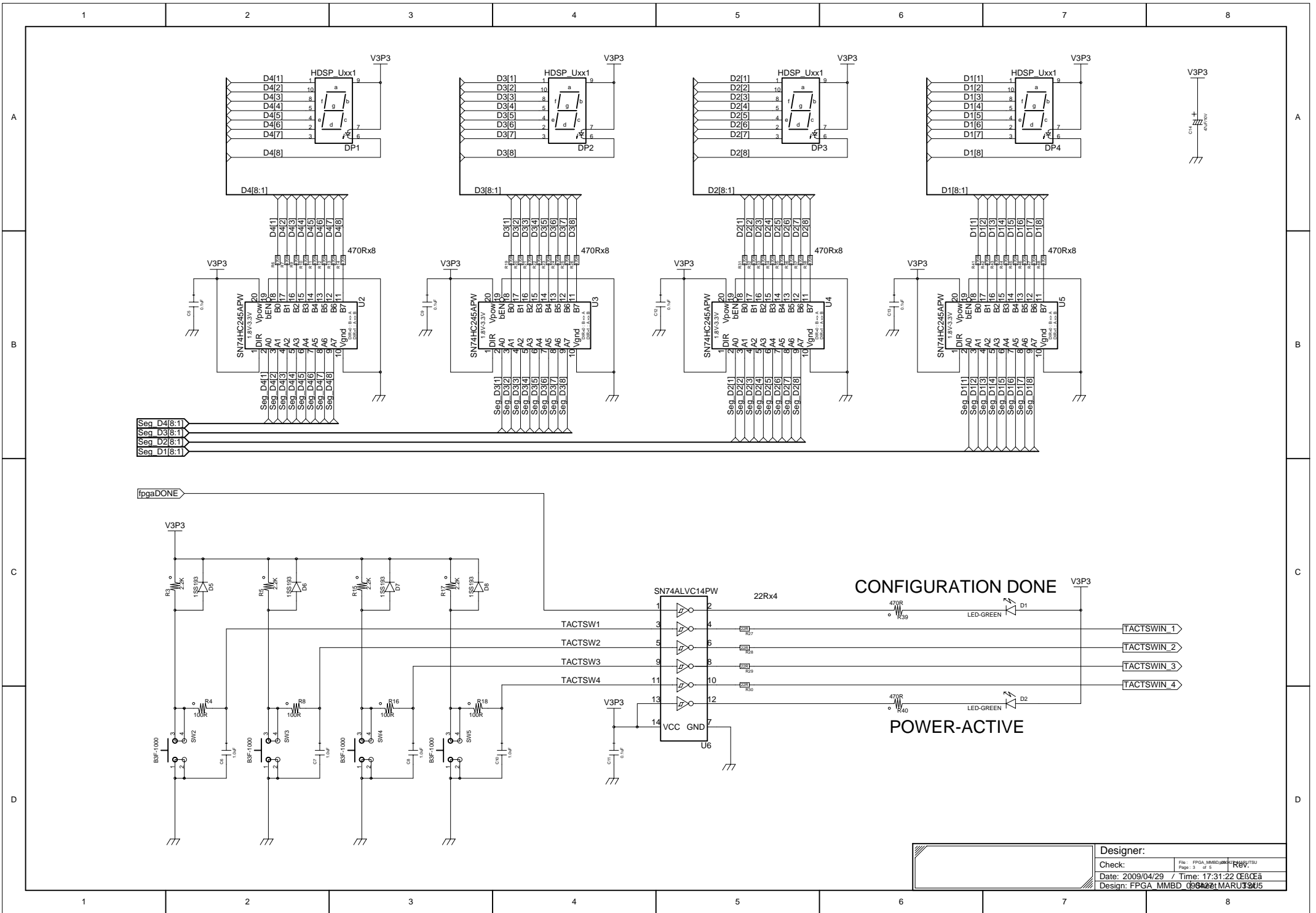
Designer:
 Check:
 Date: 2009/04/29 / Time: 17:31:22
 Design: FPGA_MMBD_090429_MARUTSU

FPGA Board

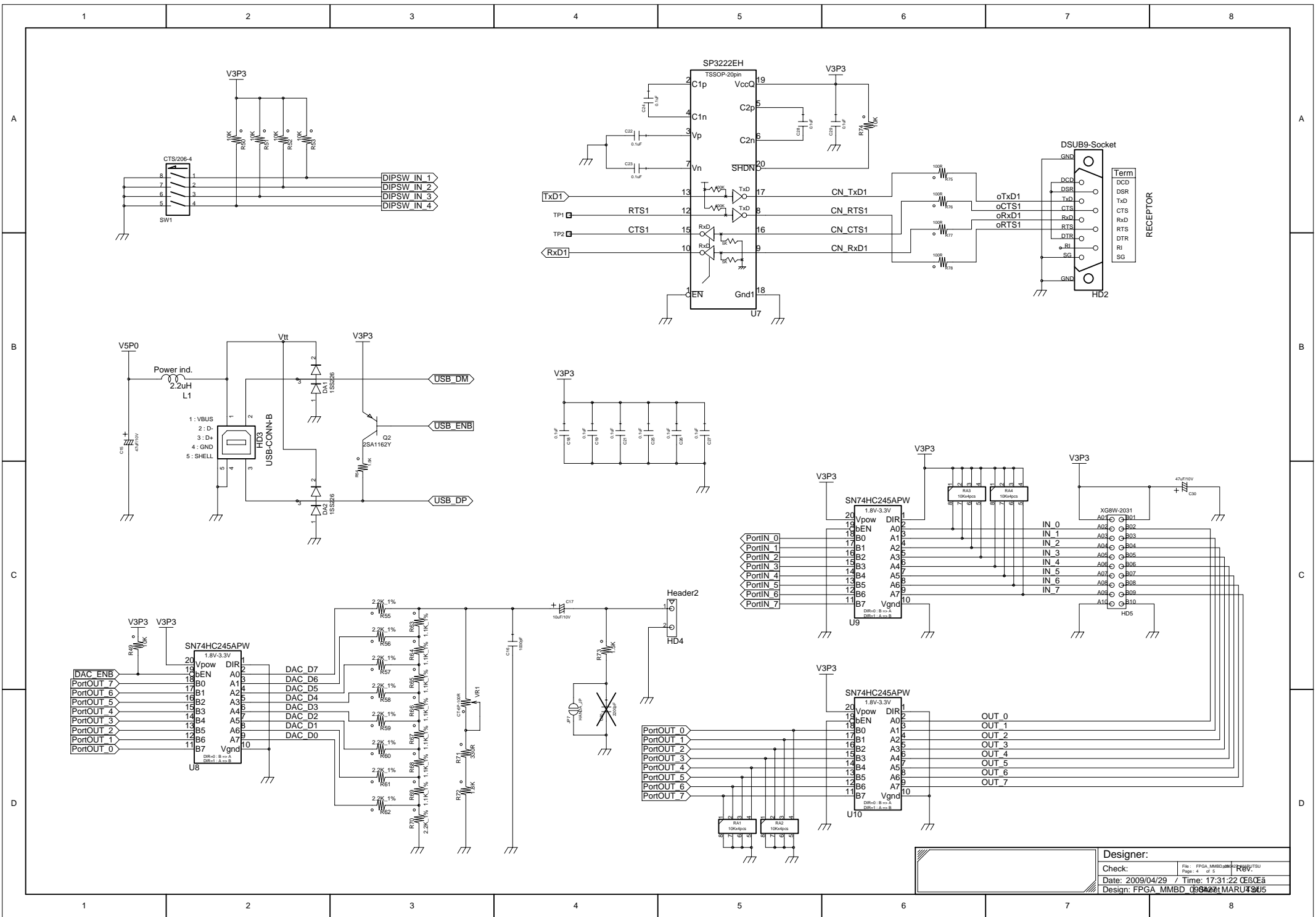
JTAG circuit



Designer:		File: FPGA_MMBD090429	
Check:	Page: 2 of 5	Date: 2009/04/29 / Time: 17:31:22 CEJCEa	
Date: 2009/04/29		Design: FPGA_MMBD090429	



Designer: _____
 Check: _____
 Date: 2009/04/29 / Time: 17:31:22 CE&C&ã
 Design: FPGA MMBD 0904291 MARUJ3015



Designer: _____
 Check: _____
 Date: 2009/04/29 / Time: 17:31:22
 Design: FPGA_MMBD_036221_MARU73015

A

B

C

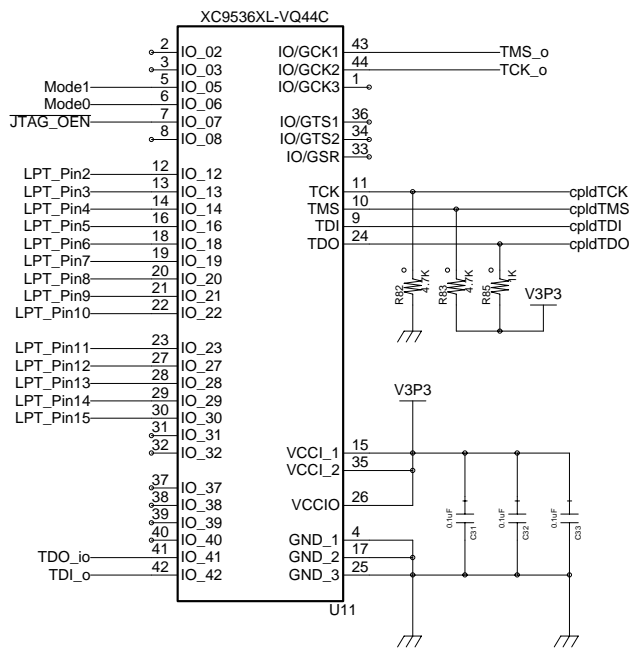
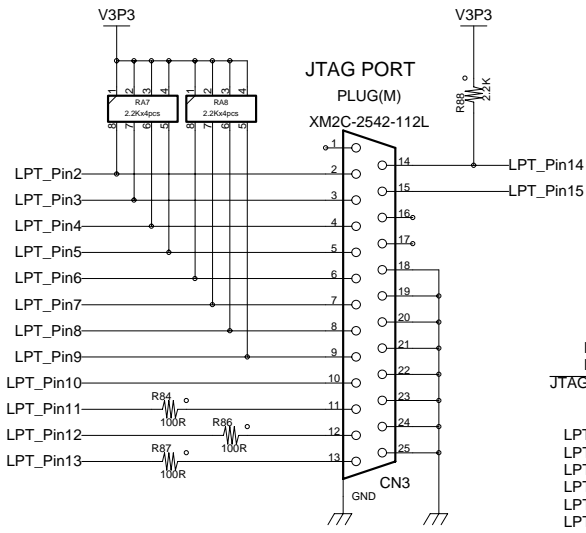
D

A

B

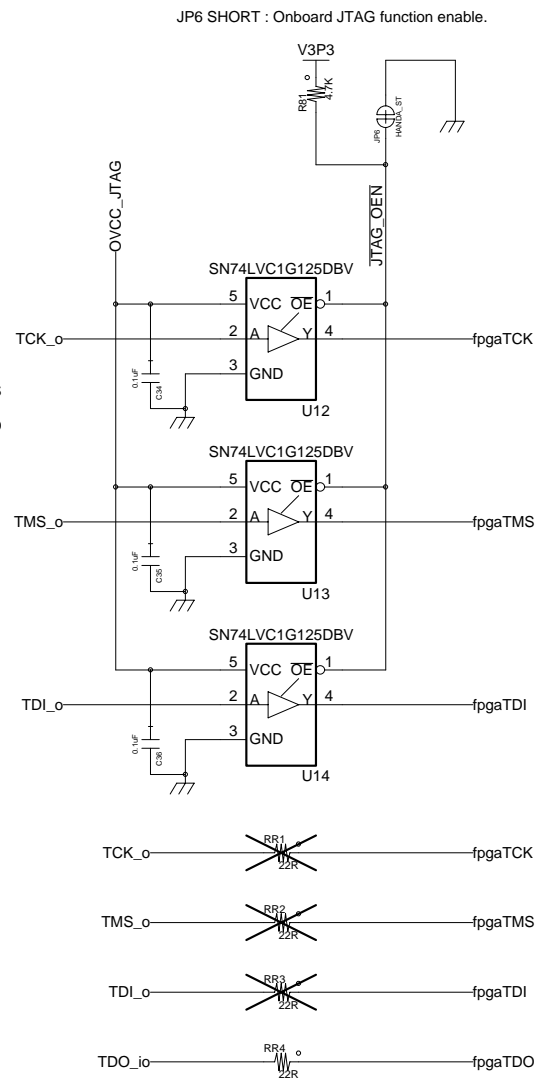
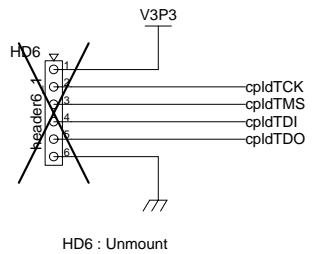
C

D



JTAG VCC select.
 1-2 : ALTERA / LATTICE (default)
 2-3 : XILINX

FPGA select
 5-6 open / 7-8 open --- LATTICE (default)
 5-6 short / 7-8 open --- ALTERA
 5-6 open / 7-8 short --- XILINX
 5-6 short / 7-8 short --- ACTEL



RR1/RR2/RR3 is exclusive equip to U12/U13/U14.
 Default : U12/U13/U14 unmount.

Designer:	
Check:	File: FPGA_MMBD... Page: 5 of 5
Date: 2009/04/29	Time: 17:31:22
Design: FPGA_MMBD	090201MARSU505