Digital Discovery Reference Manual

The Digilent Digital Discovery[™] is a combined logic analyzer and pattern generator instrument that was created to be the ultimate embedded development companion. The Digital Discovery was designed to optimize channels, speed, and portability. The small form factor facilitates easy storage and provides a whole suite of advanced features to allow you to debug, visualize, and simulate digital signals for most embedded projects. The digital inputs and outputs can be connected to a circuit using simple wire probes or breadboard wires; alternatively, the Digital Discovery High Speed Adapter and impedance-matched probes can be used to connect and utilize the inputs and outputs for more advanced projects. The Digital Discovery is driven by the free <u>WaveForms</u>

(https://reference.digilentinc.com/reference/software/waveforms/waveforms-3/start) (3.5.4 or later) software and can be configured to be any of the below instruments:

- 24-channel digital logic analyzer (1.2...3.3V CMOS, up to 800MS/s(with the High Speed Adapter))
- 16-channel pattern generator (1.2...3.3V CMOS, 100MS/s)
- 16-channel virtual digital I/O including buttons, switches, and LEDs perfect for logic training applications
- Two input/output digital trigger signals for linking multiple instruments (1.2...3.3V CMOS)
- A programmable power supply of 1.2...3.3V/100mA. The same voltage supplies the Logic Analyzer input buffers and the Pattern Generator input/output buffers, for keeping the logic level compatibility with the circuit under test.
- Digital Bus Analyzers (SPI, I²C, UART, I2S, CAN, Parallel)

The Digital Discovery was designed for anyone embarking on embedded development. Its features and specifications were deliberately chosen to maintain a small and portable form factor, withstand use in a variety of environments, and keep costs down, while balancing the requirements of operating on USB Power.

This document describes the Digital Discovery hardware. For more information on using the WaveForms software with Digital Discovery see the 🖉 WaveForms reference center (https://reference.digilentinc.com/reference/software/waveforms/waveforms-3/start) and 🎱 WaveForms reference manual (https://reference.digilentinc.com/reference/software/waveforms-3/reference-manual).

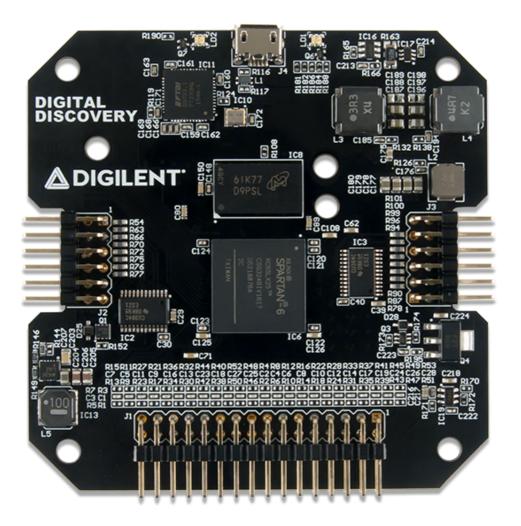


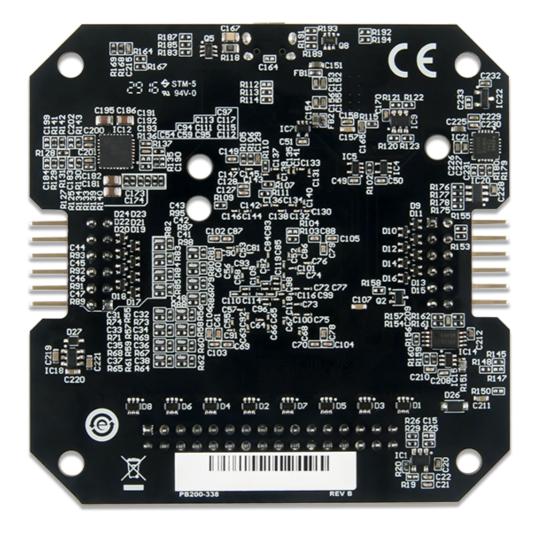
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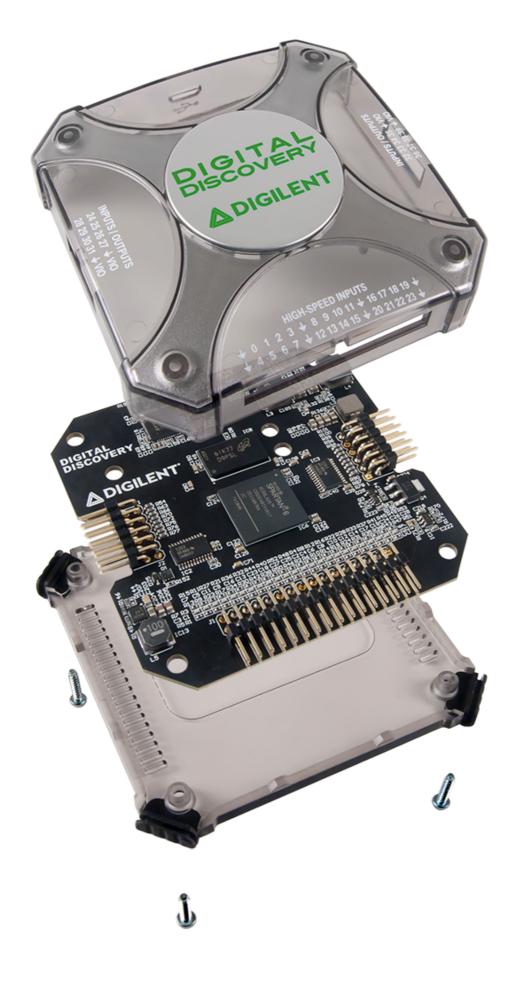


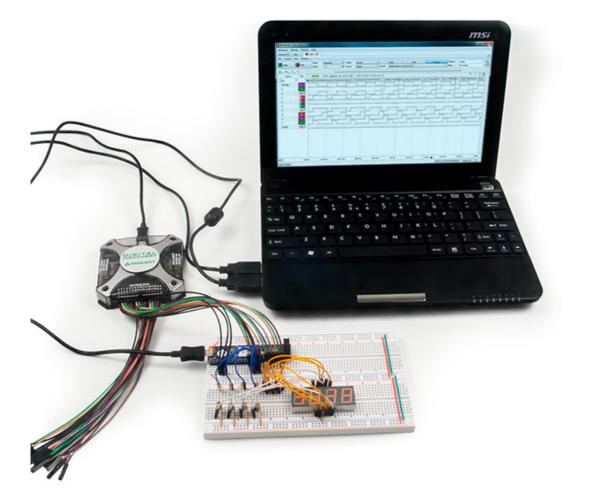
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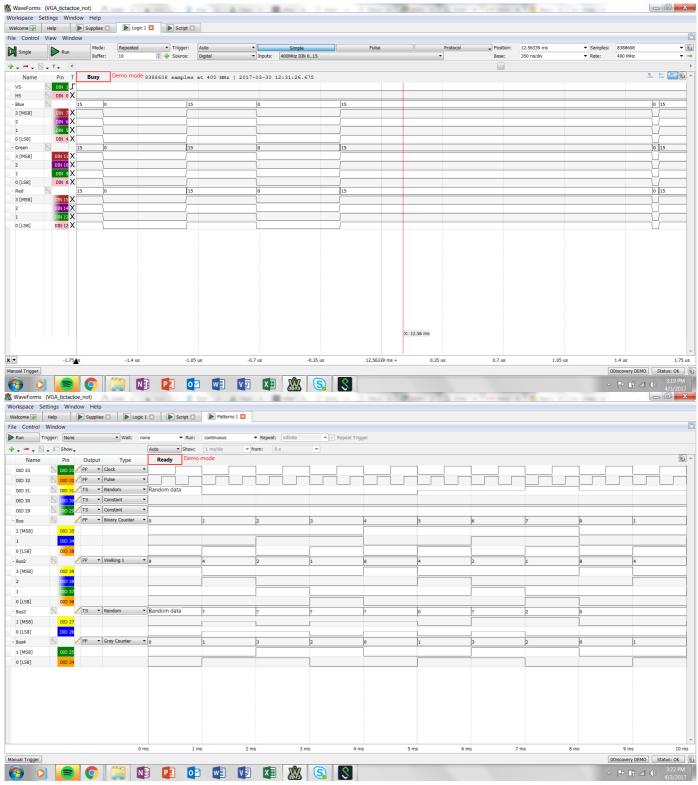








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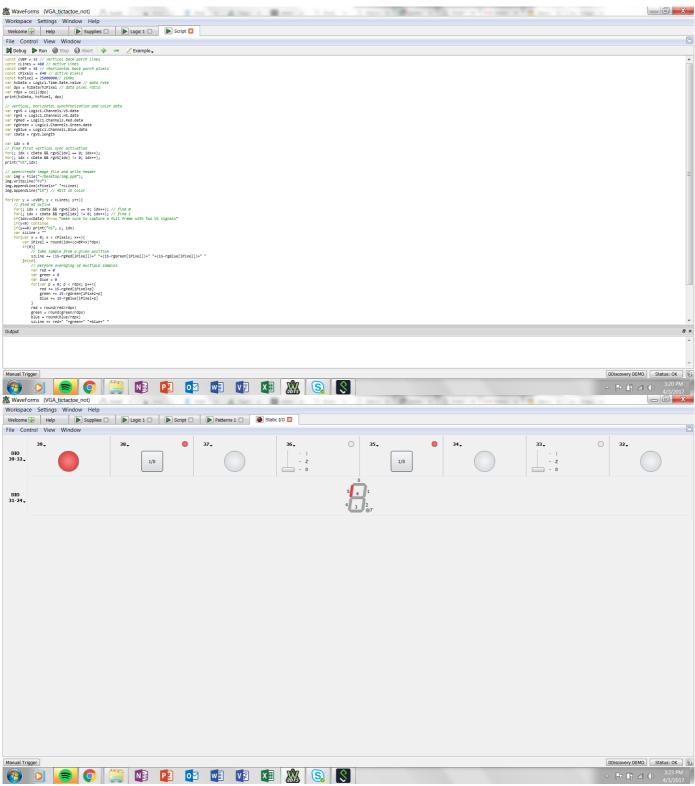


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Digital Discovery Reference Manual [Reference.Digilentinc]

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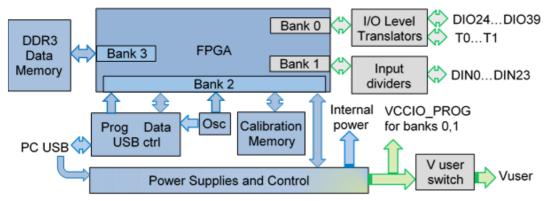


1.1 Architectural Overview and Block Diagram

Digital Discovery's high-level block diagram is presented in Figure 2, below. The core of the Digital Discovery 2 is the Xilinx® Spartan®-6 FPGA (specifically, the XC6SLX25-2 device). The WaveForms application automatically programs the Discovery's FPGA at start-up with a configuration file designed to implement a multi-function test and measurement instrument. Once programmed, the FPGA inside the Discovery communicates with the PC-based WaveForms application via a USB 2.0 connection. The WaveForms software works with the FPGA to control all the functional blocks of the Digital Discovery, including setting parameters, acquiring data, and transferring and storing data into the DDR3 memory. Signals and equations also use certain naming conventions. Signals in the Input block use "DIN" prefix to indicate these are inputs only. Signals in the Input/Output block use "DIO" prefix. Signals at the user connectors include "USR" in their names, while signals at the FPGA pins include "FPGA". Signals at the FPGA pins driving the pull resistors for DIO signals, include "PULL" in their names. DIN inputs are indexed 0 to 23, DIO input/outputs are indexed 24 to 39. Memory signals have the "DDR" prefix. Supply rails show the voltage with the <u>VCCC 0</u> prefix. Referring to the block diagram in Figure 2 below:

- The I/O Level Translators build the bidirectional interface for input/output pins (used in the Pattern Generator, Static IO, and Logic Analyzer)
- The Input Dividers are the conditioning circuits for the input pins (used in the Logic Analyzer)
- The FPGA banks are supplied at different voltages:
 - Bank 0, Bank1: VCCIO_PROG, a variable voltage, settable in the range 1.2V...3.3V. The logic standard is set to: LVCMOS18_JEDEC. The threshold voltage is about 0.45*VCCIO_PROG.
 - Bank 2: VCC3V3, a fixed voltage of 3.3V.
 - Bank 3: VCC1V5, a fixed voltage of 1.5V.
- A replica of VCCIO_PROG is also available to the user, as VCCIO_USR, under the V user switch control.
- The DDR3 Data Memory block stores the Logic analyzer acquired data.
- The Power Supplies and Control block generates all internal supply voltages as well as user supply programmable voltage. The control block also monitors the device power consumption for USB compliance.
- The USB Controller interfaces with the PC for programming the volatile FPGA memory after power on or when a new configuration is requested. After that, it performs the data transfer between the PC and FPGA.
- The Calibration Memory stores all calibration parameters. The Digital Discovery includes no analog calibration circuitry. Instead, a calibration operation is performed at manufacturing (or by the user), and parameters are stored in memory. The WaveForms software uses these parameters to adjust the acquired data and the generated signals.

In the sections that follow, schematics are not shown separately for identical blocks. For example, the Input Divider is only shown for DIN0 since the schematic for all other DIN1...DIN23 is identical.



(https://reference.digilentinc.com/_detail/digital_discovery/dd_2blockdiagram.png?id=reference%3Ainstrumentation%3Adigital-discovery%3Areference-manual)

Figure 2. Digital Discovery Hardware block diagram. 🛛

2. I/O Level Translators

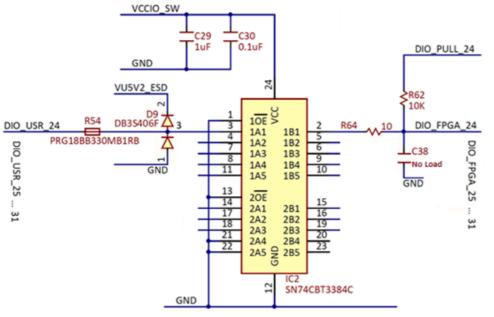
Figure 3 shows the DIO user connectors and Figure 4 shows the I/O level translator for DIO24. DIO25 to DIO31 use similar discrete components, connected to pins 1A2...2A3, respectively 1B2...2B3 of IC2.

The I/O Level Translators block includes: - Input protection: series PTC (33Ω, positive thermal coefficient thermistor) and parallel ESD/overvoltage diodes to 5.2V and <u>GND.()</u>. - Voltage level translators, SN74CBT3384C. When DIO_USR signals are driven by the DUT, the voltage at the FPGA pins is limited at VCCIO_SW-1V = 3.3V. When the FPGA drives DIO_USR signals, they pass unlimited trough the low impedance SN74CBT3384C buffer. - Pull resistors: 10k, individually settable as Pull-Up, Pull-Down or High-Z. This is done with a second FPGA pin associated to each DIO, which can be driven High, Low or HiZ. The Pull-Up voltage is VCCIO_PROG. - DIO_FPGA pin: the bank supply voltage is VCCIO_PROG> The WaveForms software can set VCCIO_PROG from 1.2 to 3.3V. The FPGA input threshold level is about 45% of VCCIO_PROG. The output strength can be set from 2mA to 16mA. The output slew rate can be set as: Quiet, Slow or Fast.



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Figure 3. DIO user connectors. []



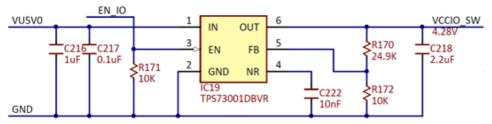
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Figure 4. I/O level translator.

The LDO in Figure 5 generates the 4.3V to supply the level translator in Figure 4.

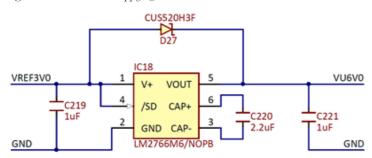
The charge-pump in Figure 6 provides the the 6V reference for the clipper in Figure 7.

When all ESD diodes protecting DIO_USR in Figure 3 are OFF, Q3B is OFF, and also Q4. If overvoltage is applied on some DIO_USR pins, rising VU5V2_ESD in Figure 7 above 5.2V, Q3B and Q4 turn ON, clipping VU5V2_ESD at approximately 5V.



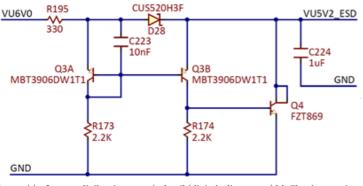
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Figure 5. VCCIO_SW supply.



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Figure 6. VU6V0 supply. []



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Figure Figure 7. Backpowering voltage clipper.

3. Input Dividers

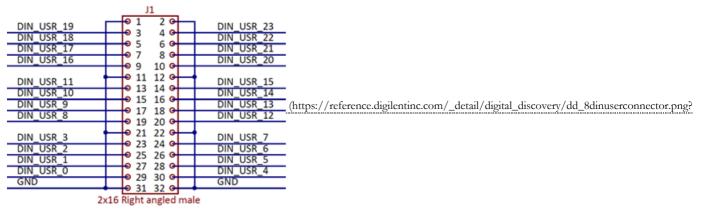
Figure 8 shows the DIN user connector and Figure 9 shows the Input Divider for DIN0. DIN1 to DIN23 use similar input circuitry.

The Input Dividers block includes:

Frequency compensated voltage dividers: 10/11 resistive dividers with compensation for FPGA input capacitance. All the dividers
together have the settable reference voltage VREFIO. Setting VREFIO close to the logical threshold voltage provides the highest
sensitivity, while setting VREFIO at <u>GND</u>() or logical supply voltage increase the noise immunity. The voltage at the FPGA pin:

$$V_{DIN_FPGA} = \frac{10}{11} \bullet V_{DIN_USR} + \frac{1}{11} \bullet V_{REFIO}$$
(1)

- The reference voltage VREFIO is generated as in Figure 10. DIN_VREF_H and DIN_VREF_L are connected to FPGA pins in bank 1. Bank1 is supplied at VCCIO. VREFIO can be set at:
 - 0V, when DIN_VREF_H = DIN_VREF_L = low
 - 0.43*VCCIO_PROG, when DIN_VREF_H = high, DIN_VREF_L = low
 - VCCIO_PROG, when DIN_VREF_H = DIN_VREF_L = high.
- ESD/Overvoltage protection: Shottky diodes to VCC3V3.
- DIN_FPGA pin: the bank supply voltage is VCCIO_PROG. The WaveForms software can set VCCIO_PROG from 1.2 to 3.3V. The FPGA input threshold level is about 45% of VCCIO_PROG.



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Figure 8. DIN user connector. []



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Figure 9. Input Divider. []



Figure 10 VREFIO reference.

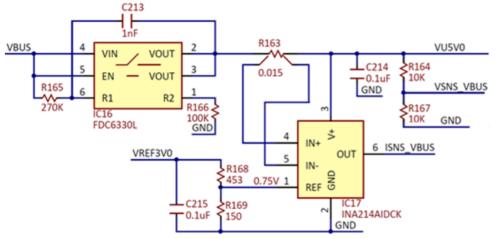
4. Power supplies and control

4.1 Internal power supplies

In Figure 11, IC16 limits the in-rush current when the device is connected to the USB port. INA214 is a current shunt amplifier, with a gain of 100. With Vref = 0.75V and R163 = $15m\Omega$, the output voltage is:

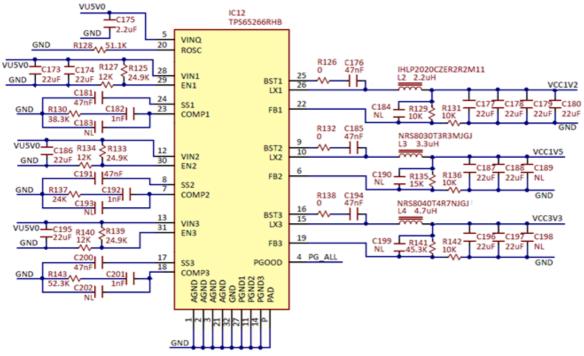
$$V_{ISNS_VBUS} = 100 \bullet (V_{IN+} - V_{IN-}) + 0.75V = 1.5 \bullet I_{VU5V0} + 0.75V$$
(2)

The VBUS voltage is halved to VSNS_VBUS, for being also monitored. IC12 in Figure 11 is a triple power supply, generating the rails of 1.2V for the FPGA core, 1.5V for Bank 3 and DDR3 memory and 3.3V, for various circuits.



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Figure 11 VBUS monitoring. []



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Figure 12. Internal voltage supplies.

4.2 Programmable power supply

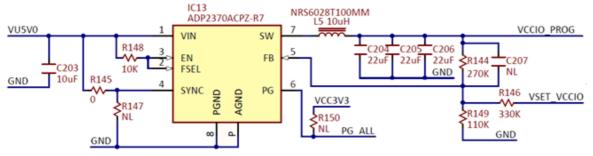
IC13 in Figure 13 generates the VCCIO_PROG, the variable voltage to supply the input and IO banks of the FPGA:

$$V_{VCCIO_PROG} = V_{FB} \bullet \left(1 + \frac{R_{144}}{R_{146}} + \frac{R_{144}}{R_{149}}\right) - V_{VSET_VCCIO} \bullet \frac{R_{144}}{R_{146}} = 3.42V - V_{VSET_VCCIO} \bullet 0.82$$
(3)

With VVSET_VCCIO ϵ (0...3V), VCCIO_PROG could be theoretically set in the range: VCCIO_PROG ϵ (1.02V...3.42V). IC15 is a current shunt amplifier, with a gain of 100. With Vref = 0.75V and R115 = 50m Ω , the output voltage is:

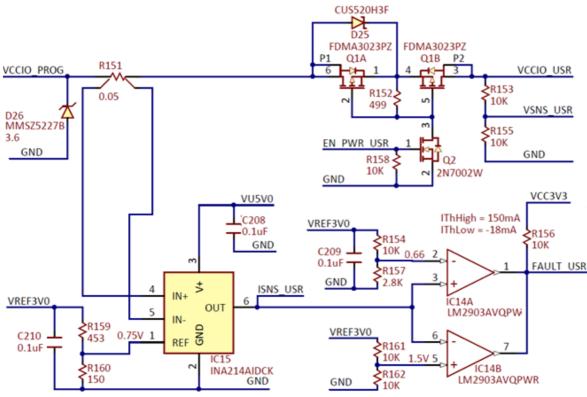
$$V_{ISNS_USR} = 100 \bullet (V_{IN+} - V_{IN-}) + 0.75V = 5 \bullet I_{VCCIO_USR} + 0.75V$$
(4)

IC14 is a window comparator: FAULT_USR is logical LOW, when VISNS_USR is either more than 1.5V (IVCCIO_USR>150mA) or less than 0.66V (IVCCIO_USR←18mA). If this happens, the FPGA turns EN_PWR_USR to LOW, which turns both Q1A and Q1B OFF, to protect VCCIO_USR against overcurrent and reverse current respectively. VCCIO_USR is halved to VSNS_USR, for being monitored.



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Figure 13. VCCIO_PROG supply.



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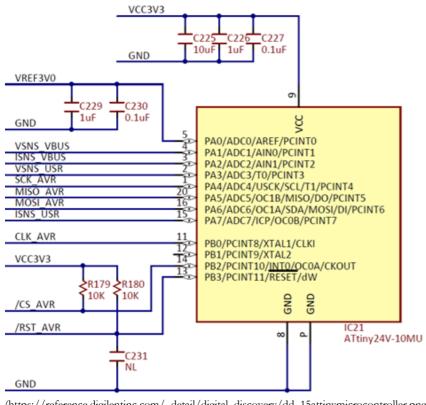
Figure 14. VCCIO_USR protection and switch. []

4.3. Monitoring the power supplies

The microcontroller in Figure 15 has two roles:

- 1. <u>A/D_()</u> Conversion of VVSNS_VBUS, VISNS_VBUS, VVSNS_USR, VISNS_USR, representing the voltages and currents consumed from VBUS and VCCIO_USR respectively. The digital results are passed to the FPGA via an SPI interface.
- 2. Storing the calibration parameters computed as a part of the manufacturing test. During regular behavior, the WaveForms Software reads the parameters and corrects both generated and acquired signals.

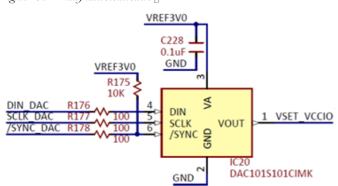
The <u>DAC.()</u> in Figure 16 generates the setting voltage for programming the value of VCCIO. IC22 in Figure 17 provides 3V reference voltage for both <u>ADC.()</u> and <u>DAC.()</u> above.



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Figure 15. ATtiny microcontroller. []



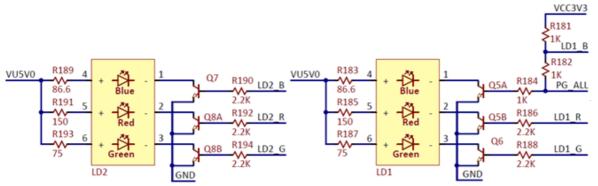
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Figure 17. VREF3V0. []

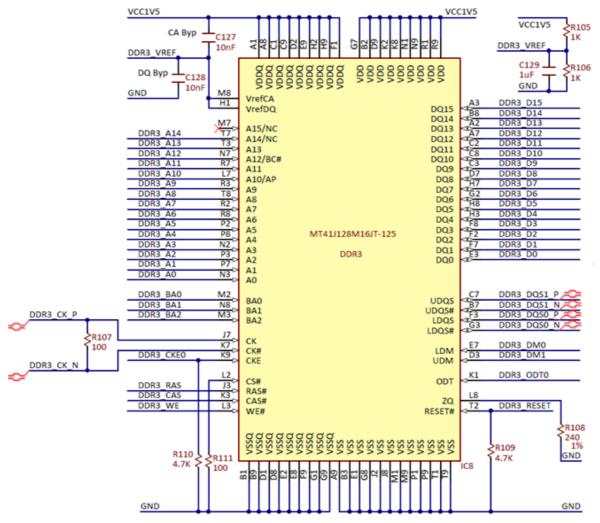
5. LEDs and DDR3 Memory

Figure 18 shows the two tricolor LEDs used to symbolize the Digital discovery status. Figure 19 shows the DDR3 memory for the Logic Analyzer buffer.



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Figure 18. LEDs. []



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Figure 19. DDR3 memory. []

6. USB Controller

The USB interface performs two tasks:

- **Programming the FPGA:** There is no non-volatile FPGA configuration memory on the Digital Discovery. The WaveForms software identifies the connected device and downloads an appropriate .bit file at power-up, via a Digilent USB-JTAG interface. Adept run-time is used for low level protocols.
- Data exchange: All instrument configuration data, acquired data and status information is handled via a Digilent synchronous parallel bus and USB interface. Speed up to 20MB/sec. is reached, depending on USB port type and load as well as PC performance.

7. FPGA

The core of the Digital Discovery is the Xilinx Spartan6 FPGA circuit XC6SLX25. The configured logic performs:

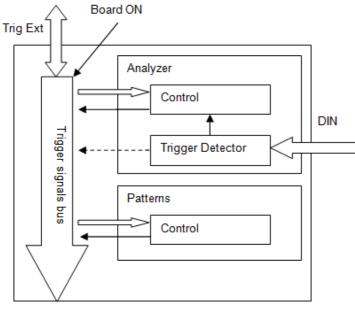
- Clock management (12MHz and 60 MHz () for USB communication, 100MHz and 800MHz for data sampling)
- Acquisition control and Data Storage (Logic Analyzer)
- · Digital signal synthesis (for pattern generator and bus protocol controllers)
- Trigger system (trigger detection and distribution for all instruments)
- Power supplies control and instruments enabling
- Power and temperature monitoring
- Calibration memory control
- Communication with the PC (settings, status data)

Block RAM () of the FPGA is used for signal synthesis. External DDR3 memory is used for data acquisition.

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Detail of the trigger system is shown in Figure 20. Each instrument generates a trigger signal when a trigger condition is met. Each trigger signal (including external triggers) can trigger any instrument and drive the external trigger outputs. This way, all the instruments can synchronize to each other.



(https://reference.digilentinc.com/_detail/digital_discovery/dd_20fpgatriggerdiagram.png?id=reference%3Ainstrumentation%3Adigital-discovery%3Areference-manual)

Figure 20. FPGA configuration trigger block diagram. []

Figure 21 shows the connections to the FPGA banks 0, 1 and 3.

Bank 0 is used for IOs. DIO_FPGA pins are the actual input/output pins to be used with the Pattern Generator, Static IO and Logic Analyzer. A DIO_PULL pin can add Pull-Up or Pull-Down resistors to the associated DIO_FPGA pin (see Figure 4).

Bank 1 is used for high speed Logic Analyzer inputs. DIN_FPGA are the actual input pins, while DIN_VREF_H and DIN_VREF_L set the reference voltage for the input dividers (see Figure 9).

Bank 3 is used as port for the DDR3 memory.

	-	•		-
BANK0	BANKI	1	BANK3	N4 DDR3_RZQ
		_F15	IO_L1P	N3 DDR3 VREF
IO_LIN_VREF	IO_L1P_A25	F15 F16	IO_L1N_VREF	P4 DDR3_ZIO
IO_L2P	IO_L1N_A24_VREF	C17	IO_L2P	P3
10_L2N <15	IO_L29P_A23_M1A13	C18	10_L2N	16
IO_L3P	IO_L29N_A22_M1A14	F14 DIN_FPGA_22	IO_L31P	M5 DDR3 VREF
IU_LSN PARS	IO_L30P_A21_M1RESET	G14	IO_L31N_VREF	U2 DDR3 D13
IO_L4P	IO_L30N_A20_M1A11	014 D17 DIN_FPGA_23	IO_L32P_M3DQ14	U1 DDR3 D12
IO_L4N 484 DIO_FPGA_34	IO_L31P_A19_M1CKE	018	IO_L32N_M3DQ15	
IO_LSP 44 DIO PULL 34	IO_L31N_A18_M1A12	HI2 DIN FPGA 15	IO_L33P_M3DQ12	T1 DDR3_D11
IO_LSN C5	IO_L32P_A17_M1A8	G13	IO_L33N_M3DQ13	
IO_LEP TAS	IO_L32N_A16_M1A9		IO_L34P_M3UDQS	P1 DDR3_DQS1_N
IO_LON POPT	IO_L33P_A15_M1A10	210	IO_L34N_M3UDQSN	
*10_L7P	IO_L33N_A14_M1A4	K12 DIN_FPGA_10	IO_L35P_M3DQ10	N1 DDR3_D14
"IO_L7N B6 DIO FPGA 38	IO_L34P_A13_M1WE	\$13	IO_L35N_M3DQ11	M3 DDR3 D9
IO_LSP A6 DIO PULL 38	IO_L34N_A12_M1BA2	F17 DIN FPGA 21	IO_L36P_M3DQ8	M1 DDR3 D10
IO_LSN_VREF	IO_L35P_A11_M1A7	210	IO_L36N_M3DQ9	L2 DDR3 D0
"IO_L9P	IO_L35N_A10_M1A2	THIS DIN FPGA 18	IO_L37P_M3DQ0	L1 DDR3 D2
*IO_L9N C7 DIO FPGA 37	IO_L36P_A9_M1BA0	H14	IO_L37N_M3DQ1	K2 DDR3 D3
IO_LIOP	IO_L36N_A8_M1BA1	H15 DIN_FPGA_20	IO_L38P_M3DQ2	K1 DDR3_D1
IO_LION DB DIO FPGA 35	IO_L37P_A7_M1A0	H16	IO_L38N_M3DQ3	L4 DDR3 DQS0 P
	IO_L37N_A6_M1A1	G16 DIN_FPGA_17	IO_L39P_M3LDQS	L3 DDR3 DQS0 N
IO_LIIN GG8	IO_L38P_A5_M1CLK	G18	IO_L39N_M3LDQSN	3 DDR3 D5
10_L32P	IO_L38N_A4_M1CLKN	DIN_FPGA_14	IO_L40P_M3DQ6	1 DDR3_D4
TIO_L32N TES DIO FPGA 33	IO_L39P_M1A3	2214	IO_L40N_M3DQ7	H2 DDR3 D6
IO_L33P AB DIO PULL 33	IO_L39N_M1ODT	DIN_FPGA_6	IO_L41P_GCLK27_M3DQ4	H1 DDR3 D7 K4 DDR3 DM1
IO_L33N D9 DIO_FPGA_39	IO_L40P_GCLK11_M1A5	[13	IO_L41N_GCLK26_M3DQ5	K4 DDR3_DM1
IO_L34P_GCLK19 C9 DIO_PULL_39	IO_L40N_GCLK10_M1A6	K15 DIN_FPGA_9	IO_L42P_GCLK25_TRDY2_M3UDM	K3 DDR3_DM0
IO_L34N_GCLK18 B9 DIO_FPGA_36	IO_L41P_GCLK9_IRDY1_M1RASN	K15 DIN_FPGA_9	IO_L42N_GCLK24_M3LDM	15 DDR3_RAS
IO_L35P_GCLK17 A9 DIO_PULL_36	IO_L41N_GCLK8_M1CASN	L15 DIN_FPGA_8	IO_L43P_GCLK23_M3RASN	K5 DDR3_CAS
D11 DIO FPGA 27	IO_L42P_GCLK7_M1UDM	116	IO_L43N_GCLK22_IRDY2_M3CASN	H4 DDR3_A5
IO_L36P_GCLK15 C11 DIO_PULL_27	IO_L42N_GCLK6_TRDY1_M1LDM	H17 DIN FPGA 16	IO_L44P_GCLK21_M3A5	H3 DDR3_A6
IO_L36N_GCLK14 C10 DIO_FPGA_32	IO_L43P_GCLK5_M1DQ4	1118	IO_L44N_GCLK20_M3A6	17 DDR3_A3
IO_L37P_GCLK13 410 DIO_PULL_32	IO_L43N_GCLK4_M1DQ5 IO_L44P_A3_M1DQ6	DIN_FPGA_11	IO_L45P_M3A3 IO_L45N_M3ODT	K6 DDR3_ODT0
	IO_L44P_A5_M1DQ6	118	IO_L46P_M3CLK	G3 DDR3_CK_P
IO_L38P	IO_L45P_A1_M1LDQS	KIT DIN FPGA 13	IO L46N M3CLKN	G1 DDR3_CK_N
IO L39P	IO L45N AO M1LDQSN	K18	IO_L47P_M3A0	J7 DDR3_A0
IO I SON TOTAL ST	IO_L46P_FCS_B_M1DQ2	DIN_FPGA_12	IO_L47N_M3A1	16 DDR3_A1
	IO L46N FOE 8 M1DQ3	118	IO L48P M3BAO	F2 DDR3_BA0
10 1401 17 10	IO_L47P_FWE_B_M1DQ0	M16 DIN_FPGA_7	IO_L48N_M3BA1	F1 DDR3_BA1
ID LATE B12 DIO FPGA SU	IO_L47N_LDC_M1DQ1	M18 DIN_FPGA_2	IO_L49P_M3A7	H6 DDR3_A7 H5 DDR3_A2
IN LANK THE DIO FOLL SU	IO L4SP HDC M1DQS	N17 DIN FPGA 2	IO L49N M3A2	F3 DDR3 A2
*IO_L42P 4E11	IO_L4SN_M1DQ9	P1 DIN_FPGA_1	IO_L50P_M3WE	
	IO_L49P_M1DQ10	P10 DIN_FPGA_1	IO_L50N_M3BA2	
10_L47P	IO_L49N_M1DQ11	N15 DIN_FPGA_5	IO_L51P_M3A10	F4 DDR3_A10 F3 DDR3_A4
*IO_L47N -4C13	IO L50P M1UDQS	This	IO L51N M3A4	D2 DDR3 A8
*IO_L50P <12	IO_LSON_M1UDQSN	THE DIAL EDGA A	IO_L52P_M3A8	D1 DDR3 A9
*10_L50N 4112	IO L51P M1DQ12	117 DIN PPGA 4	IO L52N M3A9	H7 DDR3 CKE0
*10_L51P	IO_L51N_M1DQ13	DIN_VREF_H	IO_L53P_M3CKE	G6 DDR3_A12
"IO_LS1N TB14 DIO FPGA 29	IO_L52P_M1DQ14	U18 DIN VREF L	IO_L53N_M3A12	E4 DDR3 RESET
IO_L62P A14 DIO PULL 29	IO_L52N_M1DQ15	TALL DIN EDGA O	IO_L54P_M3RESET	D3 DDR3 A11
IO_L62N_VREF	IO_L53P	9944	IO_L54N_M3A11	E6 DDR3 A13
IO_L63P_SCP7	IO_L53N_VREF	L14 DIN_FPGA_3	IO_L55P_M3A13	5 DDR3 A14
IO_L63N_SCP6	IO_L61P	M13	IO_L55N_M3A14	15 DDR3_A14
IO_L64P_SCP5	IO_L61N		IO_L83P	
IO_L64N_SCP4 D14 DIO FPGA 24	IC6C XC65LX25-2C5G324	ť	IO_L83N_VREF	C1 DDR3_VREF
IU_LOSP_SCPS C14 DIO PULL 24			IC6E XC65LX25-2C5G3	24
IO_L65N_SCP2 416 DIO EPGA 28				
IO_L66P_SCP1 A16 DIO PULL 28			DDR3_RZQ R103 GND DDR3_ZIC	R104 GND
IO_L66N_SCP0			100 1%	100
IC6B XC6SLX25-2CSG324			200	No Load

(https://reference.digilentinc.com/_detail/digital_discovery/dd_21fpgabanks01and3.png?id=reference%3Ainstrumentation%3Adigital-discovery%3Areference-manual)

Figure 21. FPGA banks 0, 1 and 3.

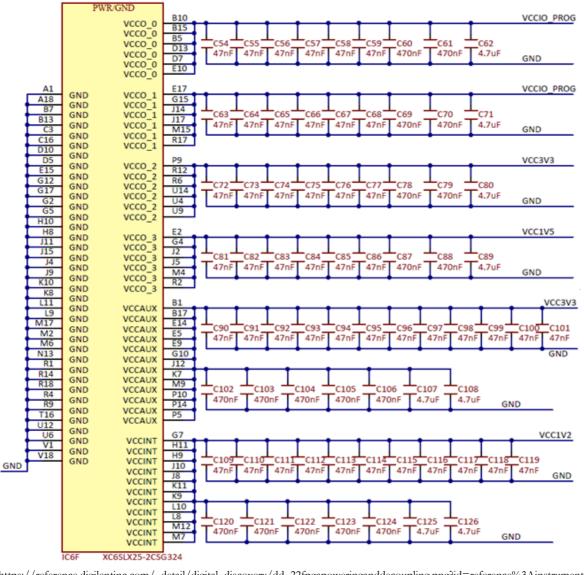
Figure 22 shows the voltage rails and decoupling for the FPGA.

The internal core of the FPGA is supplied 1.2V.

Banks 0 and 1 are supplied with the programmable VCCIO_PROG. By setting this from 1.2V to 3.3V, both inputs and IOs are set to be compatible with the I/O standard LVCMOS of the respective voltage. Notice that a protected version of VCCIO_PROG is also available to the user, as VCCIO_USR. This can be used to supply the Device/Circuit Under Test.

Bank 3 is supplied 1.5V, for compatibility with the DDR3 IC.

Bank 2 and VCCAUX are supplied 3.3V.



(https://reference.digilentinc.com/_detail/digital_discovery/dd_22fpgapoweringanddecoupling.png?id=reference%3Ainstrumentation%3Adigitaldiscovery%3Areference-manual)

Figure 22. FPGA powering and decoupling.

8. Accessories

The Digital Discovery package includes;

- One 2×16 fly-wire assembly (datasheet (https://reference.digilentinc.com/_media/reference/instrumentation/digital-discovery/250-096_sn-1050323-1.pdf)), for the DIN_USR connector. 24DIN signals (various colors), 8 <u>GND_()</u> wires (black). The connector is keyed so that the correct pins are connected to the correct color wires.
- One 2×6 fly-wire assembly (datasheet (https://reference.digilentinc.com/_media/reference/instrumentation/digital-discovery/250-097_sn160718-1.pdf)), for the DIO connectors. Each one includes two VCCIO_USR (red) wires, two <u>GND ()</u> (black) wires and 8 (colored) signal wires. It has a 2×6 female connector for the Digital Discovery DIN connector, and 1 pin female connectors for the device under test.

Additional Accessories that can be added at checkout;

• One High Speed Adapter, for the DIN_USR connector. The High Speed Adapter is an alternative to the 2×16 fly-wire assembly. It provides access for 24 twisted cables. The adapter is not keyed, and both orientations can be used as the twisted wires are not color coded. However, if the adapter is plugged in with the ground arrows pointing down, the pins will be located as shown below:

	+ GROUND + GROUND + GROUND + 0 1 2 3 J1 8 9 10 11 J3 16 17 18 19 J5	
Digital Inputs:	DIGITAL DISCOVERY HIGH-SPEED ADAPTER DIGILENT Inc.	
		. AUD

(https://reference.digilentinc.com/_detail/reference/instrumentation/digital-discovery/dd-high-speed-adapter-diagram-600.png? id=reference%3Ainstrumentation%3Adigital-discovery%3Areference-manual)

 High Speed Logic Probes (datasheet (https://reference.digilentinc.com/_media/reference/instrumentation/digital-discovery/250-104_dp_2.54_3.pdf)). Each twisted cable has a <u>GND_()</u> (black) wire twisted to a DIN_USR (colored) wire. The wire connects to the High Speed Adapter via a 2 pin female header, and two 1 pin female connectors to the device under test. A 100Ω resistor is embedded in the signal wire, on the end closest to the device under test. All <u>GND_()</u> wires should be connected to Ground of the device under test.

9. Features and Performances

This chapter shows the features and performances as described in the Digital Discovery Datasheet. Footnotes add detailed information and annotate the HW description in this Manual.

9.1. Logic Analyzer

- 24 high-speed input channels (DIN0...23), accessible through one 2×16 connector, used with the Logic Analyzer in WaveForms ($560k\Omega | | 10pF$)
- 16 digital I/Os (DIO24...39) arranged in two Pmod-style (2×6) connectors, used with the Logic Analyzer in WaveForms 1)
- 800MSps input sample rate when using maximum 8 inputs (and the High Speed Adapter), 400 MSps with maximum 16 inputs (with the High Speed Adapter), 200MSps and lower with maximum 32 inputs ²⁾
- User programmable input and output LVCMOS voltage levels from 1.2V to 3.3V ³⁾ (5V compatible ⁴⁾)
- 100MHz signal input bandwidth
- 2Gbit DDR3 acquisition buffer for Logic Analyzer
- Multiple trigger options including pin change, bus pattern, etc ⁵⁾
- Digital Bus Analyzers (SPI, I²C, UART, Parallel)

9.2. Multi-purpose Digital I/O

- 16 digital I/Os arranged in two Pmod-style (2×6) connectors.
- Each of the 16 pins can be configured for input (Logic analyzer) or set as output ⁶.
- Algorithmic pattern generator (no buffers used) 7)
- Custom pattern buffer/ch.: 32Ksamples
- ROM () Logic for implementing user defined Boolean functions and State Machines
- Bus Protocol Controllers (SPI, UART, I²C)
- 100MSps max. output sample rate (50MHz maximum output frequency).
- Automatic or manual strength and slew settings for outputs.⁸⁾
- User programmable logic I/O levels from 1.2V to 3.3V (5V compatible) ^{9),10)}.

9.3. Other features

- USB bus powered
- User power supplies, 1.2V to 3.3V, available in the two Pmod-style connectors (100mA max)
- · Twisted wire high-speed cable option for input channels to insure signal integrity
- Free WaveForms software runs on Windows, MacOS, and Linux
- · Cross-triggering between Logic Analyzer, Pattern Generator or external trigger
- · Data file import/export using standard formats
- 80X80X25mm, 80g (without accessories)
- includes: USB cable, fly-wire accessory

Written by Mircea Dabacan, PhD, Technical University of Cluj-Napoca Romania

¹⁾ The 16 DIO lines are primarily intended for the Pattern Generator, protocol controllers and Static IO instruments. For user convenience, some or all of them can be used by the Logic Analyzer also (see footnote 2). However, DIO input circuitry is different compared to DIN. Even more, when driving a DIO pin with the Pattern Generator and reading it back with the Logic Analyzer, the

signal is read at the FPGA pin and does not propagate trough the external DIO circuitry. Consequently, when combining DIN and DIO pins in the Logic Analyzer, misalignments can be observed, at high acquisition rate.

²⁾ Available combinations in WaveForms: - 200MHz, DIN0...23, DIO24...31 - 200MHz, DIO24...39, DIN0...15 - 400MHz, DIN0... 15 - 400MHz, DIO24...39 - 800MHz, DIN0...7 - 800MHz, DIO24...31

3) The FPGA DIN and DIO pins are set to LVCMOS18_JEDEC IOSTANDARD. The supply voltage of the associated FPGA banks is set (by user) to any value from 1.2V to 3.3V. The threshold level (at the FPGA pins) is about 45% of the bank supply voltage. For standard voltages of: 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, the threshold levels (at the FPGA pins) are: 0.58V, 0.7V, 0.82V, 1.1V and 1.42V respectively.

⁴⁾ Setting the voltage to 3.3V, 5V logic inputs are tolerated but the input threshold is 1.42V. LVCMOS 3.3V output signals are compatible to most external logical circuits supplied with 5V.

⁵⁾ Trigger Detectors and Trigger Distribution Networks are implemented in the FPGA. This allows real time triggering and cross-triggering of different instruments within the Digital Discovery device. Using external Trigger inputs/outputs, cross-triggering between multiple Digital Discovery devices is possible.

9. The 16 DIO lines are primarily intended for the Pattern Generator, protocol controllers and Static IO instruments. For user convenience, some or all of them can be used by the Logic Analyzer also (see footnote 2). However, DIO input circuitry is different compared to DIN. Even more, when driving a DIO pin with the Pattern Generator and reading it back with the Logic Analyzer, the signal is read at the FPGA pin and does not propagate trough the external DIO circuitry. Consequently, when combining DIN and DIO pins in the Logic Analyzer, misalignments can be observed, at high acquisition rate.

7) Real time implemented in the FPGA configuration.

8) The FPGA DIN and DIO pins are set to LVCMOS18_JEDEC IOSTANDARD. The supply voltage of the associated FPGA banks is set (by user) to any value from 1.2V to 3.3V. The threshold level (at the FPGA pins) is about 45% of the bank supply voltage. For standard voltages of: 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, the threshold levels (at the FPGA pins) are: 0.58V, 0.7V, 0.82V, 1.1V and 1.42V respectively.

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¹⁰⁾ Setting the voltage to 3.3V, 5V logic inputs are tolerated but the input threshold is 1.42V. LVCMOS 3.3V output signals are compatible to most external logical circuits supplied with 5V.

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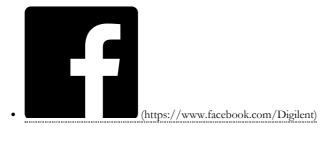
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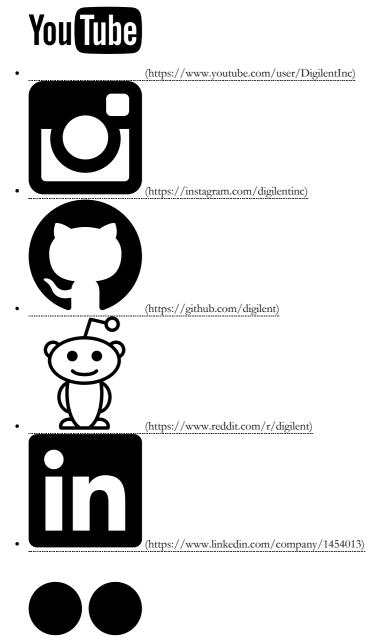
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