PROCESSOR-CENTRIC EXTENSIBLE PLATFORMS FOR POWERFUL, SCALABLE, COST-EFFICIENT EMBEDDED DESIGNS

THE FIRST GENERATION OF EXTENSIBLE PROCESSING PLATFORMS: A NEW LEVEL OF PERFORMANCE, FLEXIBILITY AND SCALABILITY

Embedded Systems Challenges

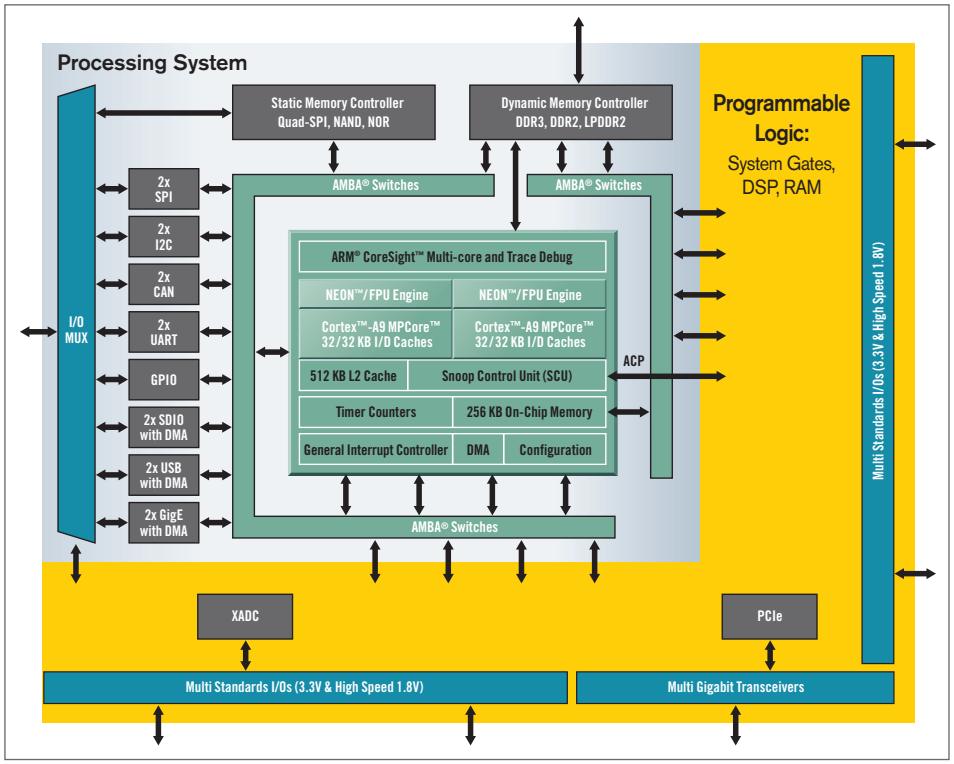
- Critical need to build in more differentiation in less time, which limits the use of standard products
- Increasingly complex functions and exploding demand for signal-processing performance
- Balancing performance, power, cost and flexibility without sacrificing results
- Reducing costs through hardware and software design reuse across a common platform for multiple products
- Flexibility to comply with continually changing industry standards, regulations and market needs

Xilinx Solution

- Powerful foundation for system on a chip (SoC): dual ARM®Cortex™-A9 processing system including hardened memory controllers and peripherals, along with Xilinx 7 series programmable logic
- Size, power, throughput and cost advantages in a flexible single-chip architecture
- Best-in-class tools, operating system support, and ecosystem leveraging the ARM connected community
- A complete product family that enables solutions to scale features and reduce costs within a defined SW programming model – accelerating time to market
- Advanced software and hardware programmability, enabling unique system partitioning and unparalleled performance while accommodating late product definition changes and standards evolutions

The Xilinx® Zynq™-7000 Extensible Processing Platform (EPP) redefines the possibilities for embedded systems, giving system and software architects and developers a flexible platform to launch their new solutions and traditional ASIC and ASSP users an alternative that aligns with today's programmable imperative. The new class of product elegantly combines an industry-standard ARM®processor-based system with Xilinx 28nm programmable logic—in a single device. The processor boots first, prior to configuration of the programmable logic. This, along with a streamlined workflow, saves time and effort and lets software developers and hardware designers start development simultaneously.

ZYNQ-7000 EPP



ZYNQ™

XILINX®

The Zynq-7000 EPP makes market- and application-specific platforms easier to use, modify, and extend thanks to the programmable logic. These new devices build on Xilinx-pioneered development methodologies to maximize the value of the break-through levels of integration, power efficiency, and high performance. Integrating the industry-standard dual ARM® Cortex™-A9 MPCore™ also gives designers access to the ARM IP and software ecosystem. Design teams can get started today using Xilinx ISE® Design Suite, industry-standard operating systems, and best-in-class productivity tools from the industry's leading solution providers.

Breakthrough Single-Chip Platforms

The architecture of the Zynq-7000 EPP offers unrivaled features and performance while driving down cost and power requirements. The ARM dual-core Cortex™-A9 processor is enhanced with the NEON engine, a single and double-precision vector floating-point unit and a large set of peripherals including memory controllers, CAN, USB, Gigabit, Ethernet, SD-SDIO, UARTs, analog-to-digital converters and more. Its high-performance multi standard I/Os and multi-gigabit transceivers offer a wide range of connectivity options allowing designers to use Zynq-7000 EPP devices in most applications. The programmable logic portion of Zynq-7000 EPP devices leverages the Xilinx 7 series programmable logic. This allows designers currently developing on the Xilinx 7 series to seamlessly port their FPGA designs to Zynq-7000 EPP devices. Z-7010 and Z-7020 are based on the Artix™-7 FPGA fabric, and Z-7030 and Z-7045 are based on the Kintex™-7 FPGA fabric.

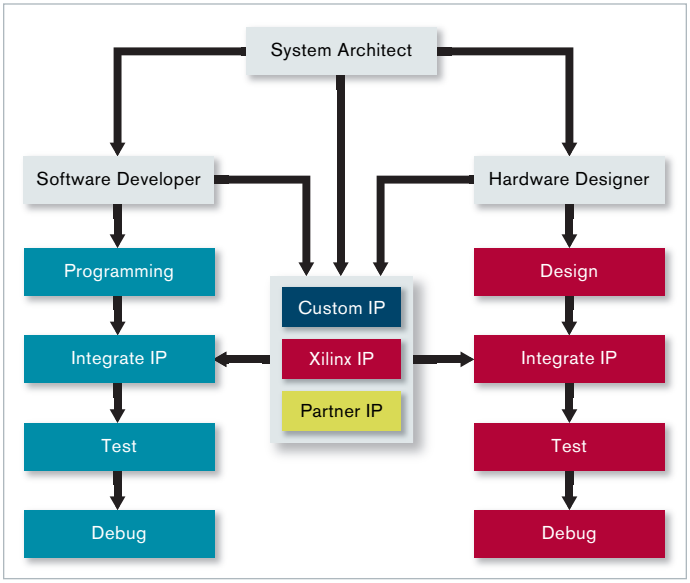
But the real value of the Zynq-7000 EPP family lies in the tight integration of its programmable logic with the processing system. The interface between the processing system and the programmable logic is built on nine AXI interfaces and many control signals (like DMA and Interrupts) which represents more than 3000 interconnections. The high throughput interface eliminates the bottleneck that plague two-chip ASSP-FPGA solutions and allows designers to easily extend the processing system capabilities. This enables designers to not only build their own custom device by adding peripherals in the programmable logic, but also increase the overall system performance by allowing designers to uniquely partition HW and SW functions by creating custom accelerators.

Zynq-7000 Product Table (Software View)

	Device Name	Z-7010	Z-7020	Z-7030	Z-7045
	Part Number	XC7Z010	XC7Z020	XC7Z030	XC7Z045
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™			
	Processor Extensions	NEON™ and Single/Double Precision Floating Point			
	Maximum Frequency	800 MHz			
	L1 Cache	32 KB Instruction, 32 KB Data per processor			
	L2 Cache	512 KB			
	On-Chip Memory	256 KB			
	External Memory Support	DDR3, DDR2, LPDDR2			
	External Static Memory Support	2x QSPI-SPI, NAND, NOR			
	DMA Channels	8 (4 dedicated to Programmable Logic)			
	Peripherals	2x USB 2.0 (OTG) w/DMA, 2x Tri-mode Gigabit Ethernet w/DMA, 2x SD/SDIO w/DMA, 2x UART (2), 2x CAN2.0B, 2x I2C, 2x SPI, 4x 32b GPIO			
	Security	AES and SHA 256b for secure boot			
	Peripherals and Static Memory Multiplexed I/O[1]	54			
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts			
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix™-7 FPGA	Artix™-7 FPGA	Kintex™-7 FPGA	Kintex™-7 FPGA
	Programmable Logic Cells (Approximate ASIC Gates[3])	28K Logic Cells (~430K)	85K Logic Cells (~1.3M)	125K Logic Cells (~1.9M)	350K Logic Cells (~5.2M)
	Extensible Block RAM (# 36 Kb Blocks)	240KB (60)	560KB (140)	1,060KB (265)	2,180KB (545)
	Programmable DSP Slices (18x25 MACCs)	80	220	400	900
	Peak DSP Performance (Symmetric FIR)	58 GMACS	158 GMACS	480 GMACS	1080 GMACS
	PCI Express® (Root Complex or Endpoint)	—	—	Gen2 x4	Gen2 x8
	Agile Mixed Signal (AMS)/XADC	2x 12 bit, 1 MSPS ADCs with up to 17 Differential Inputs			
	Security	AES and SHA 256b for secure configuration			
	Multi-Standards 3.3V I/O[2]	100	200	250	350
	Serial Transceivers[2]	—	—	4	16

Notes:
1. Static memory interface combined with the usage of many peripherals could require more than 54 I/Os. A designer can use the Programmable Logic I/Os.
2. Total Number of I/O and Transceivers depends on package used.
3. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.
4. Preliminary product information. Subject to change. Please contact your Xilinx representative for the latest information.

TOOL DEVELOPMENT FLOW



Designing Software and Hardware in Parallel

The Zynq-7000 EPP family allows software and hardware designs to be done in parallel. System architects can optimize and differentiate systems on a cost-efficient, power-optimized platform. Logic designers have a familiar register transfer-level (RTL) environment with unprecedented features and flexibility to extend capabilities and performance. And software developers can program in a familiar environment to build and debug applications.

Familiar Design Environments Enable Optimized Results

Software designers can start designing from day one. Using the Eclipse environment-based Software Developers Kit (SDK) designers can:

- Create applications, middleware, driver software code and Board Support Packages (BSP) without a finalized target hardware
- Compile, build and debug standalone software applications

Software designers also benefit from the support for industry-standard commercial distributions as well as open source, operating systems software and development tools ranging from virtualizers, IDEs, compilers, debuggers, profilers and libraries.

Hardware designers can maximize productivity by using familiar hardware development tools. With Xilinx's industry-standard ISE Design Suite, designers can:

- Create, synthesize and generate programmable logic configuration
- Configure the processing system and enhance designs using a built-in AXI4 IP repository of simple to more complex peripherals and hardware acceleration functions—all using the Xilinx Embedded Developers Kit (EDK)

Hardware designers also benefit from the support for industry-standard design entry, HDL simulators, design rule checkers and hardware-assisted verification synthesis to board-level design and verification tools.

System designers benefit from a wide-range of support including:

- Xilinx and Alliance Member development hardware including generic and application-specific development kits
- Market-specific Targeted Design Platforms which allow system developers to start design efforts with an integrated targeted system solution
- Xilinx and 3rd party IP including connectivity, DSP, embedded and video processing options
- C-to-gate and ESL tools improve system partitioning by taking compute intensive software code and mapping it directly into optimized and powerful hardware accelerators

Speeding Highly Differentiated Applications to Market

By simplifying and accelerating embedded systems development through the use of industry-standard tools and a large choice of IP from Xilinx and its ecosystem partners, Xilinx gives designers more time to focus on system features. More time for optimizations, algorithm development, and feature extensions ultimately creates highly differentiated products and more fully extracts the power of the tightly coupled programmable logic.

This allows designers to drive up performance while controlling power consumption and costs, or minimize power and cost without sacrificing performance. The range also enables designers to address a portfolio of products that scale from cost-effective to feature-rich and high-performance—all from a single platform.

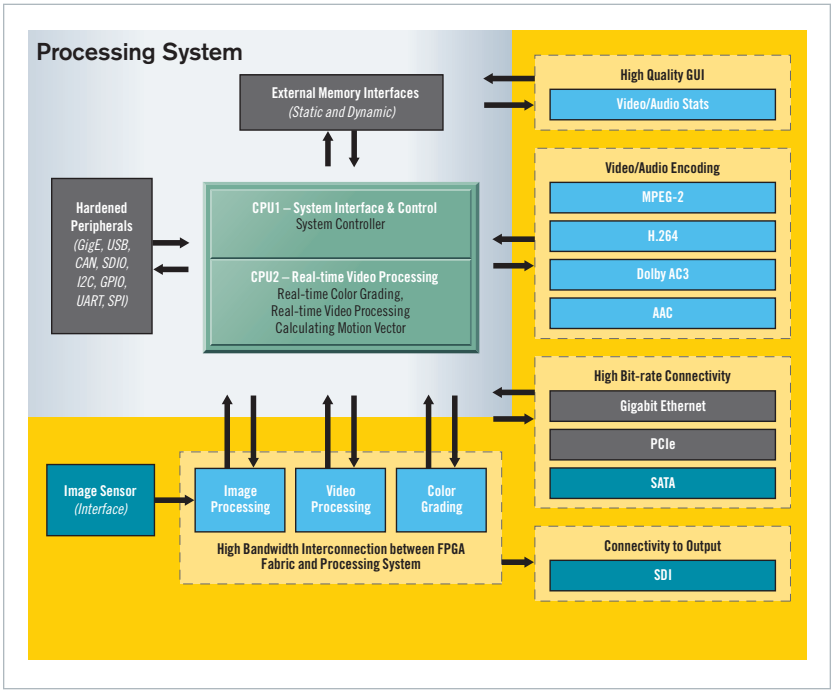
MAPPING APPLICATIONS TO EACH ZYNQ-7000 EPP DEVICE

CLUSTER	MARKET	KEY APPLICATIONS	SAME PROCESSING SYSTEM Different Programmable Logic Densities ● Optimal for application			
			Z-7010	Z-7020	Z-7030	Z-7045
Intelligent Video	Auto	Driver Assistance, Driver Information, Infotainment	●	●		
	Consumer	Business-class Multi-function Printers	●	●	●	
	ISM	IP and Smart Cameras	●	●	●	
		Medical Diagnostics, Monitoring and Therapy	●	●		
		Medical Imaging	●		●	●
	Broadcast	Prosumer/Studio Cameras, Transcoders		●	●	●
	A&D	Video/Night Vision Equipment	●	●		
Comms	A&D	Milcomms, Cockpit & Instrumentation		●	●	●
	Wireless	LTE Radio, Basband, Enterprise Femto		●	●	●
	Wired	Routers, Switches, Multiplexers, Edge Cards			●	●
Control	ISM	Motor Control, Programmable Logic Controller (PLC)	●	●	●	
	A&D	Missiles, Smart Munitions			●	●
Bridging	Broadcast	Edge QAMs, Routers, Switchers, Encoders/Decoders			●	●
	ISM	Industrial Networking	●	●	●	

While each device in the Zynq-7000 EPP family contains the same ARM dual-core Cortex-A9 MPCore based processing system, programmable logic and I/O resources vary between devices and serve a wide range of applications.

The Zynq-7000 EPP family serves many applications for various markets. For some applications, flexibility and performance are the key factors making Zynq-7000 EPP devices the best option. Others will benefit from the power and space savings that this integrated solution has to offer. Here are a few key examples where Zynq-7000 EPP devices are ideally suited.

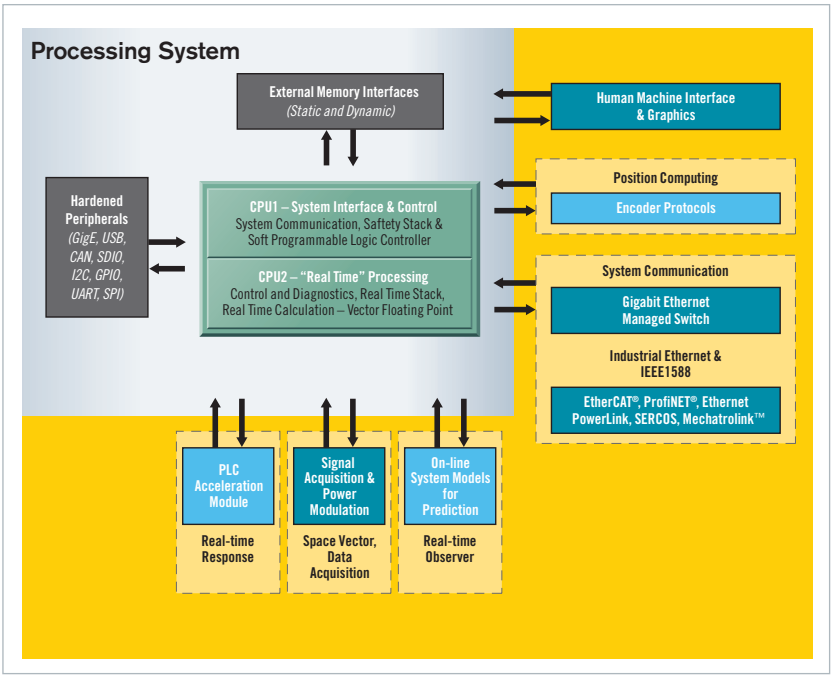
BROADCAST CAMERA APPLICATION EXAMPLE



Zynq-7000 EPP devices provide very high bit-rate bandwidth for high-accuracy video processing and analytics in broadcast-level camera systems.

- Zynq-7000 EPP devices improve time to market and accommodate for broadcasting standards and future algorithms evolution.
- The high integration in the Zynq-7000 EPP devices enables system power consumption savings and cost reduction.
- Dual ARM Cortex-A9 with NEON and dual precision offer high levels of performance for algorithmic processing and video data compression encoding (e.g. MPEG-2, H.264).
- Processing system to DSP-rich programmable logic interconnect allows high bandwidth, low latency interface to enable hardware accelerations of most video processing and video analytics functions.

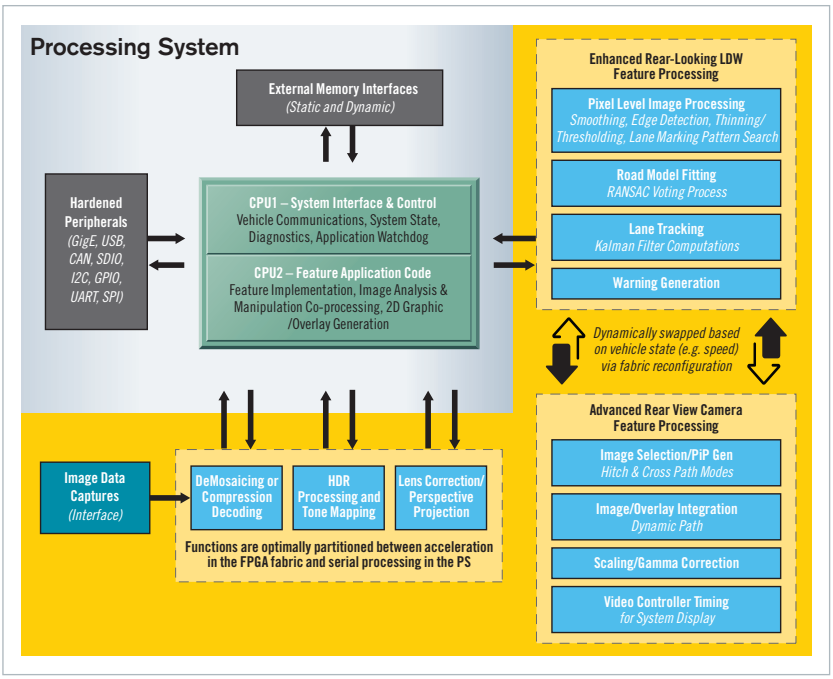
INDUSTRIAL MOTOR CONTROL APPLICATION EXAMPLE



Zynq-7000 EPP devices offer a unique blend of performance and flexibility to meet the high-processing demands and integration required for current and future motor control systems.

- Designers can accelerate time to market while enabling in-system programmability and ensuring "future proofing" of products.
- The scalability between the Z-7010 and Z-7020 EPP devices allow customers to offer bundled product solutions and support varying motor types from a single platform.
- Zynq-7000 EPP devices possess all the elements required for motor control (powerful processors, peripherals, analog-to-digital converter) which offer an integrated cost effective solution for tomorrow's greener industrial solutions.
- Tight coupling of the processing system and programmable logic enable high bandwidth low latency for real-time industrial networking interfaces and motor control hardware accelerators in a single device.

SINGLE-CAMERA / MULTI-FEATURE DRIVER ASSISTANCE APPLICATION EXAMPLE



The Zynq-7000 EPP family addresses the stringent video processing and analytics requirements for current and future driver assistance systems.

- The programmable logic accommodates emerging camera interface standards and evolving DA processing algorithms while also improving time to market.
- The tight integration provides a high bandwidth and low-latency interface for unprecedented optimization of HW/SW partitioning for computationally intensive video/image processing functions.
- Leveraging the dynamic reconfiguration capability of Zynq-7000 EPP devices allows features like rear view camera and lane departure warning systems to be dynamically swapped based on vehicle state (e.g. speed) thereby reducing total required logic and system cost.
- The scalability of the Zynq-7000 EPP family allows designers to chose between Z-7010 and Z-7020 devices and offer solutions that are ideally tailored and cost-optimized to each DA system.
- Dual Cortex-A9 processors with dual precision floating point and NEON engines offer complex algorithmic processing and support for video data compression codecs.
- Automotive compatible SoC architecture is supported by key hardened peripherals like CAN and Ethernet.

Zynq-7000 Product Table (Hardware View)

	Device Name	Z-7010		Z-7020		Z-7030			Z-7045		
	Part Number	XC7Z010		XC7Z020		XC7Z030			XC7Z045		
	Processing System (Dual ARM® Cortex™-A9 MPCore™ with NEON™ & Double Precision FPUCache, Memory Controllers, DMA, Security and Peripherals)	Same processing system for all devices									
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix™-7 FPGA		Artix™-7 FPGA		Kintex™-7 FPGA			Kintex™-7 FPGA		
	Programmable Logic Cells (Approximate ASIC Gates[2])	28K Logic Cells (~430K)		85K Logic Cells (~1.3M)		125K Logic Cells (~1.9M)			350K Logic Cells (~5.2M)		
	Logic Cells	28,160		85,120		125,760			349,760		
	Look-Up Tables LUTs	17,600		53,200		78,600			218,600		
	Flip Flops	35,200		106,400		157,200			437,200		
	Extensible Block RAM (# 36 Kb Blocks)	240 KB (60)		560 KB (140)		1,060 KB (265)			2,180KB (545)		
	Programmable DSP Slices (18x25 MACCs)	80		220		400			900		
	Peak DSP Performance (Symmetric FIR)	58 GMACS		158 GMACS		480 GMACS			1080 GMACS		
	PCI Express® (Root Complex or Endpoint)	—		—		Gen2 x4			Gen2 x8		
	Agile Mixed Signal (AMS)/XADC	2x 12 bit, 1 MSPS ADCs with up to 17 Differential Inputs									
	Security [1]	AES and SHA 256b for secure configuration									
Packages	Package Type	CLG400	CLG484	CLG400	CLG484	FBG484	FBG676	FFG676	FBG676	FFG676	FFG900
	Size (mm)	17x17	19x19	17x17	19x19	23x23	27x27	27x27	27x27	27x27	31x31
	Pitch (mm)	0.8	0.8	0.8	0.8	1.0	1.0	1.0	1.0	1.0	1.0
	Processing System Total I/Os (includes Multiplexed I/Os)	130	130	130	130	130	130	130	130	130	130
	Multi-Standards and Multi-Voltage SelectIO Interfaces (1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V)	100	100	120	200	100	100	100	100	100	200
	Multi-Standards and Multi-Voltage High Performance SelectIO Interfaces (1.2V, 1.35V, 1.5V, 1.8V)	—	—	—	—	63	150	150	150	150	150
	Serial Transceivers	—	—	—	—	4	4	4	8	8	16
	Maximum Transceiver Speed (Speed Grade Dependent)	N/A	N/A	N/A	N/A	6.6Gbps	6.6Gbps	12.5Gbps	6.6Gbps	12.5Gbps	12.5Gbps

Notes:
1. Security is shared by the Processing System and the Programmable Logic.
2. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.
3. Preliminary product information. Subject to change. Please contact your Xilinx representative for the latest information.

Take the NEXT STEP

For more information about the Zynq-7000 family, visit **www.xilinx.com/zynq**

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Printed in the U.S.A. PN 2476-3