The LM118 series are precision high speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

The LM118 series has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over 150V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μs.

The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. These devices are easy to apply and offer an order of magnitude better AC performance than industry standards such as the LM709.

The LM218-N is identical to the LM118 except that the LM218-N has its performance specified over a −25°C to +85°C temperature range. The LM318-N is specified from 0°C to +70°C.
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>LM118-N/LM218-N</th>
<th>LM318-N</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>±20V</td>
<td></td>
<td></td>
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<tr>
<td>Power Dissipation</td>
<td></td>
<td></td>
<td>500 mW</td>
<td></td>
</tr>
<tr>
<td>Differential Input Current</td>
<td>±10 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage</td>
<td>±15V</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Output Short-Circuit Duration</td>
<td>Continuous</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td></td>
<td>−55°C to +125°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LM218-N</td>
<td></td>
<td>−25°C to +85°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LM318-N</td>
<td></td>
<td>0°C to +70°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td></td>
<td>−65°C to +150°C</td>
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<td></td>
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<tr>
<td>Lead Temperature (Soldering, 10 sec.)</td>
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<td></td>
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</tr>
<tr>
<td>TO-99 Package</td>
<td></td>
<td></td>
<td>300°C</td>
<td></td>
</tr>
<tr>
<td>PDIP Package</td>
<td></td>
<td></td>
<td>260°C</td>
<td></td>
</tr>
<tr>
<td>Soldering Information</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Soldering (10 sec.)</td>
<td></td>
<td></td>
<td>260°C</td>
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</tr>
<tr>
<td>SOIC Package</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vapor Phase (60 sec.)</td>
<td></td>
<td></td>
<td>215°C</td>
<td></td>
</tr>
<tr>
<td>Infrared (15 sec.)</td>
<td></td>
<td></td>
<td>220°C</td>
<td></td>
</tr>
<tr>
<td>ESD Tolerance</td>
<td></td>
<td></td>
<td>2000V</td>
<td></td>
</tr>
</tbody>
</table>

(1) Refer to RETS118X for LM118H and LM118J military specifications.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) The maximum junction temperature of the lm118-n is 150°C, the LM218-N is 110°C, and the LM318-N is 110°C. For operating at elevated temperatures, devices in the LMC package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
(4) The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
(5) For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
(6) Human body model, 1.5 kΩ in series with 100 pF.

### Electrical Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>LM118-N/LM218-N</th>
<th>LM318-N</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Voltage</td>
<td>T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>2 4</td>
<td>4 10</td>
<td>mV</td>
</tr>
<tr>
<td>Input Offset Current</td>
<td>T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>6 50</td>
<td>30 200</td>
<td>nA</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>120 250</td>
<td>150 500</td>
<td>nA</td>
</tr>
<tr>
<td>Input Resistance</td>
<td>T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>1 3</td>
<td>0.5 3</td>
<td>MO</td>
</tr>
<tr>
<td>Supply Current</td>
<td>T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>5 8</td>
<td>5 10</td>
<td>mA</td>
</tr>
<tr>
<td>Large Signal Voltage Gain</td>
<td>T&lt;sub&gt;A&lt;/sub&gt; = 25°C, V&lt;sub&gt;S&lt;/sub&gt; = ±15V</td>
<td>50 200</td>
<td>25 200</td>
<td>V/mV</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>T&lt;sub&gt;A&lt;/sub&gt; = 25°C, V&lt;sub&gt;S&lt;/sub&gt; = ±15V, A&lt;sub&gt;V&lt;/sub&gt; = 1</td>
<td>50 70</td>
<td>50 70</td>
<td>V/μs</td>
</tr>
<tr>
<td>Small Signal Bandwidth</td>
<td>T&lt;sub&gt;A&lt;/sub&gt; = 25°C, V&lt;sub&gt;S&lt;/sub&gt; = ±15V</td>
<td>15</td>
<td>15</td>
<td>MHz</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td></td>
<td>6 15</td>
<td></td>
<td>nV</td>
</tr>
<tr>
<td>Input Offset Current</td>
<td></td>
<td>100 300</td>
<td></td>
<td>nA</td>
</tr>
</tbody>
</table>

(1) These specifications apply for ±5V ≤ V<sub>S</sub> ≤ ±20V and −55°C ≤ T<sub>A</sub> ≤ +125°C (lm118-n), −25°C ≤ T<sub>A</sub> ≤ +85°C (LM218-N), and 0°C ≤ T<sub>A</sub> ≤ +70°C (LM318-N). Also, power supplies must be bypassed with 0.1 µF disc capacitors.
(2) Slew rate is tested with V<sub>S</sub> = ±15V. The lm118-n is in a unity-gain non-inverting configuration. V<sub>IN</sub> is stepped from −7.5V to +7.5V and vice versa. The slew rates between −5.0V and +5.0V and vice versa are tested and specified to exceed 50V/μs.
### Electrical Characteristics (continued)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>LM118-N/LM218-N</th>
<th>LM318-N</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>Input Bias Current</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_A = 125^\circ C$</td>
<td>500</td>
<td></td>
<td>750</td>
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<tr>
<td>Supply Current</td>
<td></td>
<td>4.5</td>
<td></td>
<td>7</td>
</tr>
<tr>
<td>Large Signal Voltage Gain</td>
<td>$V_S = \pm 15\text{V}, V_{\text{OUT}} = \pm 10\text{V}$</td>
<td>25</td>
<td></td>
<td>20</td>
</tr>
<tr>
<td></td>
<td>$R_L \geq 2\text{k}\Omega$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage Swing</td>
<td>$V_S = \pm 15\text{V}, R_L = 2\text{k}\Omega$</td>
<td>$\pm 12$</td>
<td>$\pm 13$</td>
<td>$\pm 12$</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>$V_S = \pm 15\text{V}$</td>
<td>$\pm 11.5$</td>
<td></td>
<td>$\pm 11.5$</td>
</tr>
<tr>
<td>Common-Mode Rejection Ratio</td>
<td></td>
<td>80</td>
<td>100</td>
<td>70</td>
</tr>
<tr>
<td>Supply Voltage Rejection Ratio</td>
<td></td>
<td>70</td>
<td>80</td>
<td>65</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS
LM118-N, LM218-N

Input Current

![Input Current Graph](image)

Temperature (°C)

Figure 1.

Voltage Gain

![Voltage Gain Graph](image)

Supply Voltage (±V)

Figure 2.

Power Supply Rejection

![Power Supply Rejection Graph](image)

Frequency (Hz)

Figure 3.

Input Noise Voltage

![Input Noise Voltage Graph](image)

Noise (nV/√Hz)

Figure 4.

Common Mode Rejection

![Common Mode Rejection Graph](image)

Frequency (Hz)

Figure 5.

Supply Current

![Supply Current Graph](image)

Supply Voltage (±V)

Figure 6.
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

LM118-N, LM218-N

Closed Loop Output Impedance

Current Limiting

Input Current

Unity Gain Bandwidth

Voltage Follower Slew Rate

Inverter Settling Time

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

LM118-N, LM218-N

Large Signal Frequency Response

Open Loop Frequency Response

Voltage Follower Pulse Response

Large Signal Frequency Response

Open Loop Frequency Response

Inverter Pulse Response

Figure 13.

Figure 14.

Figure 15.

Figure 16.

Figure 17.

Figure 18.
Typical Performance Characteristics
LM318-N

Input Current

Voltage Gain

Power Supply Rejection

Input Noise Voltage

Common Mode Rejection

Supply Current

Figure 19.
Figure 20.
Figure 21.
Figure 22.
Figure 23.
Figure 24.
Typical Performance Characteristics (continued)

LM318-N

Closed Loop Output Impedance

Current Limiting

Input Current

Unity Gain Bandwidth

Voltage Follower Slew Rate

Inverter Settling Time
Typical Performance Characteristics (continued)

LM318-N

Large Signal Frequency Response

Open Loop Frequency Response

Voltage Follower Pulse Response

Inverter Pulse Response

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Product Folder Links: LM118-N, LM218-N, LM318-N
AUXILIARY CIRCUITS

Figure 37. Feedforward Compensation for Greater Inverting Slew Rate

Figure 38. Compensation for Minimum Settling Time

Figure 39. Offset Balancing

Figure 40. Isolating Large Capacitive Loads

Figure 41. Overcompensation

*Balance circuit necessary for increased slew.
Slew rate typically 150V/μs.
Do not hard-wire as voltage follower ($R_1 \geq 5 \text{k}\Omega$)

**Figure 42. Fast Voltage Follower**

$C_F = \text{Large}$  
($C_F \geq 50 \text{ pF}$)

*Do not hard-wire as integrator or slow inverter; insert a 10k-5pF network in series with the input, to prevent oscillation.

Do not hard-wire as voltage follower ($R_1 \geq 5 \text{k}\Omega$)

**Figure 43.**

**Figure 44. Fast Summing Amplifier**

**Figure 45. Differential Amplifier**
Figure 46. Fast Sample and Hold

Figure 47. D/A Converter Using Ladder Network

*Optional—Reduces settling time.
ΔOutput zero.
* "Y" zero
+ "X" zero
‡ Full scale adjust.

Figure 48. Four Quadrant Multiplier

Figure 49. D/A Converter Using Binary Weighted Network

*Optional—Reduces settling time.
Figure 50. Fast Summing Amplifier with Low Input Current

Figure 51. Wein Bridge Sine Wave Oscillator

Figure 52. Instrumentation Amplifier
Schematic Diagram
Pin Diagram

Dual-In-Line Package (Top View)
See Package Number J (R-GDIP-T14)

Dual-In-Line Package (Top View)
See Package Number NAB008A, D (R-PDSO-G8), or P (R-PDIP-T8)

Pin connections shown on schematic diagram and typical applications are for TO-99 package.

TO-99 Package (Top View)
See Package Number LMC (O-MBCY-W8)
## REVISION HISTORY

### Changes from Revision B (March 2013) to Revision C

<table>
<thead>
<tr>
<th>Change Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Changed layout of National Data Sheet to TI format</td>
<td>16</td>
</tr>
</tbody>
</table>

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# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM118H</td>
<td>ACTIVE</td>
<td>TO-99</td>
<td>LMC</td>
<td>8</td>
<td>500</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-55 to 125</td>
<td>(LM118H, LM118H)</td>
<td>Samples</td>
</tr>
<tr>
<td>LM118H/NOPB</td>
<td>ACTIVE</td>
<td>TO-99</td>
<td>LMC</td>
<td>8</td>
<td>500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>POST-PLATE</td>
<td>Level-1-NA-UNLIM</td>
<td>-55 to 125</td>
<td>(LM118H, LM118H)</td>
<td>Samples</td>
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<tr>
<td>LM318M</td>
<td>NRND</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>95</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>0 to 70</td>
<td>LM318M</td>
<td>Samples</td>
</tr>
<tr>
<td>LM318M/NOPB</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>95</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>LM318M</td>
<td>Samples</td>
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<tr>
<td>LM318MX/NOPB</td>
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<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
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<td>Level-1-260C-UNLIM</td>
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<td>LM318M</td>
<td>Samples</td>
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<tr>
<td>LM318N/NOPB</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>P</td>
<td>8</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
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<td>Level-1-NA-UNLIM</td>
<td>0 to 70</td>
<td>LM318N</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substances do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp. -** The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish -** Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
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**TAPE AND REEL INFORMATION**

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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</thead>
<tbody>
<tr>
<td>LM318MX/NOPB</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
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<td>2.0</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
# TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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</thead>
<tbody>
<tr>
<td>LM318MX/NOPB</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
LMC (O-MBCY-W8) METAL CYLINDRICAL PACKAGE

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads in true position within 0.010 (0.25) R Ø MMC at seating plane.
D. Pin numbers shown for reference only. Numbers may not be marked on package.
E. Falls within JEDEC MO-002/10-99.
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.

4. This dimension does not include interlead flash.

5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
9. Board assembly site may have different recommendations for stencil design.
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