

FEATURES

- Offset Voltage – Prime Grade: 60 μ V Max
- Offset Voltage – Low Cost Grade (Including Surface Mount Dual/Quad): 75 μ V Max
- Offset Voltage Drift: 0.5 μ V/ $^{\circ}$ C Max
- Input Bias Current: 250pA Max
- 0.1Hz to 10Hz Noise: 0.3 μ V_{P-P}, 2.2pA_{P-P}
- Supply Current per Amplifier: 400 μ A Max
- CMRR: 120dB Min
- Voltage Gain: 1 Million Min
- Guaranteed Specs with \pm 1.0V Supplies
- Guaranteed Matching Specifications
- SO-8 Package – Standard Pinout
- LT1114 in Narrow Surface Mount Package

APPLICATIONS

- Picoampere/Microvolt Instrumentation
- Two and Three Op Amp Instrumentation Amplifiers
- Thermocouple and Bridge Amplifiers
- Low Frequency Active Filters
- Photo Current Amplifiers
- Battery-Powered Systems

DESCRIPTION

The LT[®]1112 dual and LT1114 quad op amps achieve a new standard in combining low cost and outstanding precision specifications.

The performance of the selected prime grades matches or exceeds competitive devices. In the design of the LT1112/LT1114 however, particular emphasis has been placed on optimizing performance in the low cost plastic and SO packages. For example, the 75 μ V maximum offset voltage in these low cost packages is the lowest on any dual or quad non-chopper op amp.

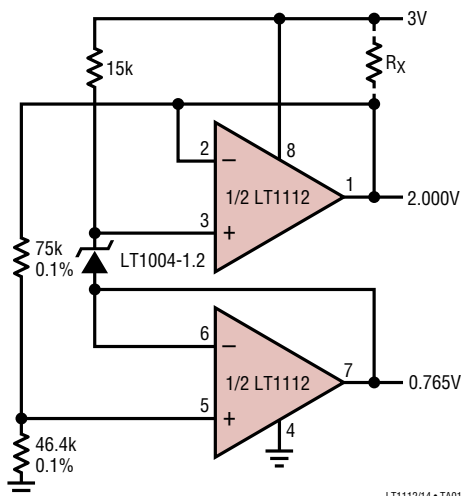
The LT1112/LT1114 also provide a full set of matching specifications, facilitating their use in such matching dependent applications as two and three op amp instrumentation amplifiers.

Another set of specifications is furnished at \pm 1V supplies. This, combined with the low 320 μ A supply current per amplifier, allows the LT1112/LT1114 to be powered by two nearly discharged AA cells.

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 Protected by U.S. Patents 4,575,685; 4,775,884 and 4,837,496

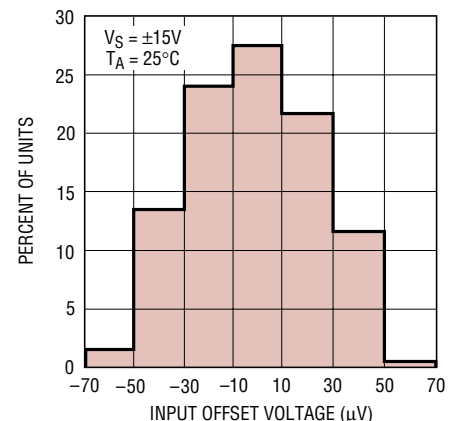
TYPICAL APPLICATION

Dual Output, Buffered Reference (On Single 3V Supply)



TOTAL SUPPLY CURRENT = 700 μ A
 2V REFERENCE: SOURCES 1.7mA, SINKS 5mA
 OPTIONAL $R_X = 300\Omega$ INCREASES SOURCE CURRENT TO 5mA
 0.765V REFERENCE: SOURCES 5mA, SINKS 0.5mA
 TEMPERATURE COEFFICIENT LIMITED BY REFERENCE = 20ppm/ $^{\circ}$ C
 MINIMUM SUPPLY = 2.7V

Distribution of Input Offset Voltage (In All Packages)



LT1112/14 • TA02

ABSOLUTE MAXIMUM RATINGS (Note 1)

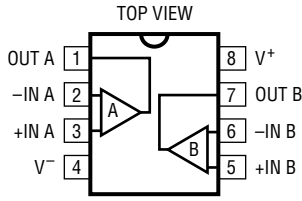
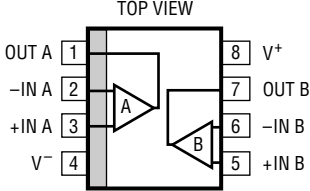
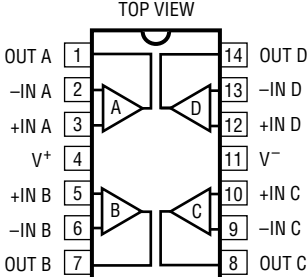
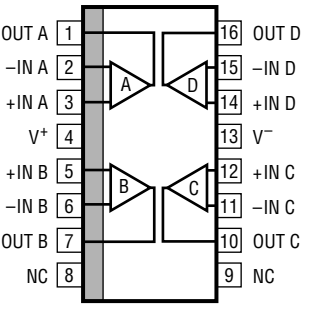
Supply Voltage $\pm 20V$
 Differential Input Current (Note 2) $\pm 10mA$
 Input Voltage (Equal to Supply Voltage) $\pm 20V$
 Output Short-Circuit Duration Indefinite
 Storage Temperature Range $-65^{\circ}C$ to $150^{\circ}C$
 Lead Temperature (Soldering, 10 sec) $300^{\circ}C$
 Operating Temperature Range (Note 11)

Specified Temperature Range (Note 12)

LT1112AM/LT1112M
 LT1114AM/LT1114M (**OBSOLETE**)... $-55^{\circ}C$ to $125^{\circ}C$
 LT1112AC/LT1112C/LT1112S8
 LT1114AC/LT1114C/LT1114S $-40^{\circ}C$ to $85^{\circ}C$
 LT1112I/LT1114I $-40^{\circ}C$ to $85^{\circ}C$
 LT1112MPS8 $-55^{\circ}C$ to $125^{\circ}C$

LT1112AM/LT1112M
 LT1114AM/LT1114M (**OBSOLETE**)... $-55^{\circ}C$ to $125^{\circ}C$
 LT1112AC/LT1112C/LT1112S8
 LT1114AC/LT1114C/LT1114S $-40^{\circ}C$ to $85^{\circ}C$
 LT1112I/LT1114I $-40^{\circ}C$ to $85^{\circ}C$
 LT1112MPS8 $-55^{\circ}C$ to $125^{\circ}C$

PACKAGE/ORDER INFORMATION

 <p>N8 PACKAGE 8-LEAD PDIP</p> <p>$T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 130^{\circ}C/W$</p>	<p>ORDER PART NUMBER</p> <p>LT1112ACN8 LT1112CN8 LT1112IN8</p>	 <p>S8 PACKAGE 8-LEAD PLASTIC SO</p> <p>$T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 190^{\circ}C/W$</p>	<p>ORDER PART NUMBER</p> <p>LT1112S8 LT1112IS8 LT1112MPS8</p> <p>S8 PART MARKING</p> <p>1112 1112I 1112MP</p>
<p>OBSOLETE PACKAGE Consider the N8 Package for Alternate Source</p> <p>J8 PACKAGE 8-LEAD CERDIP $T_{JMAX} = 160^{\circ}C$, $\theta_{JA} = 100^{\circ}C/W$</p> <p>LT1112AMJ8 LT1112MJ8</p>			
 <p>N PACKAGE 14-LEAD PDIP</p> <p>$T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 110^{\circ}C/W$</p> <p>J PACKAGE 14-LEAD CERDIP $T_{JMAX} = 160^{\circ}C$, $\theta_{JA} = 80^{\circ}C/W$ (J)</p> <p>OBSOLETE PACKAGE Consider the N Package for Alternate Source</p> <p>LT1114AMJ LT1114MJ</p>	<p>ORDER PART NUMBER</p> <p>LT1114ACN LT1114CN LT1114IN</p>	 <p>S PACKAGE 16-LEAD PLASTIC SO (NARROW)</p> <p>$T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 150^{\circ}C/W$</p>	<p>ORDER PART NUMBER</p> <p>LT1114S LT1114IS</p>

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 3)	LT1112AM/AC LT1114AM/AC			LT1112M/C/I LT1114M/C/I			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$V_S = \pm 1.0V$		20 40	60 110		25 45	75 130	μV μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			0.3			0.3		$\mu V/Mo$
I_{OS}	Input Offset Current	LT1114S/LT1114IS		50	180		60 75	230 330	pA pA
I_B	Input Bias Current	LT1114S/LT1114IS		± 70	± 250		± 80 ± 100	± 280 ± 450	pA pA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 10)		0.3	0.9		0.3	0.9	μV_{P-P}
	Input Noise Voltage Density	$f_0 = 10Hz$ (Note 10) $f_0 = 1000Hz$ (Note 10)		16 14	28 18		16 14	28 18	nV/\sqrt{Hz} nV/\sqrt{Hz}
i_n	Input Noise Current	0.1Hz to 10Hz		2.2			2.2		pA_{P-P}
	Input Noise Current Density	$f_0 = 10Hz$ $f_0 = 1000Hz$		0.030 0.008			0.030 0.008		pA/\sqrt{Hz} pA/\sqrt{Hz}
V_{CM}	Input Voltage Range		± 13.5	± 14.3		± 13.5	± 14.3		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	120	136		115	136		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.0V$ to $\pm 20V$	116	126		114	126		dB
	Minimum Supply Voltage	(Note 5)	± 1.0			± 1.0			V
R_{IN}	Input Resistance Differential Mode Common Mode	(Note 4)	20	50 800		15	40 700		M Ω G Ω
A_{VOL}	Large-Signal Voltage Gain	$V_0 = \pm 12V$, $R_L = 10k\Omega$ $V_0 = \pm 10V$, $R_L = 2k\Omega$	1000 800	5000 1500		800 600	5000 1300		V/mV V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$ $R_L = 2k\Omega$	± 13.0 ± 11.0	± 14.0 ± 12.4		± 13.0 ± 11.0	± 14.0 ± 12.4		V V
SR	Slew Rate		0.16	0.30		0.16	0.30		V/ μs
GBW	Gain-Bandwidth Product	$f_0 = 10kHz$	450	750		450	750		kHz
I_S	Supply Current per Amplifier	$V_S = \pm 1.0V$		350 320	400 370		350 320	450 420	μA μA
	Channel Separation	$f_0 = 10Hz$		150			150		dB
ΔV_{OS}	Offset Voltage Match	(Note 6)		35	100		40	130	μV
ΔI_B^+	Noninverting Bias Current Match (Notes 6, 7)	LT1114S/LT1114IS		100	450		100 120	500 680	pA pA
$\Delta CMRR$	Common Mode Rejection Match	(Notes 6, 8)	117	136		113	136		dB
$\Delta PSRR$	Power Supply Rejection Match	(Notes 6, 8)	114	130		112	130		dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range of $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$, otherwise specifications are at $T_A = 25^{\circ}\text{C}$. $V_S = \pm 15\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 3)	LT1112AMJ8 LT1114AMJ			LT1112MJ8/MPS8 LT1114MJ			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1112MPS8 $V_S = \pm 1.2\text{V}$	●	35	120	45	150	μV	
			●	60	220	70	260	μV	
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Average Input Offset Voltage Drift	(Note 9) LT1112MPS8	●	0.15	0.5	0.20	0.75	$\mu\text{V}/^{\circ}\text{C}$	
			●			0.4	1.3	$\mu\text{V}/^{\circ}\text{C}$	
I_{OS}	Input Offset Current		●	80	400	100	500	pA	
I_B	Input Bias Current		●	± 150	± 600	± 170	± 700	pA	
V_{CM}	Input Voltage Range		●	± 13.5	± 14.1	± 13.5	± 14.1	V	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5\text{V}$	●	116	130	111	130	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.2\text{V}$ to $\pm 20\text{V}$	●	112	124	110	124	dB	
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 12\text{V}$, $R_L = 10\text{k}\Omega$ $V_O = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$	●	500	2500	400	2500	V/mV	
			●	200	600	170	500	V/mV	
V_{OUT}	Output Voltage Swing	$R_L = 10\text{k}\Omega$	●	± 13.0	± 13.85	± 13.0	± 13.85	V	
SR	Slew Rate		●	0.12	0.22	0.12	0.22	V/ μs	
I_S	Supply Current per Amplifier		●	380	460	380	530	μA	
ΔV_{OS}	Offset Voltage Match (Note 6)	LT1112MPS8	●	55	200	70	240	μV	
			●			70	270	μV	
	Offset Voltage Match Drift (Notes 6, 9)	LT1112MPS8	●	0.2	0.7	0.3	1.0	$\mu\text{V}/^{\circ}\text{C}$	
			●			0.5	1.9	$\mu\text{V}/^{\circ}\text{C}$	
ΔI_B^+	Noninverting Bias Current Match	(Notes 6, 7)	●	150	750	170	850	pA	
ΔCMRR	Common Mode Rejection Ratio	(Notes 6, 8)	●	112	130	106	130	dB	
ΔPSRR	Power Supply Rejection Ratio	(Notes 6, 8)	●	109	126	106	126	dB	

The ● denotes the specifications which apply over the full operating temperature range of $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, otherwise specifications are at $T_A = 25^{\circ}\text{C}$. $V_S = \pm 15\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 3)	LT1112ACN8 LT1114ACN			LT1112CN8/S8/IS8 LT1114CN/S/IS			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1112CN8 LT1112S8, LT1114CN/S $V_S = \pm 1.2\text{V}$	●	27	100	30	125	μV	
			●	35	125	45	150	μV	
			●	50	175	65	210	μV	
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Average Input Offset Voltage Drift (Note 9)	LT1112CN8 LT1112S8, LT1114CN/S	●	0.15	0.5	0.2	0.75	$\mu\text{V}/^{\circ}\text{C}$	
			●	0.3	1.1	0.4	1.3	$\mu\text{V}/^{\circ}\text{C}$	
I_{OS}	Input Offset Current	LT1114S	●	60	220	70	290	pA	
			●			90	420	pA	
I_B	Input Bias Current	LT1114S	●	± 80	± 300	± 90	± 350	pA	
			●			± 115	± 550	pA	
V_{CM}	Input Voltage Range		●	± 13.5	± 14.2	± 13.5	± 14.2	V	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5\text{V}$	●	118	133	113	133	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.2\text{V}$ to $\pm 20\text{V}$	●	114	125	112	125	dB	
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 12\text{V}$, $R_L = 10\text{k}\Omega$ $V_O = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$	●	800	4000	650	4000	V/mV	
			●	500	1300	400	1000	V/mV	
V_{OUT}	Output Voltage Swing	$R_L = 10\text{k}\Omega$	●	± 13.0	± 13.9	± 13.0	± 13.9	V	
SR	Slew Rate		●	0.14	0.27	0.14	0.27	V/ μs	

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range of $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, otherwise specifications are at $T_A = 25^{\circ}\text{C}$. $V_S = \pm 15\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 3)	LT1112ACN8 LT1114ACN			LT1112CN8/S8/IS8 LT1114CN/S/IS			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_S	Supply Current per Amplifier		●	370	440	370	500	μA	
ΔV_{OS}	Offset Voltage Match (Note 6)	LT1112CN8	●	45	170	55	210	μV	
		LT1112S8, LT1114CN/S	●	55	220	70	270	μV	
	Offset Voltage Match Drift (Notes 6, 9)	LT1112N8	●	0.2	0.7	0.3	1.0	$\mu\text{V}/^{\circ}\text{C}$	
		LT1112S8, LT1114CN/S	●	0.4	1.6	0.5	1.9	$\mu\text{V}/^{\circ}\text{C}$	
ΔI_B^+	Noninverting Bias Current Match (Notes 6, 7)	LT1114S	●	120	530	135	620	pA	
ΔCMRR	Common Mode Rejection Ratio	(Notes 6, 8)	●	114	134	109	134	dB	
ΔPSRR	Power Supply Rejection Ratio	(Notes 6, 8)	●	110	128	108	128	dB	

The ● denotes the specifications which apply over the full operating temperature range of $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, otherwise specifications are at $T_A = 25^{\circ}\text{C}$. $V_S = \pm 15\text{V}$, unless otherwise noted. (Note 12)

SYMBOL	PARAMETER	CONDITIONS (Note 3)	LT1112ACN8 LT1114ACN			LT1112CN8/IN8/S8/IS8 LT1114CN/S/IS			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1112CN8/IN8	●	30	110	35	135	μV	
		LT1112S8/IS8, LT1114CN/S/IS	●	40	135	45	160	μV	
		$V_S = \pm 1.2\text{V}$	●	55	200	60	240	μV	
$\frac{\Delta V_{OS}}{\Delta\text{Temp}}$	Average Input Offset Voltage Drift	LT1112CN8/IN8	●	0.15	0.50	0.20	0.75	$\mu\text{V}/^{\circ}\text{C}$	
		LT1112S8/IS8, LT1114CN/S/IS	●	0.30	1.10	0.40	1.30	$\mu\text{V}/^{\circ}\text{C}$	
I_{OS}	Input Offset Current	LT1114S/IS	●	70	330	85	400	pA	
			●			110	600	pA	
I_B	Input Bias Current	LT1114S/IS	●	± 110	± 500	± 120	± 550	pA	
			●			± 150	± 800	pA	
V_{CM}	Input Voltage Range		●	± 13.5	± 14.1	± 13.5	± 14.1	V	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5\text{V}$	●	117	132	112	132	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.2\text{V}$ to $\pm 20\text{V}$	●	113	125	111	125	dB	
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 12\text{V}$, $R_L = 10\text{k}\Omega$	●	700	3300	600	3300	V/mV	
		$V_O = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$	●	400	1100	300	900	V/mV	
V_{OUT}	Output Voltage Swing	$R_L = 10\text{k}\Omega$	●	± 13.0	± 13.85	± 13.0	± 13.85	V	
SR	Slew Rate		●	0.13	0.24	0.13	0.24	$\text{V}/\mu\text{s}$	
I_S	Supply Current per Amplifier		●	370	450	370	510	μA	
ΔV_{OS}	Offset Voltage Match (Note 6)	LT1112CN8/IN8	●	50	180	60	225	μV	
		LT1112S8/IS8, LT1114CN/S/IS	●	60	230	70	270	μV	
	Offset Voltage Match Drift (Notes 6)	LT1112CN8/IN8	●	0.2	0.7	0.3	1.0	$\mu\text{V}/^{\circ}\text{C}$	
		LT1112S8/IS8, LT1114CN/S/IS	●	0.4	1.6	0.5	1.9	$\mu\text{V}/^{\circ}\text{C}$	
ΔI_B^+	Noninverting Bias Current Match (Notes 6, 7)	LT1114S/IS	●	140	660	155	770	pA	
			●			190	1300	pA	
ΔCMRR	Common Mode Rejection Ratio	(Notes 6, 8)	●	113	133	109	133	dB	
ΔPSRR	Power Supply Rejection Ratio	(Notes 6, 8)	●	110	127	107	127	dB	

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

Note 3: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1114s (or 100 LT1112s) typically 240 op amps (or 120) will be better than the indicated specification.

Note 4: This parameter is guaranteed by design and is not tested.

ELECTRICAL CHARACTERISTICS

Note 5: Offset voltage, supply current and power supply rejection ratio are measured at the minimum supply voltage.

Note 6: Matching parameters are the difference between amplifiers A and D and between B and C on the LT1114; between the two amplifiers on the LT1112.

Note 7: This parameter is the difference between two noninverting input bias currents.

Note 8: ΔCMRR and ΔPSRR are defined as follows: (1) CMRR and PSRR are measured in $\mu\text{V}/\text{V}$ on the individual amplifiers. (2) The difference is calculated between the matching sides in $\mu\text{V}/\text{V}$. (3) The result is converted to dB.

Note 9: This parameter is not 100% tested.

Note 10: These parameters are not tested. More than 99% of the op amps tested during product characterization have passed the maximum limits. 100% passed at 1kHz.

Note 11: The LT1112AC/LT1112C/LT1112S8/LT1112I and LT1114AC/LT1114C/LT1114S/LT1114I are guaranteed functional over the temperature range of -40°C to 85°C .

Note 12: The LT1112AC/LT1112C/LT1112S8/LT1114AC/LT1114C/LT1114S are guaranteed to meet specified performance from 0°C to 70°C and are designed, characterized and expected to meet specified performance from -40°C to 85°C , but are not tested or QA sampled at these temperatures. The LT1112I/LT1114I are guaranteed to meet specified performance from -40°C to 85°C .

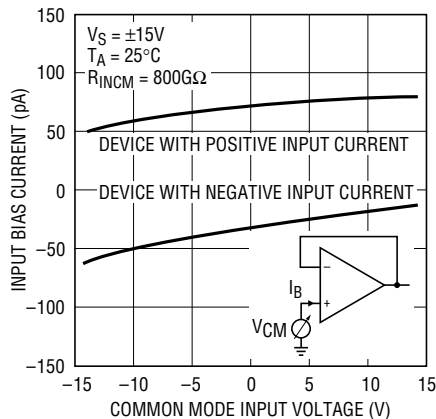
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias and Offset Current, Noninverting Bias Current Match vs Temperature



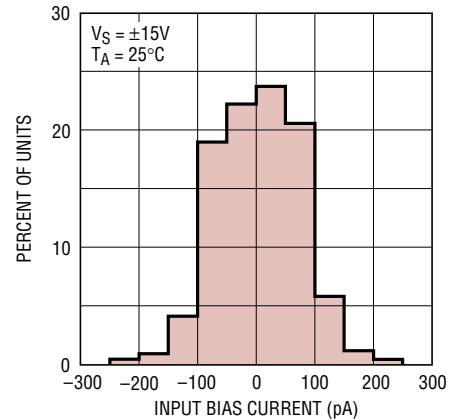
LT1112/14 • TPC01

Input Bias Current Over Common Mode Range



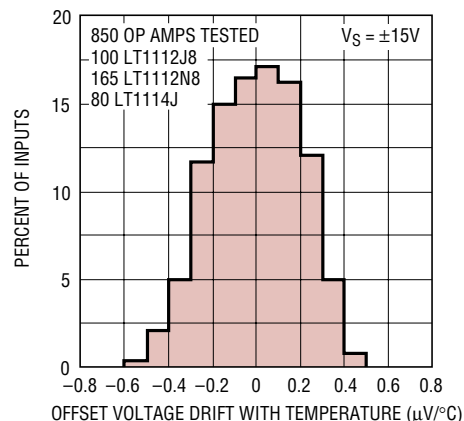
LT1112/14 • TPC02

Distribution of Input Bias Current (In All Packages Except LT1114S)



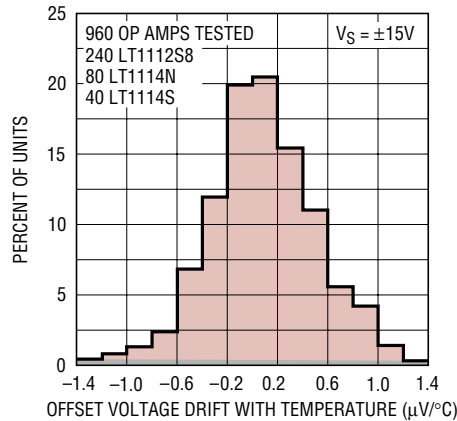
LT1112/14 • TPC03

Drift with Temperature LT1112N8/J8, LT1114J



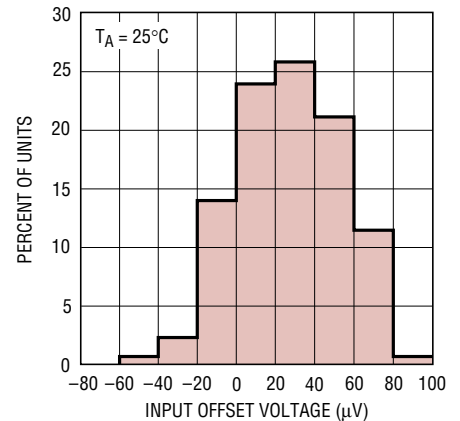
LT1112/14 • TPC04

Drift with Temperature LT1112S8, LT1114N/S



LT1112/14 • TPC05

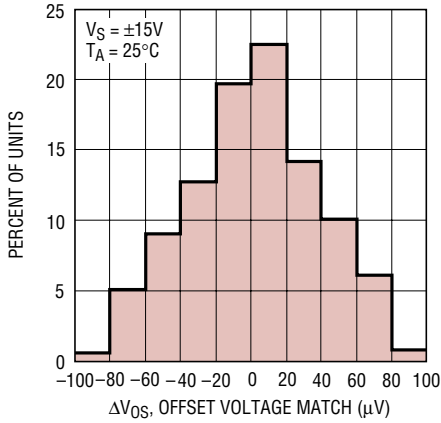
Distribution of Offset Voltage at VS = ±1.0V (In All Packages)



LT1112/14 • TPC06

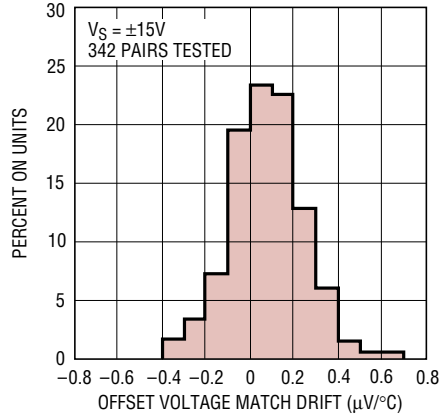
TYPICAL PERFORMANCE CHARACTERISTICS

Distribution of Offset Voltage Match



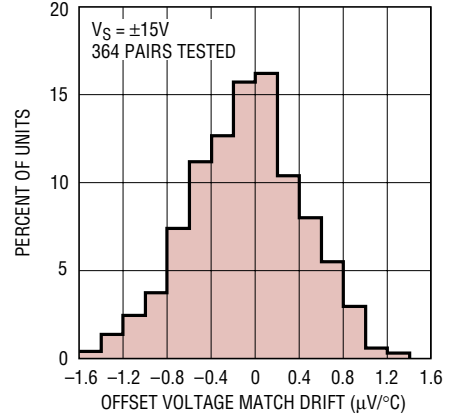
LT1112/14 • TPC07

Distribution of Offset Voltage Match Drift (LT1112J8, LT1112N8, LT1114J Packages)



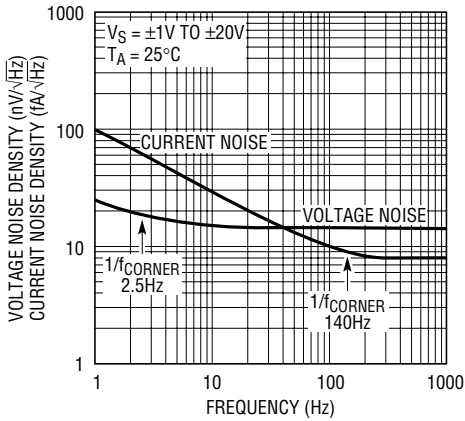
LT1112/14 • TPC08

Distribution of Offset Voltage Match Drift (LT1112S8, LT1114N, LT1114S Packages)



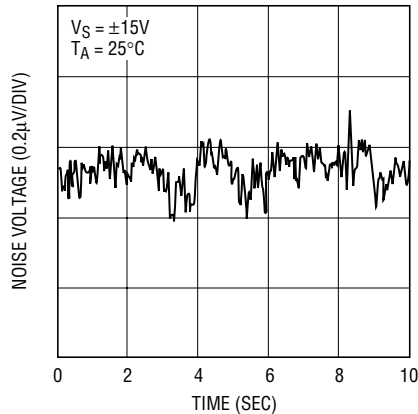
LT1112/14 • TPC09

Noise Spectrum



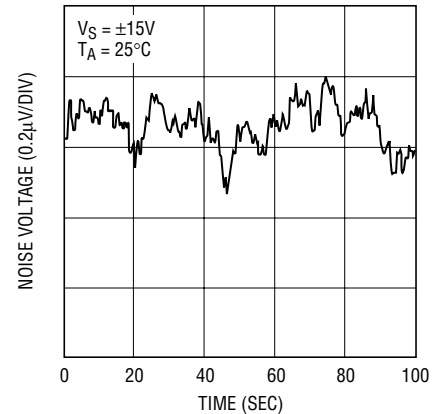
LT1112/14 • TPC10

0.1Hz to 10Hz Noise



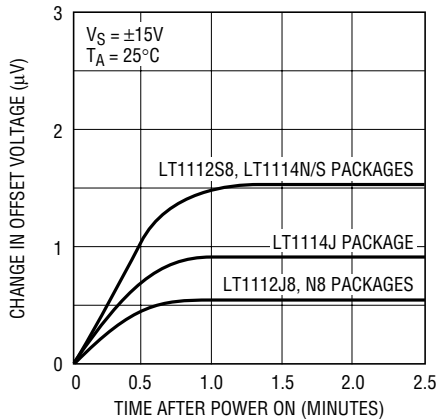
LT1112/14 • TPC11

0.01Hz to 1Hz Noise



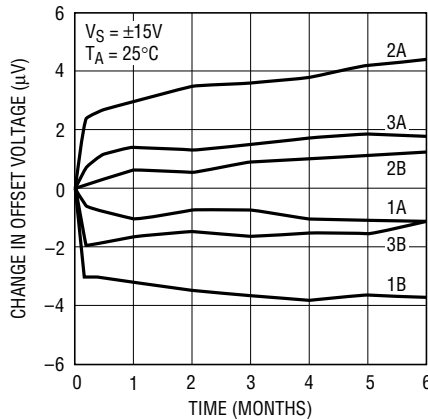
LT1112/14 • TPC12

Warm-Up Drift



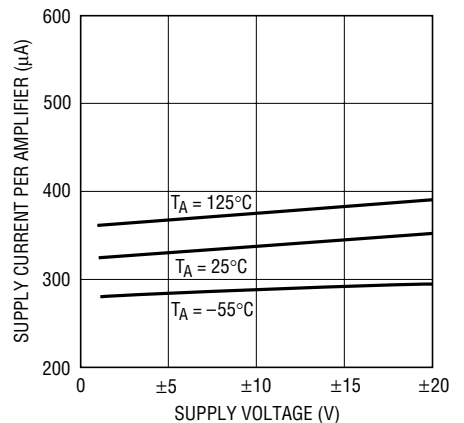
LT1112/14 • TPC13

Long Term Stability of Three Representative Units



LT1112/14 • TPC14

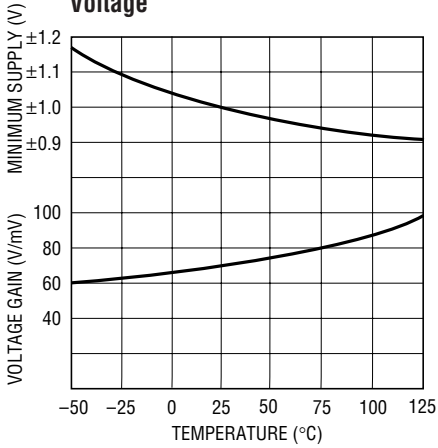
Supply Current per Amplifier vs Supply Voltage



LT1112/14 • TPC15

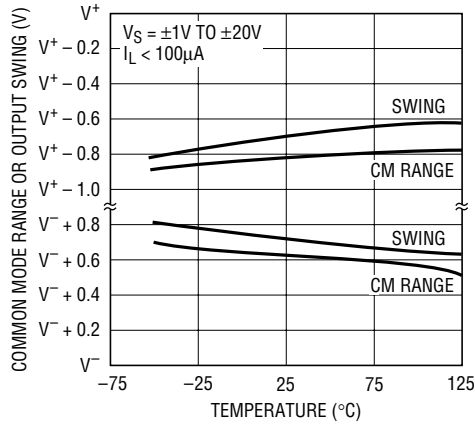
TYPICAL PERFORMANCE CHARACTERISTICS

**Minimum Supply Voltage vs Temp
Voltage Gain at Minimum Supply Voltage**



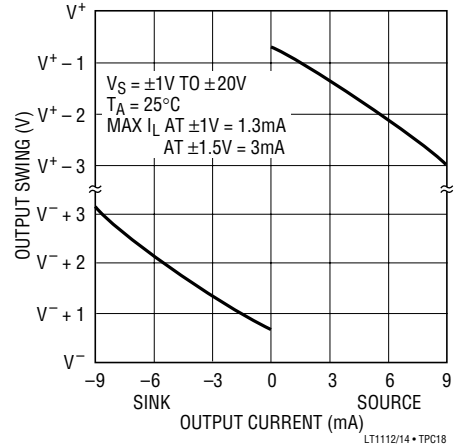
LT1112/14 • TPC16

**Common Mode Range and
Voltage Swing with Respect to
Supply Voltages**



LT1112/14 • TPC17

**Output Voltage Swing
vs Load Current**



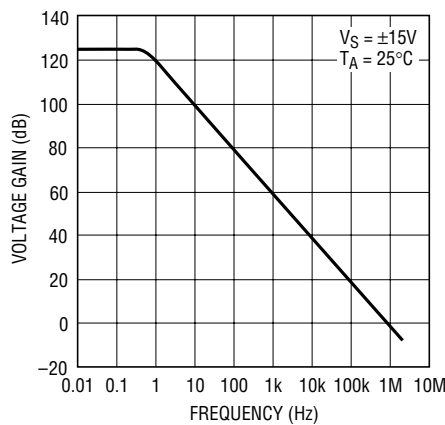
LT1112/14 • TPC18

Voltage Gain



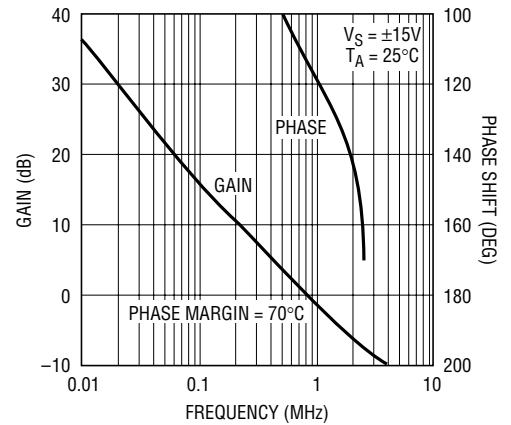
LT1112/14 • TPC19

Voltage Gain vs Frequency



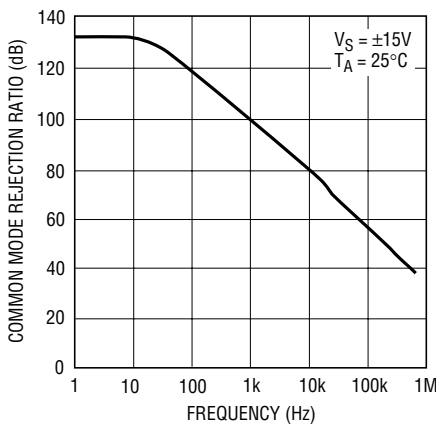
LT1112/14 • TPC20

Gain, Phase Shift vs Frequency



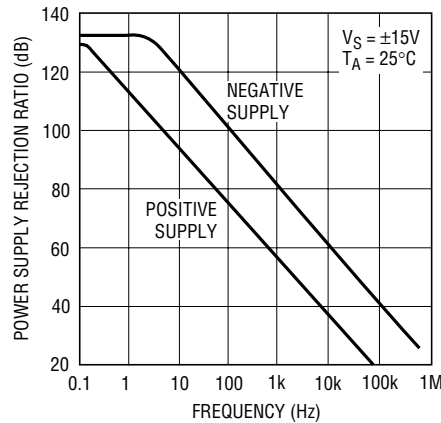
LT1112/14 • TPC21

**Common Mode Rejection
vs Frequency**



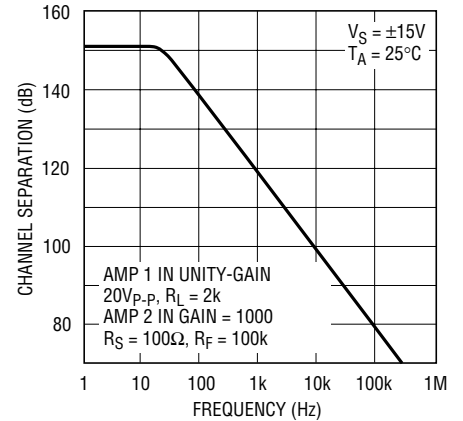
LT1112/14 • TPC22

**Power Supply Rejection
vs Frequency**



LT1112/14 • TPC23

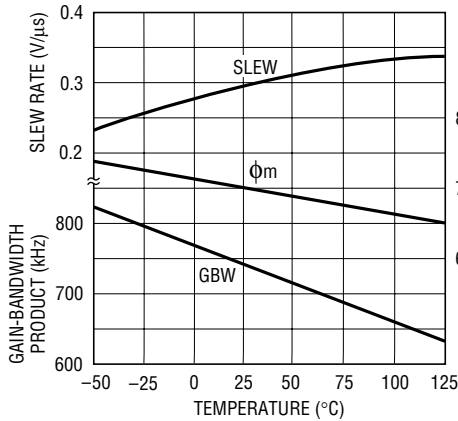
Channel Separation vs Frequency



LT1112/14 • TPC24

TYPICAL PERFORMANCE CHARACTERISTICS

Slew Rate, Gain-Bandwidth Product and Phase Margin vs Temperature



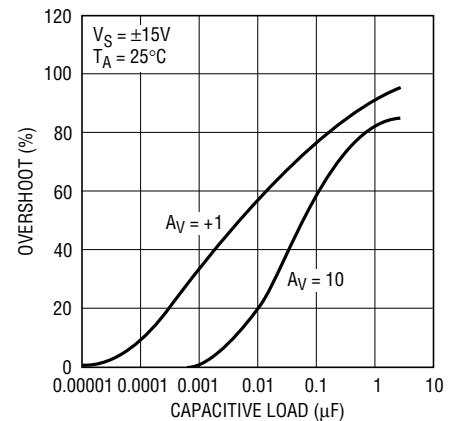
LT1112/14 • TPC25

Closed-Loop Output Impedance



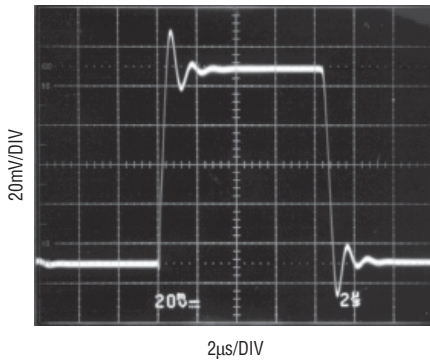
LT1112/14 • TPC26

Capacitive Loading Handling



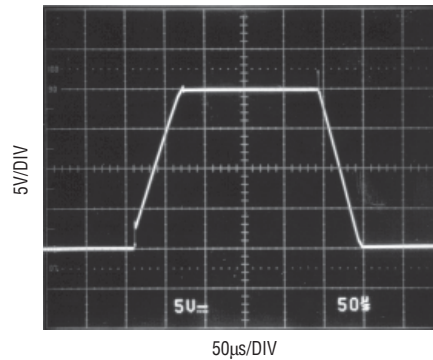
LT1112/14 • TPC27

Small-Signal Transient Response



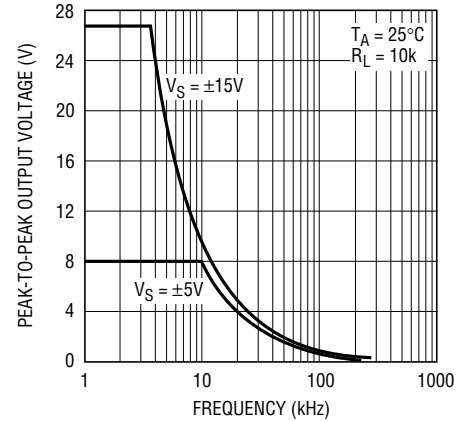
$A_V = +1$
 $C_L = 500\text{pF}$
 $V_S = \pm 15\text{V}$

Large-Signal Transient Response



$A_V = +1$
 $R_F = 10\text{k}$
 $C_F = 100\text{pF}$
 $V_S = \pm 15\text{V}$

Undistorted Output Voltage vs Frequency



LT1112/14 • TPC30

APPLICATIONS INFORMATION

The LT1112 dual and LT1114 quad in the plastic and ceramic DIP packages are pin compatible to and directly replace such precision op amps as the OP-200, OP-297, AD706 duals and OP-400, OP-497, AD704 quads with improved price/performance.

The LT1112 in the S8 surface mount package has the standard pin configuration, i.e., the same configuration as the plastic and ceramic DIP packages.

The LT1114 quad is offered in the narrow 16-pin surface mount package. All competitors are in the wide 16-pin package which occupies 1.8 times the area of the narrow package. The wide package is also 1.8 times thicker than the narrow package.

The inputs of the LT1112/1114 are protected with back-to-back diodes. In the voltage follower configuration, when the input is driven by a fast large-signal pulse (>1V), the input protection diodes effectively short the output to the input during slewing, and a current, limited only by the output short-circuit protection, will flow through the diodes.

The use of a feedback resistor is recommended because this resistor keeps the current below the short-circuit limit, resulting in faster recovery and settling of the output.

The input voltage of the LT1112/1114 should never exceed the supply voltages by more than a diode drop. However, the example below shows that as the input voltage exceeds the common mode range, the LT1112's

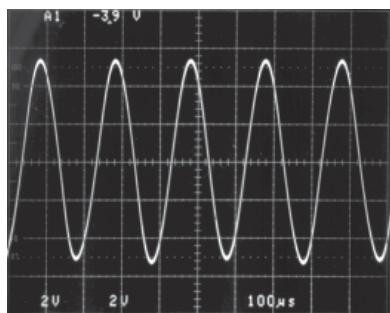
output clips cleanly, without any glitches or phase reversal. The OP-297 exhibits phase reversal. The photos also illustrate that both the input and output ranges of the LT1112 are within 800mV of the supplies. The effect of input and output overdrive on the other amplifiers in the LT1112 or LT1114 packages is negligible, as each amplifier is biased independently.

Advantages of Matched Dual and Quad Op Amps

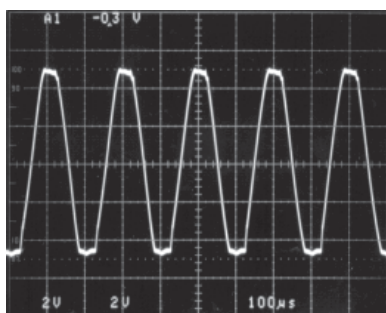
In many applications the performance of a system depends on the matching between two operational amplifiers rather than the individual characteristics of the two op amps. Two or three op amp instrumentation amplifiers, tracking voltage references and low drift active filters are some of the circuits requiring matching between two op amps.

The well-known triple op amp configuration illustrates these concepts. Output offset is a function of the difference between the offsets of the two halves of the LT1112. This error cancellation principle holds for a considerable number of input referred parameters in addition to offset voltage and its drift with temperature. Input bias current will be the average of the two noninverting input currents (I_B^+). The difference between these two currents (ΔI_B^+) is the offset current of the instrumentation amplifier. Common mode and power supply rejections will be dependent only on the match between the two amplifiers (assuming perfect resistor matching).

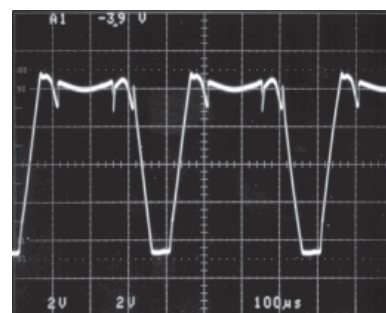
Voltage Follower with Input Exceeding the Common Mode Range ($V_S = \pm 5V$)



INPUT: $\pm 5.2V$ Sine Wave



LT1112 Output



OP-297 Output

APPLICATIONS INFORMATION

Three Op Amp Instrumentation Amplifier



The concepts of common mode and power supply rejection ratio match (ΔCMRR and ΔPSRR) are best demonstrated with a numerical example:

Assume $\text{CMRR}_A = +1\mu\text{V}/\text{V}$ or 120dB,
 and $\text{CMRR}_B = +0.75\mu\text{V}/\text{V}$ or 122.5dB,
 then $\Delta\text{CMRR} = 0.25\mu\text{V}/\text{V}$ or 132dB;
 if $\text{CMRR}_B = -0.75\mu\text{V}/\text{V}$ which is still 122.5dB,
 then $\Delta\text{CMRR} = 1.75\mu\text{V}/\text{V}$ or 115dB.

Clearly the LT1112/LT1114, by specifying and guaranteeing all of these matching parameters, can significantly improve the performance of matching-dependent circuits.

Typical performance of the instrumentation amplifier:

Input offset voltage = $35\mu\text{V}$
 Offset voltage drift = $0.3\mu\text{V}/^\circ\text{C}$
 Input bias current = 80pA
 Input offset current = 100pA
 Input resistance = $800\text{G}\Omega$
 Input noise = $0.42\mu\text{V}_{\text{P-P}}$

When the instrumentation amplifier is used with high impedance sources, the LT1114 is recommended because its CMRR vs frequency performance is better than the LT1112's. For example, with two matched $1\text{M}\Omega$ source resistors, CMRR at 100Hz is 100dB with the LT1114, 76dB with the LT1112.

This difference is explained by the fact that capacitance between adjacent pins on an IC package is about 0.25pF (including package, socket and PC board trace capacitances).

On the dual op amp package, positive input A is next to the V^- pin (AC ground), while positive input B has no AC ground pin adjacent to it, resulting in a 0.25pF input capacitance mismatch. At 100Hz, 0.25pF represents a $6.4 \cdot 10^9$ input impedance mismatch, which is only 76dB higher than the $1\text{M}\Omega$ source resistors.

On the quad package, all four inputs are adjacent to a power supply terminal—therefore, there is no mismatch.

SCHEMATIC DIAGRAM (1/2 LT1112, 1/4 LT1114)



Q1 TO Q4 ARE SUPERGAIN TRANSISTORS

LT1112/14 • SD01

PACKAGE DESCRIPTION

J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
 (Reference LTC DWG # 05-08-1110)



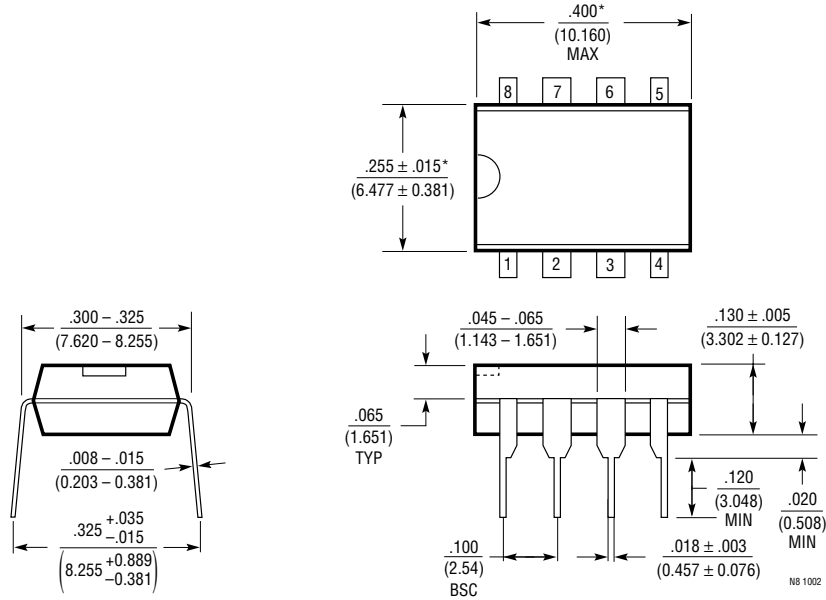
J Package
14-Lead CERDIP (Narrow .300 Inch, Hermetic)
 (Reference LTC DWG # 05-08-1110)



OBSOLETE PACKAGES

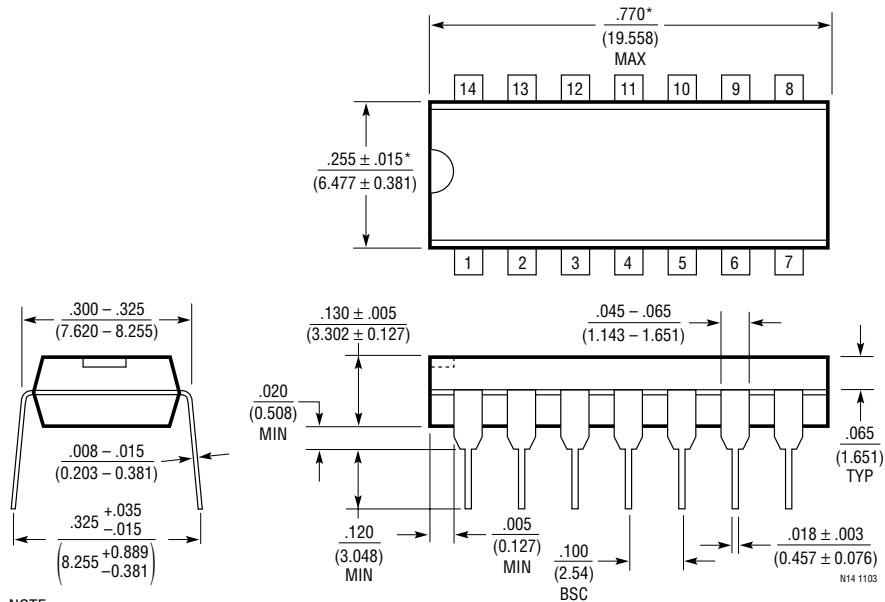
PACKAGE DESCRIPTION

N8 Package
8-Lead PDIP (Narrow .300 Inch)
 (Reference LTC DWG # 05-08-1510)



NOTE:
 1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
 *THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

N Package
14-Lead PDIP (Narrow .300 Inch)
 (Reference LTC DWG # 05-08-1510)



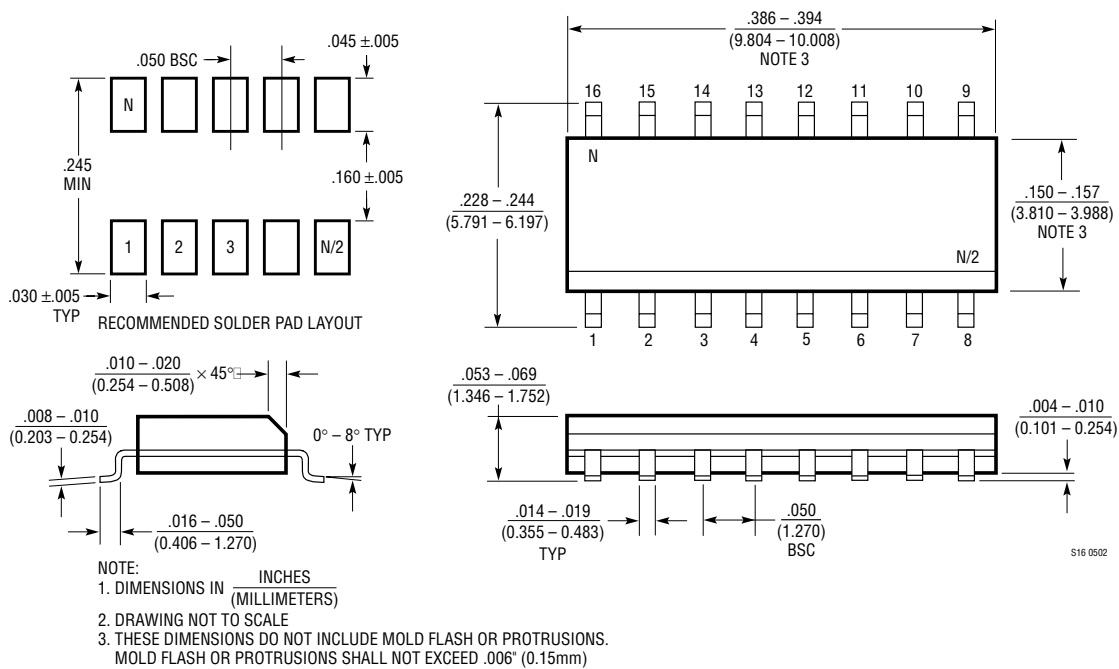
NOTE:
 1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
 *THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)

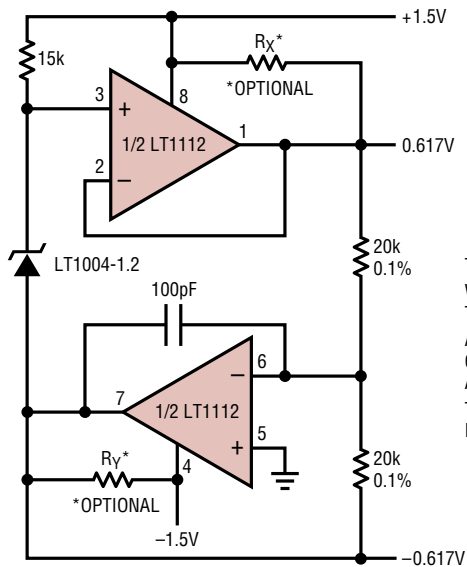


S Package 16-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



TYPICAL APPLICATION

Dual Buffered $\pm 0.617V$ Reference Powered by Two AA Batteries



TOTAL SUPPLY CURRENT = $700\mu A$
 WORKS WITH BATTERIES DISCHARGED TO $\pm 1.3V$
 AT $\pm 1.5V$: MAXIMUM LOAD CURRENT = $800\mu A$;
 CAN BE INCREASED WITH OPTIONAL R_X, R_Y ;
 AT $R_X = R_Y = 750\Omega$ LOAD CURRENT = $2mA$
 TEMPERATURE COEFFICIENT LIMITED BY REFERENCE = $20ppm/^{\circ}C$

LT1112/14 • TA03

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1880	Rail-to-Rail Output, Picoamp Input Precision Op Amp	SOT-23
LT1881/LT1882	Dual/Quad Rail-to-Rail Output, Picoamp Input Precision Op Amp	C_{LOAD} Up to $1000pF$
LT1884/LT1885	Dual/Quad Rail-to-Rail Output, Picoamp Input Precision Op Amp	$9.5nV/\sqrt{Hz}$ Input Noise
LT6011/LT6012	Dual/Quad Rail-to-Rail Output, Picoamp Input Precision Op Amp	$135\mu A$ Supply Current, $14nV/\sqrt{Hz}$