# **Small Signal MOSFET**

-20 V, -760 mA, Single P-Channel, Gate Zener, SC-75, SC-89

#### **Features**

- Low R<sub>DS(on)</sub> for Higher Efficiency and Longer Battery Life
- Small Outline Package (1.6 x 1.6 mm)
- SC-75 Standard Gullwing Package
- ESD Protected Gate
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### **Applications**

- High Side Load Switch
- DC-DC Conversion
- Small Drive Circuits
- Battery Operated Systems such as Cell Phones, PDAs, Digital Cameras, etc.

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise stated)

Parameter	Symbol	Value	Units	
Drain-to-Source Voltage	V <sub>DSS</sub>	-20	V	
Gate-to-Source Voltage		V <sub>GS</sub>	±6.0	V
Continuous Drain Current (Note 1) Steady State		I <sub>D</sub>	-760	mA
Power Dissipation (Note 1) SC-75 SC-89 Steady State		P <sub>D</sub>	301 313	mW
Pulsed Drain Current	I <sub>DM</sub>	±1000	mA	
Operating Junction and Storage	T <sub>J</sub> , T <sub>STG</sub>	–55 to 150	°C	
Continuous Source Current (Bo	I <sub>S</sub>	-250	mA	
Lead Temperature for Soldering (1/8 in from case for 10 s)	TL	260	°C	
Gate-to-Source ESD Rating - (Human Body Model	ESD	1800	V	

#### THERMAL RESISTANCE RATINGS

$R_{\theta JA}$		°C/W
	415	
	400	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

 Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

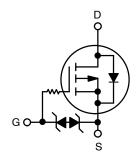


### ON Semiconductor®

#### http://onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> MAX	
-20 V	0.26 Ω @ -4.5 V		
	0.35 Ω @ -2.5 V	-760 mA	
	0.49 Ω @ -1.8 V		

#### P-Channel MOSFET

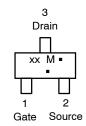


# MARKING DIAGRAM & PIN ASSIGNMENT





SC-89 CASE 463C



xx = Device Code

M = Date Code\*

= Pb-Free Package

(Note: Microdot may be in either location)
\*Date Code orientation may vary depending

\*Date Code orientation may vary depending upon manufacturing location.

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

## **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise stated)

Parameter Symbol Test Condition		Test Condition	Min	Тур	Max	Unit
OFF CHARACTERISTICS			•	•		
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V, } I_D = -250  \mu\text{A}$ -20				V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 \text{ V}, V_{DS} = -16 \text{ V}$		-1.0	-100	nA
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$		±1.0	±10	μΑ
ON CHARACTERISTICS (Note 2)			•	•		
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-0.45			V
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	$V_{GS} = -4.5 \text{ V}, I_D = -350 \text{ mA}$ 0.2		0.26	0.36	Ω
		$V_{GS} = -2.5 \text{ V}, I_D = -300 \text{ mA}$		0.35	0.45	1
		$V_{GS} = -1.8 \text{ V}, I_D = -150 \text{ mA}$		0.49	1.0	
Forward Transconductance	9FS	$V_{DS} = -10 \text{ V}, I_D = -250 \text{ mA}$	$V_{DS} = -10 \text{ V}, I_D = -250 \text{ mA}$ 0.			S
CHARGES AND CAPACITANCES			•	1		
Input Capacitance	C <sub>ISS</sub>	$V_{GS} = 0 \text{ V, f} = 1.0 \text{ MHz,}$		156		pF
Output Capacitance	C <sub>OSS</sub>	V <sub>DS</sub> = -5.0 V		28		
Reverse Transfer Capacitance	C <sub>RSS</sub>			18		
Total Gate Charge	Q <sub>G(TOT)</sub>	$V_{GS} = -4.5 \text{ V}, V_{DD} = -10 \text{ V},$		2.1		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>	I <sub>D</sub> = -0.3 A		0.125		1
Gate-to-Source Charge	Q <sub>GS</sub>			0.325		
Gate-to-Drain Charge	$Q_{GD}$			0.5		
SWITCHING CHARACTERISTICS (Note	3)		•	•		
Turn-On Delay Time	td <sub>(ON)</sub>	$V_{GS} = -4.5 \text{ V}, V_{DD} = -10 \text{ V},$		8.0		ns
Rise Time	t <sub>r</sub>	$I_D$ = -200 mA, $R_G$ = 10 $\Omega$		8.2		]
Turn-Off Delay Time	td <sub>(OFF)</sub>			29		
Fall Time	t <sub>f</sub>			20.4		
DRAIN-SOURCE DIODE CHARACTER	ISTICS	1				
Forward Diode Voltage	$V_{SD}$	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -250 mA		-0.72	-1.1	V

#### **ORDERING INFORMATION**

Device	Marking	Package	Shipping <sup>†</sup>
NTA4151PT1G	TN	SC-75 (Pb-Free)	3000 / Tape & Reel
NTA4151PT1H	TN	SC-75 (Pb-Free)	3000 / Tape & Reel
NTE4151PT1G	ТМ	SC-89 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

#### TYPICAL ELECTRICAL CHARACTERISTICS

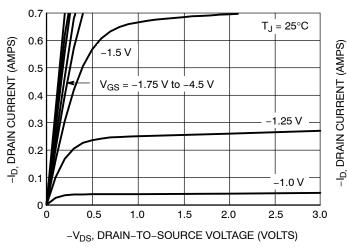
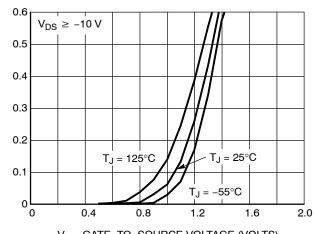


Figure 1. On-Region Characteristics



-V<sub>GS</sub>, GATE-TO-SOURCE VOLTAGE (VOLTS)

Figure 2. Transfer Characteristics

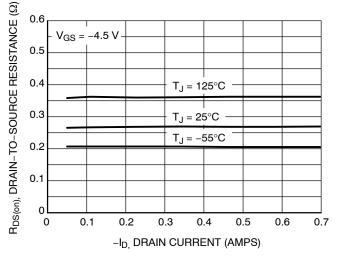


Figure 3. On–Resistance vs. Drain Current and Temperature

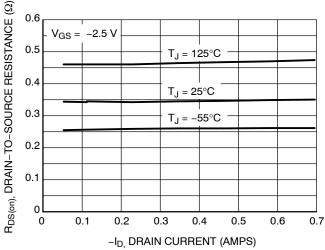


Figure 4. On-Resistance vs. Drain Current and Temperature

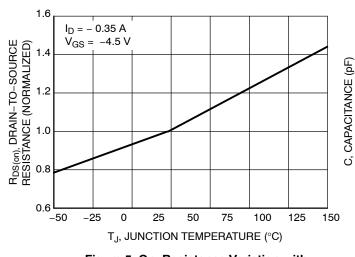


Figure 5. On–Resistance Variation with Temperature

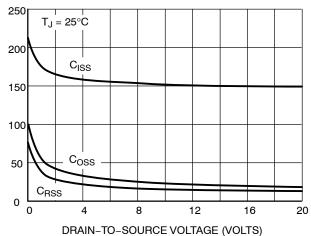
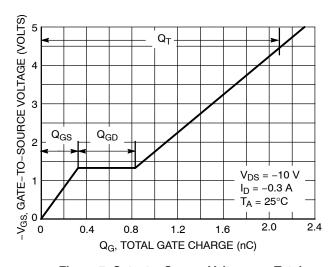


Figure 6. Capacitance Variation

#### TYPICAL ELECTRICAL CHARACTERISTICS



0.7  $V_{GS} = 0 V$ -I<sub>S</sub>, SOURCE CURRENT (AMPS) 0.6 0.5 0.4 0.3  $T_J = 125^{\circ}C$ 0.2 0.1 = 25°C 0 L 0.6 1.0 0.4 -V<sub>SD</sub>, SOURCE-TO-DRAIN VOLTAGE (VOLTS)

Figure 7. Gate-to-Source Voltage vs. Total Gate Charge

Figure 8. Diode Forward Voltage vs. Current

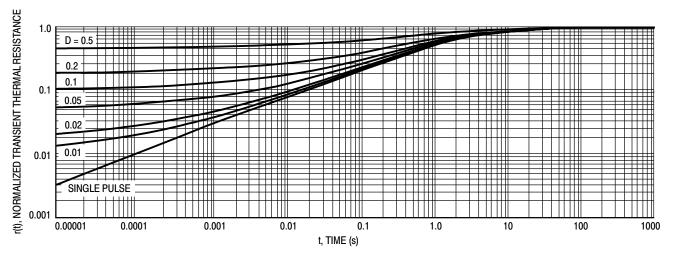
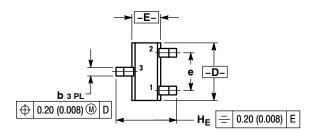
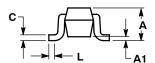


Figure 9. Normalized Thermal Response

## PACKAGE DIMENSIONS

#### SC-75/SOT-416 CASE 463 **ISSUE F**





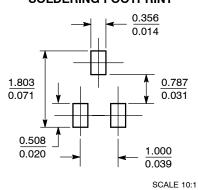
- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	0.70	0.80	0.90	0.027	0.031	0.035
A1	0.00	0.05	0.10	0.000	0.002	0.004
b	0.15	0.20	0.30	0.006	0.008	0.012
С	0.10	0.15	0.25	0.004	0.006	0.010
D	1.55	1.60	1.65	0.059	0.063	0.067
E	0.70	0.80	0.90	0.027	0.031	0.035
е	1.00 BSC			C	.04 BS0	
L	0.10	0.15	0.20	0.004	0.006	0.008
He	1 50	1.60	1 70	0.061	0.063	0.065

STYLE 5: PIN 1. GATE 2. SOURCE 3. DRAIN

 $\left(\frac{\text{mm}}{\text{inches}}\right)$ 

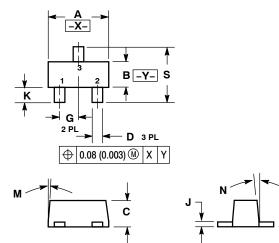
#### **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### PACKAGE DIMENSIONS

SC-89, 3-LEAD CASE 463C-03 ISSUE C

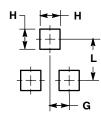


- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETERS
  MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
- 463C-01 OBSOLETE, NEW STANDARD 463C-02.

	MIL	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α	1.50	1.60	1.70	0.059	0.063	0.067	
В	0.75	0.85	0.95	0.030	0.034	0.040	
С	0.60	0.70	0.80	0.024	0.028	0.031	
D	0.23	0.28	0.33	0.009 0.011 0.01		0.013	
G	0.50 BSC			0.020 BSC			
Н	0.53 REF			0.021 REF			
J	0.10	0.15	0.20	0.004 0.006 0.0		0.008	
K	0.30	0.40	0.50	0.012	0.016	0.020	
L	1.10 REF 0.0			.043 RE	F		
М			10			10	
N			10 -			10 -	
S	1.50	1.60	1.70	0.059	0.063	0.067	

#### SOLDERING FOOTPRINT\*

SEATING PLANE



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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