

1.2V Drive Nch MOSFET

RUM002N05

● **Structure**

Silicon N-channel MOSFET SOT-72
3

● **Features**

- 1) High speed switing.
- 2) Small package(VMT3).
- 3) Ultra low voltage drive(1.2V drive).

● **Application**

Switching

● **Packaging specifications**

Type	Package	Taping
	Code	T2L
	Basic ordering unit (pieces)	8000
RUM002N05		○

● **Absolute maximum ratings (Ta = 25°C)**

Parameter	Symbol	Limits	Unit	
Drain-source voltage	V_{DSS}	50	V	
Gate-source voltage	V_{GSS}	±8	V	
Drain current	Continuous	I_D	±200	mA
	Pulsed	I_{DP} *1	±800	mA
Source current (Body Diode)	Continuous	I_S	125	mA
	Pulsed	I_{SP} *1	800	mA
Power dissipation	P_D *2	150	mW	
Channel temperature	T_{ch}	150	°C	
Range of storage temperature	T_{stg}	-55 to +150	°C	

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

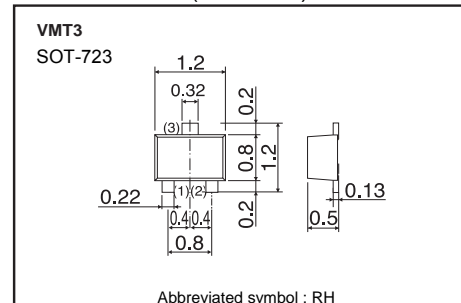
*2 Each terminal mounted on a recommended land.

● **Thermal resistance**

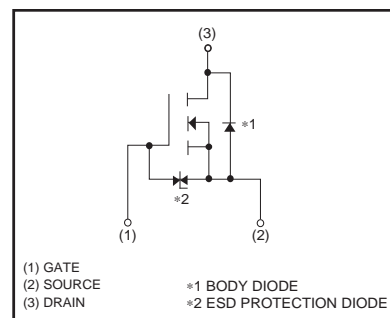
Parameter	Symbol	Limits	Unit
Channel to Ambient	$R_{th}(ch-a)^*$	833	°C / W

* Each terminal mounted on a recommended land.

● **Dimensions (Unit : mm)**



● **Inner circuit**



●Electrical characteristics (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	± 10	μA	$V_{GS}=\pm 8V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	50	-	-	V	$I_D=1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=50V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	0.3	-	1.0	V	$V_{DS}=10V, I_D=1mA$
Static drain-source on-state resistance	$R_{DS(on)}^*$	-	1.6	2.2	Ω	$I_D=200mA, V_{GS}=4.5V$
		-	1.7	2.4		$I_D=200mA, V_{GS}=2.5V$
		-	1.9	2.7		$I_D=100mA, V_{GS}=1.8V$
		-	2.0	4.0		$I_D=40mA, V_{GS}=1.5V$
		-	2.4	7.2		$I_D=20mA, V_{GS}=1.2V$
Forward transfer admittance	$ Y_{fs} ^*$	0.4	-	-	S	$I_D=200mA, V_{DS}=10V$
Input capacitance	C_{iss}	-	25	-	pF	$V_{DS}=10V$
Output capacitance	C_{oss}	-	6	-	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	-	3	-	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}^*$	-	4	-	ns	$I_D=100mA, V_{DD}=30V$
Rise time	t_r^*	-	6	-	ns	$V_{GS}=4.5V$
Turn-off delay time	$t_{d(off)}^*$	-	15	-	ns	$R_L=300\Omega$
Fall time	t_f^*	-	55	-	ns	$R_G=10\Omega$

*Pulsed

●Body diode characteristics (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD}^*	-	-	1.2	V	$I_s=200mA, V_{GS}=0V$

*Pulsed

●Electrical characteristic curves

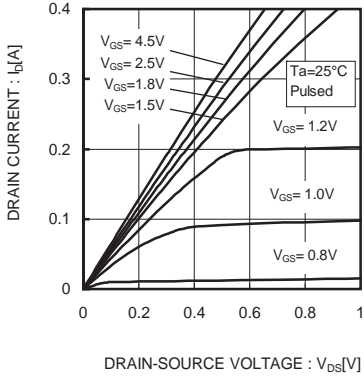


Fig.1 Typical Output Characteristics(I)

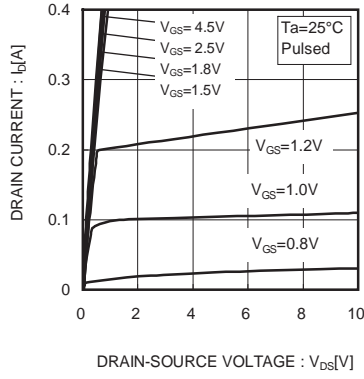


Fig.2 Typical Output Characteristics(II)

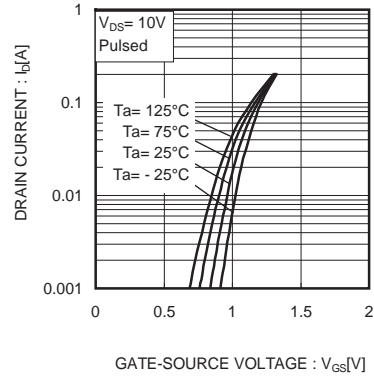


Fig.3 Typical Transfer Characteristics

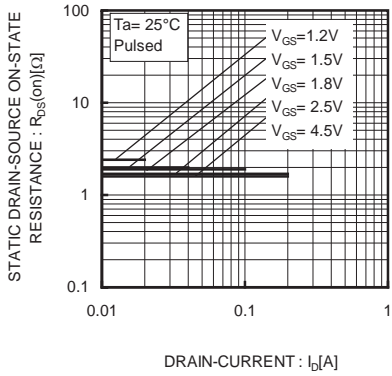


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

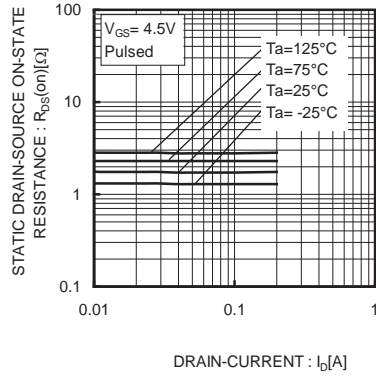


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

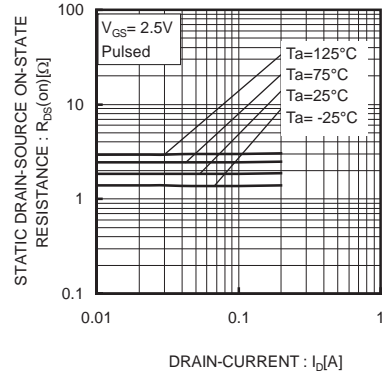


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

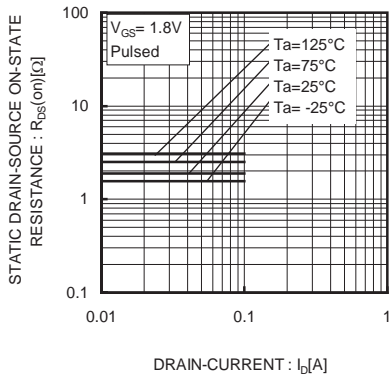


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

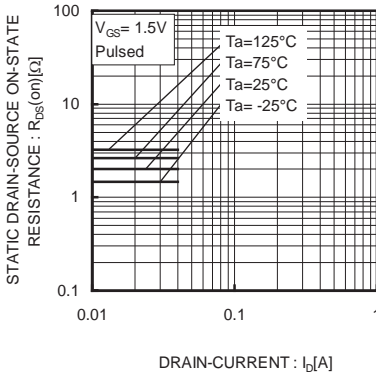


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(V)

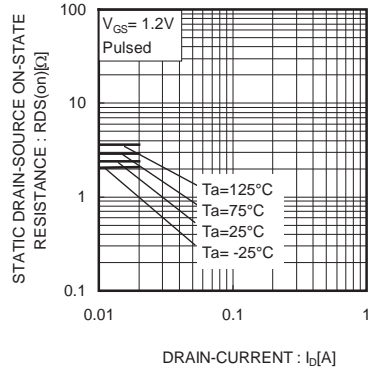


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current(VI)

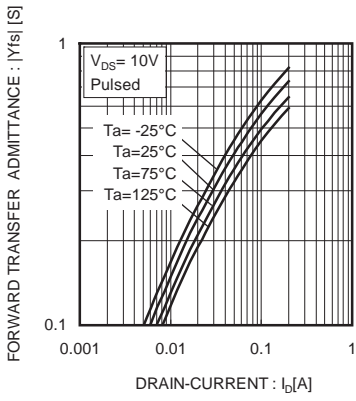


Fig.10 Forward Transfer Admittance vs. Drain Current

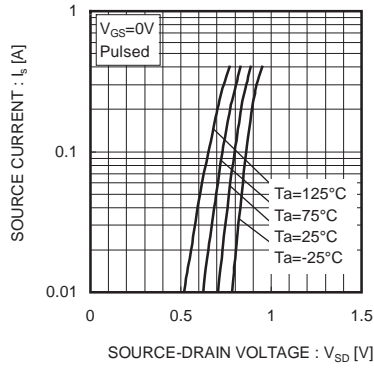


Fig.11 Reverse Drain Current vs. Source-Drain Voltage

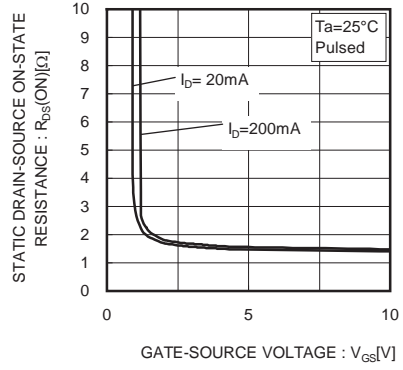


Fig.12 Static Drain-Source On-State Resistance vs. Gate Source Voltage

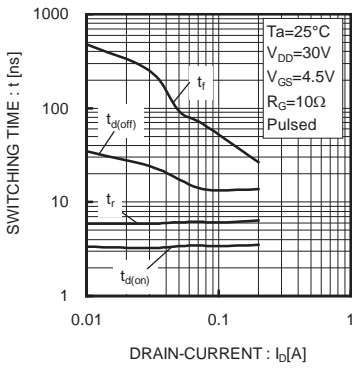


Fig.13 Switching Characteristics

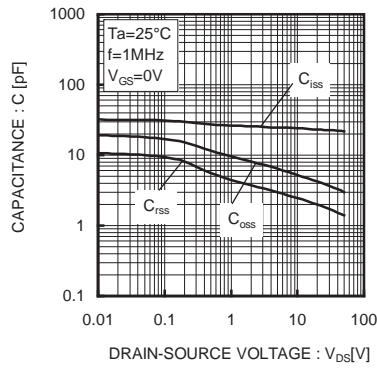


Fig.14 Typical Capacitance vs. Drain-Source Voltage

●Measurement circuits

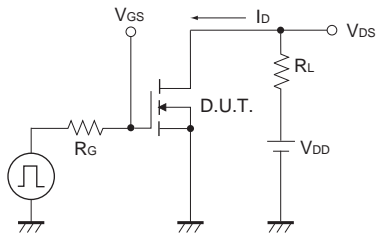


Fig.1-1 Switching time measurement circuit

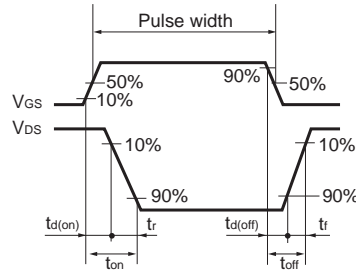


Fig.1-2 Switching waveforms

●Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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