Unit: mm

TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type

# SSM3J117TU

#### **High-Speed Switching Applications**

• 4 V drive

• Low ON-resistance:  $R_{on}$  = 225 m $\Omega$  (max) (@V<sub>GS</sub> = -4 V)  $R_{on}$  = 117 m $\Omega$  (max) (@V<sub>GS</sub> = -10 V)

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#### Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit	
Drain-source voltage		V <sub>DS</sub>	-30	V	
Gate-source voltage		V <sub>GSS</sub>	± 20	V	
Drain current	DC	I <sub>D</sub>	-2	А	
	Pulse	I <sub>DP</sub>	-4		
Drain power dissipation		P <sub>D (Note 1)</sub>	800	mW	
		P <sub>D (Note 2)</sub>	500		
Channel temperature		T <sub>ch</sub>	150	°C	
Storage temperature range		T <sub>stg</sub>	–55 to 150	°C	

Note:

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on a ceramic board.

 $(25.4 \text{ mm} \times 25.4 \text{ mm} \times 0.8 \text{ t}, \text{ Cu Pad: } 645 \text{ mm}^2)$ 

Note 2: Mounted on an FR4 board.

 $(25.4 \text{ mm} \times 25.4 \text{ mm} \times 1.6 \text{ t}, \text{ Cu Pad: } 645 \text{ mm}^2)$ 

## 2.0±0.1 1.2±0.05 0.65±0.05 1.0±0.05 0.166±0.05 0.3±0.11

2.1±0.1

1: Gate 2: Source

3: Drain

UFM

JEDEC —

TOSHIBA 2-2U1A

Weight: 6.6 mg (typ.)

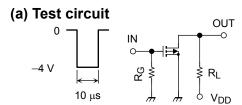
**JEITA** 

#### **Electrical Characteristics (Ta = 25°C)**

Characte	eristic	Symbol	Test Condition	Min	Тур.	Max	Unit
Drain–source breakdown voltage		V (BR) DSS	$I_D = -1 \text{ mA}, V_{GS} = 0$	-30	_	_	V
		V (BR) DSX	$I_D = -1 \text{ mA}, V_{GS} = +20 \text{ V}$	-15	_	_	
Drain cutoff current		I <sub>DSS</sub>	$V_{DS} = -30 \text{ V}, V_{GS} = 0$	_	_	-1	μА
Gate leakage curre	nt	I <sub>GSS</sub>	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$	_	_	±1	μА
Gate threshold volta	age	V <sub>th</sub>	$V_{DS} = -5 \text{ V}, I_D = -1 \text{ mA}$	-1.2	_	-2.6	V
Forward transfer ad	Imittance	Y <sub>fs</sub>	$V_{DS} = -5 \text{ V}, I_D = -1 \text{ A}$ (Note 3)	1.6	3.1	_	S
Drain-source ON-resistance		R <sub>DS</sub> (ON)	$I_D = -1 \text{ A}, V_{GS} = -10 \text{ V}$ (Note 3)	_	80	117	mΩ
			$I_D = -0.5 \text{ A}, V_{GS} = -4 \text{ V}$ (Note 3)	_	160	225	
Input capacitance		C <sub>iss</sub>	$V_{DS} = -15 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	_	280	_	pF
Output capacitance		Coss	$V_{DS} = -15 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	_	80	_	pF
Reverse transfer ca	ansfer capacitance $C_{rss}$ $V_{DS} = -15 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		_	45	_	pF	
Switching time	Turn-on time	t <sub>on</sub>	$V_{DD} = -15 \text{ V}, I_D = -1 \text{ A},$	_	16	_	ns
	Turn-off time	t <sub>off</sub>	$V_{GS} = 0$ to $-4$ V, $R_G = 10 \Omega$	_	35	_	
Drain-source forwa	rd voltage	V <sub>DSF</sub>	$I_D = 2 \text{ A}, V_{GS} = 0 \text{ V}$ (Note 3)	_	0.8	1.2	V

Note 3: Pulse test

#### **Switching Time Test Circuit**



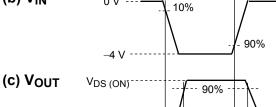
 $V_{DD} = -15 \text{ V}$   $R_G = 10 \Omega$ 

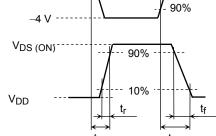
D.U. ≦ 1%

 $V_{IN}$ :  $t_r$ ,  $t_f < 5$  ns Common Source

Ta = 25°C

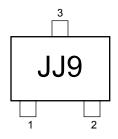
#### (b) V<sub>IN</sub>

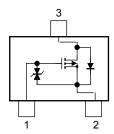




#### **Marking**

### **Equivalent Circuit (top view)**





#### **Precaution**

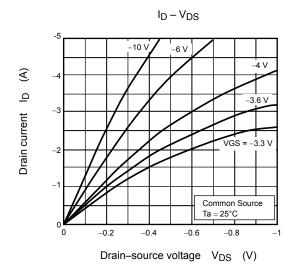
 $V_{th}$  can be expressed as the voltage between gate and source when the low operating current value is  $I_D$  = -1 mA for this product. For normal switching operation,  $V_{GS}$  (on) requires a higher voltage than  $V_{th}$  and  $V_{GS}$  (off) requires a lower voltage than  $V_{th}$ .

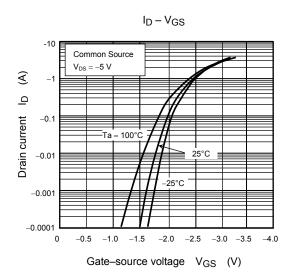
(The relationship can be established as follows:  $V_{GS (off)} < V_{th} < V_{GS (on)}$ .)

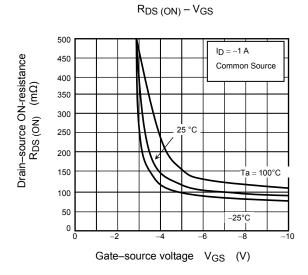
Take this into consideration when using the device.

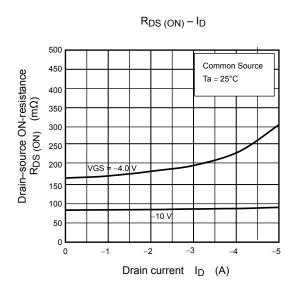
### **Handling Precaution**

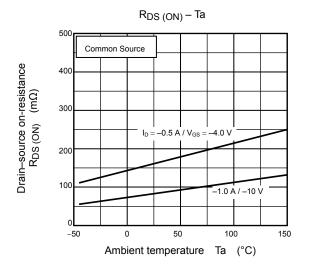
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

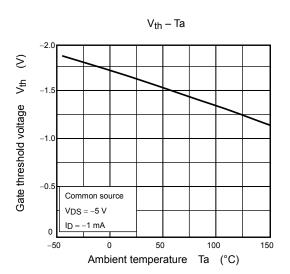


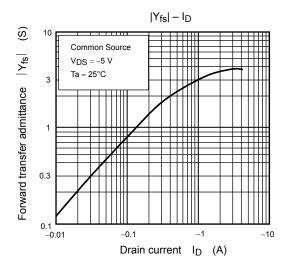


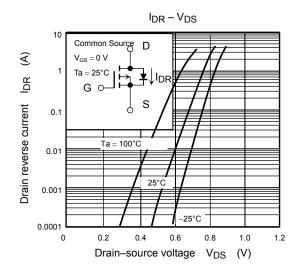


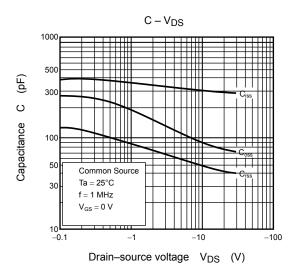


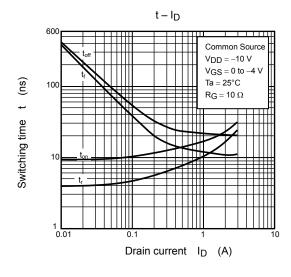


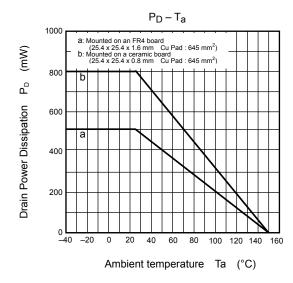


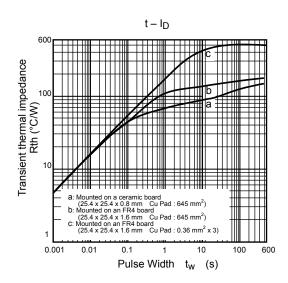












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20070701-EN GENERAL

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