TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC4520BP,TC4520BF,TC4520BFN

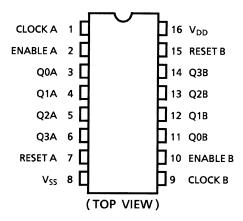
TC4520B Dual Binary Up Counter

TC4520B is up counters of 4 bit binary.

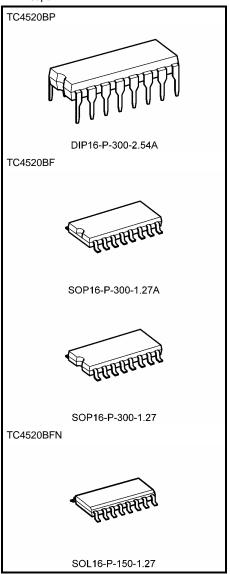
Since both of TC4520B contain two independent circuits of counters with the same functions in one package, counting or frequency division of two BCD digits or eight binary bits can be achived with one IC. The counters can be reset to "0" (Q0 \sim Q3 = "L") by giving "H" level signal to RESET input regardless of other inputs

The counting condition is changed by the rising edge of CLOCK input if ENABLE = "H" or by the falling edge of ENABLE if CLOCK = "L".

Pin Assignment



Note: xxxFN (JEDEC SOP) is not available in Japan.



Weight

 DIP16-P-300-2.54A
 : 1.00 g (typ.)

 SOP16-P-300-1.27A
 : 0.18 g (typ.)

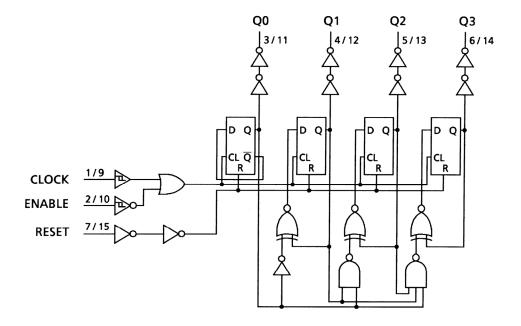
 SOP16-P-300-1.27
 : 0.18 g (typ.)

 SOL16-P-150-1.27
 : 0.13 g (typ.)

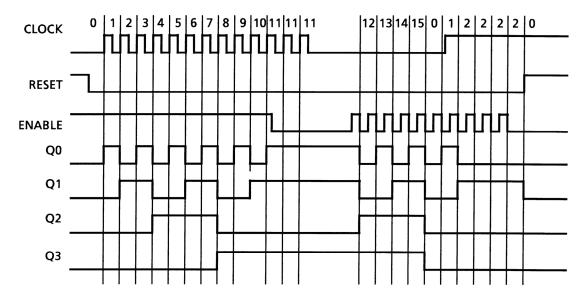
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Logic Diagram



Timing Chart



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Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
DC supply voltage	V_{DD}	V _{SS} - 0.5~V _{SS} + 20	V
Input voltage	V _{IN}	V _{SS} - 0.5~V _{DD} + 0.5	V
Output voltage	V _{OUT}	V _{SS} - 0.5~V _{DD} + 0.5	V
DC input current	I _{IN}	±10	mA
Power dissipation	P _D	300 (DIP)/180 (SOIC)	mW
Operating temperature range	T _{opr}	-40~85	°C
Storage temperature range	T _{stg}	-65~150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Recommended Operating Conditions (V_{SS} = 0 V) (Note)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
DC supply voltage	V_{DD}	_	3	_	18	V
Input voltage	V _{IN}	_	0	_	V_{DD}	V

Note: The recommended operating conditions are required to ensure the normal operation of the device.

Unused inputs must be tied to either VCC or GND.



Static Electrical Characteristics ($V_{SS} = 0 V$)

Characteristics		Sym-	Test Condition		-40°C		25°C			85°C		11.2	
		bol		V _{DD} (V)	Min	Max	Min	Тур.	Max	Min	Max	Unit	
		V _{OH}	11	5	4.95	_	4.95	5.00	_	4.95	_		
High-level output voltage	I _{OUT} < 1 μA		10	9.95	_	9.95	10.00	_	9.95	_	V		
Voltage			$V_{IN} = V_{SS}, V_{DD}$	15	14.95	_	14.95	15.00	_	14.95	_		
			I _{OUT} < 1 μA	5	_	0.05	_	0.00	0.05	_	0.05		
Low-level voltage	output	V _{OL}	$V_{IN} = V_{SS}, V_{DD}$	10	_	0.05	_	0.00	0.05	_	0.05	V	
Ü			VIN - VSS, VDD	15	_	0.05	_	0.00	0.05	_	0.05		
			V _{OH} = 4.6 V	5	-0.61	_	-0.51	-1.0	_	-0.42	_		
			V _{OH} = 2.5 V	5	-2.5	_	-2.1	-4.0	_	-1.7	_	mA	
Output hig	h current	I _{OH}	V _{OH} = 9.5 V	10	-1.5	_	-1.3	-2.2	_	-1.1	_		
			V _{OH} = 13.5 V	15	-4.0	_	-3.4	-9.0	_	-2.8	_		
			$V_{IN} = V_{SS}, V_{DD}$										
		la.	$V_{OL} = 0.4 V$	5	0.61	_	0.51	1.2	_	0.42	_	mA	
Output low	/ current		$V_{OL} = 0.5 V$	10	1.5	_	1.3	3.2	_	1.1	_		
Output low current		l _{OL}	$V_{OL} = 1.5 V$	15	4.0	_	3.4	12.0	_	2.8	_	ША	
			$V_{IN} = V_{SS}, V_{DD}$										
		V _{IH}	$V_{OUT} = 0.5 \text{ V}, 4.5 \text{ V}$	5	3.5	_	3.5	2.75	_	3.5	_	V	
Input high	voltage		$V_{OUT} = 1.0 \text{ V}, 9.0 \text{ V}$	10	7.0	_	7.0	5.5	_	7.0	_		
input nigh	voltage		V _{OUT} = 1.5 V, 13.5 V	15	11.0	_	11.0	8.25	_	11.0	_		
			$ I_{OUT} < 1 \mu A$										
		V _{IL}	V _{OUT} = 0.5 V, 4.5 V	5	_	1.5	_	2.25	1.5	_	1.5		
	V _{OUT} = 1.0 V, 9.0 V		10	_	3.0	_	4.5	3.0	_	3.0	V		
Input low voltage			V _{OUT} = 1.5 V, 13.5 V	15	_	4.0	_	6.75	4.0	_		4.0	
			$ I_{OUT} < 1 \mu A$										
Input current	"H" level	I _{IH}	V _{IH} = 18 V	18	_	0.1	_	10 ⁻⁵	0.1	_	1.0	μА	
	"L" level	I _{IL}	V _{IL} = 0 V	18	_	-0.1	_	-10 ⁻⁵	-0.1	_	-1.0	μА	
			V = V.a. V = -	5	_	5	_	0.005	5	_	150		
Quiescent current	Quiescent supply current		$V_{IN} = V_{SS}, V_{DD}$	10	_	10	_	0.010	10	_	300	μΑ	
			(Note)	15	_	20	_	0.015	20	_	600		

Note: All valid input combinations.

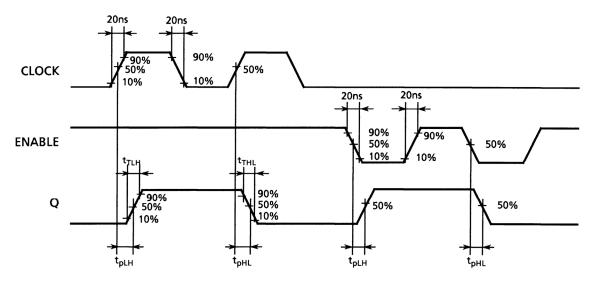


Dynamic Electrical Characteristics (Ta = 25°C, V_{SS} = 0 V, C_L = 50 pF)

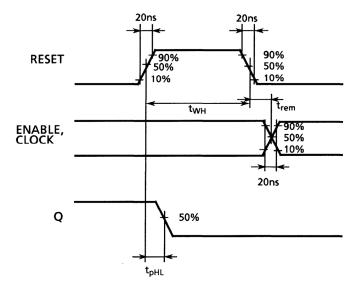
01	0 1 1	Test Condition					
Characteristics	Symbol		V _{DD} (V)	Min	Тур.	Max	Unit
			5	_	70	200	
Output transition time	t _{TLH}	_	10	_	35	100	ns
(low to high)			15	_	30	80	
			5	_	70	200	
Output transition time	t _{THL}	_	10	_	35	100	ns
(high to low)			15	_	30	80	
			5	_	160	560	
Propagation delay time	t _{pLH}	_	10	_	75	230	ns
(CLOCK, ENABLE-Q)	tpHL		15	_	60	160	
			5	_	110	560	
Propagation delay time	t _{pHL}	_	10	_	55	230	ns
(RESET-Q)	'		15	_	40	160	
			5	1.5	6	_	
Max clock frequency	t _{CL}	_	10	3	14	_	MHz
			15	4	18	_	
	t _{rCL}	_	5	No limit			
Max clock input rise/fall time			10				μS
·			15				
	t _r	_	5	No limit			
Max input rise/fall time			10				μS
(ENABLE)	t _f		15				
			5	_	30	200	
Min clock pulse width	t _W	_	10	_	15	100	ns
·			15	_	10	70	
			5	_	35	250	
Min pulse width	t _W	_	10	_	20	110	ns
(ENABLE)			15	_	15	80	
			5	_	45	250	
Min pulse width	t _{WH}	_	10	_	20	110	ns
(RESET)	****		15	_	15	80	
			5	_	_	0	
Min removal time	t _{rem}	_	10	_	_	0	ns
(RESET-CLOCK, ENABLE)	10		15	_	_	0	
Input capacitance	C _{IN}	_	I .	_	5	7.5	pF

Waveforms for Measurement of Dynamic Characteristics

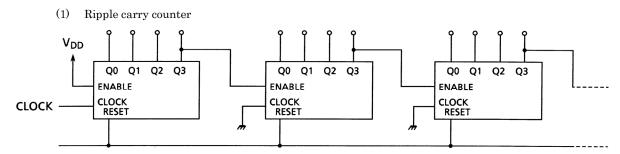
Waveform 1

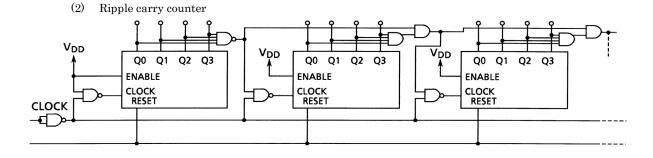


Waveform 2



Application Circuit

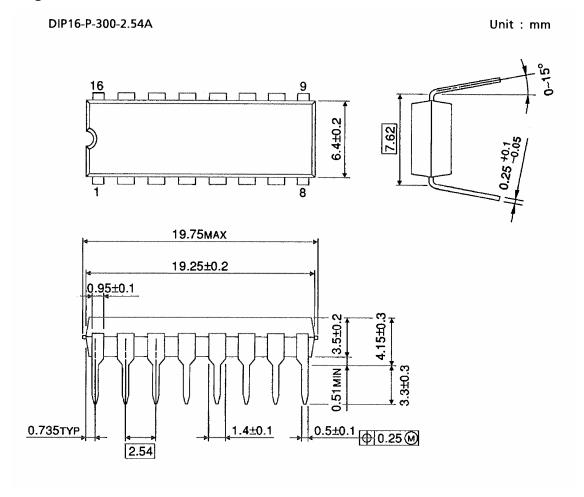




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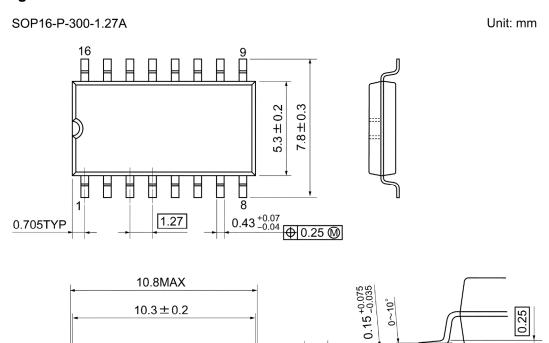
Package Dimensions



Weight: 1.00 g (typ.)

 0.8 ± 0.2

Package Dimensions



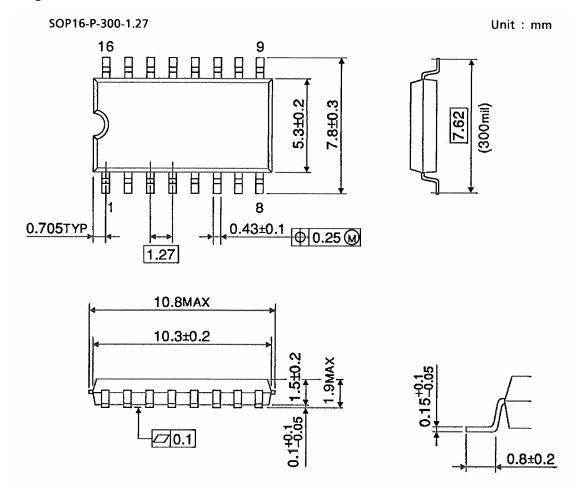
1.5±0.2 1.9MAX

□ 0.1

Weight: 0.18 g (typ.)



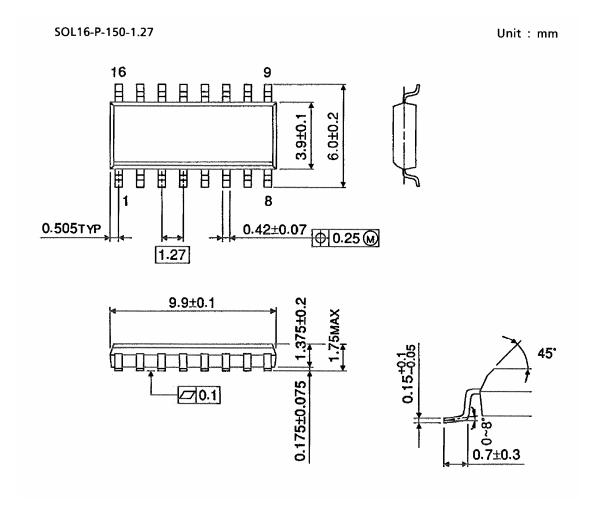
Package Dimensions



Weight: 0.18 g (typ.)



Package Dimensions (Note)



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

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Note: Lead (Pb)-Free Packages

DIP16-P-300-2.54A SOP16-P-300-1.27A SOL16-P-150-1.27

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