

MOSFETs Silicon N-channel MOS (U-MOSVII-H)

TK30E06N1

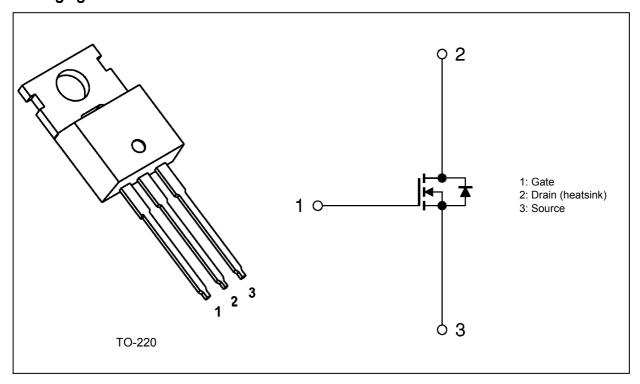
1. Applications

· Switching Voltage Regulators

2. Features

- (1) Low drain-source on-resistance: $R_{DS(ON)} = 12.2 \text{ m}\Omega$ (typ.) ($V_{GS} = 10 \text{ V}$)
- (2) Low leakage current: I_{DSS} = 10 μA (max) (V_{DS} = 60 V)
- (3) Enhancement mode: V_{th} = 2.0 to 4.0 V (V_{DS} = 10 V, I_D = 0.2 mA)

3. Packaging and Internal Circuit





4. Absolute Maximum Ratings (Note) (Ta = 25°C unless otherwise specified)

Characteristi	cs		Symbol	Rating	Unit
Drain-source voltage			V_{DSS}	60	V
Gate-source voltage			V_{GSS}	±20	
Drain current (DC)	(Silicon limit)	(Note 1), (Note 2)	Ι _D	43	Α
Drain current (DC)		(Note 1), (Note 3)	I _D	30	
Drain current (pulsed)	(t = 1 ms)	(Note 1)	I _{DP}	95	
Power dissipation	(T _c = 25°C)		P_D	53	W
Single-pulse avalanche energy		(Note 4)	E _{AS}	38	mJ
Avalanche current			I _{AR}	30	Α
Channel temperature			T _{ch}	150	°C
Storage temperature			T _{stg}	-55 to 150]

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	R _{th(ch-c)}	2.34	°C/W
Channel-to-ambient thermal resistance	R _{th(ch-a)}	83.3	

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: Limited by silicon chip capability.

Note 3: Device mounted with heatsink so that $R_{th(ch-a)}$ becomes 5.00°C/W.

Note 4: V_{DD} = 48 V, T_{ch} = 25°C (initial), L = 32.8 μ H, I_{AR} = 30 A

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.



6. Electrical Characteristics

6.1. Static Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current	I _{GSS}	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±0.1	μΑ
Drain cut-off current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V	_	-	10	
Drain-source breakdown voltage	V _{(BR)DSS}	I _D = 10 mA, V _{GS} = 0 V	60	_	_	V
Drain-source breakdown voltage (Note 5)	V _{(BR)DSX}	I _D = 10 mA, V _{GS} = -20 V	45	_	_	
Gate threshold voltage	V _{th}	V _{DS} = 10 V, I _D = 0.2 mA	2.0	_	4.0	
Drain-source on-resistance	R _{DS(ON)}	V _{GS} = 10 V, I _D = 15 A	_	12.2	15.0	mΩ

Note 5: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

6.2. Dynamic Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C _{iss}	V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz	_	1050		pF
Reverse transfer capacitance	C _{rss}		_	33	_	
Output capacitance	C _{oss}		_	400	_	
Gate resistance	r _g	_	_	3.9		Ω
Switching time (rise time)	t _r	See Figure 6.2.1.	_	7.3	_	ns
Switching time (turn-on time)	t _{on}		_	21	_	
Switching time (fall time)	t _f		_	7.3		
Switching time (turn-off time)	t _{off}		_	28		

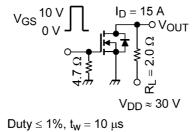


Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Qg	$V_{DD} \approx 48 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 30 \text{ A}$	1	16	1	nC
Gate-source charge 1	Q _{gs1}			5.2		
Gate-drain charge	Q_{gd}			4.4		
Gate switch charge	Q _{SW}		_	6.8		



6.4. Source-Drain Characteristics (T_a = 25°C unless otherwise specified)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Reverse drain current (DC)	(Note 6)	I _{DR}	_	_	_	30	Α
Reverse drain current (pulsed)	(Note 6)	I _{DRP}		_	_	95	
Diode forward voltage		V _{DSF}	I _{DR} = 30 A, V _{GS} = 0 V	_	_	-1.2	V
Reverse recovery time	(Note 7)	t _{rr}	I _{DR} = 30 A, V _{GS} = 0 V	_	39	_	ns
Reverse recovery charge	(Note 7)	Q _{rr}	-dI _{DR} /dt = 100 A/μs	_	39	_	nC

Note 6: Ensure that the channel temperature does not exceed 150°C.

Note 7: Ensure that V_{DS} peak does not exceed V_{DSS} .

7. Marking

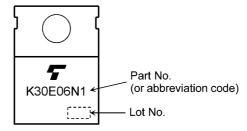


Fig. 7.1 Marking

8. Characteristics Curves (Note)

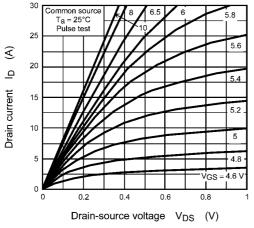
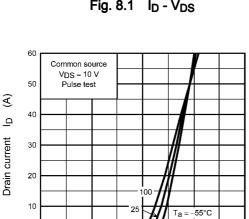


Fig. 8.1 I_D - V_{DS}



Gate-source voltage V_{GS} (V) Fig. 8.3 ID - VGS

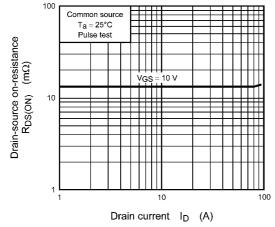


Fig. 8.5 R_{DS(ON)} - I_D

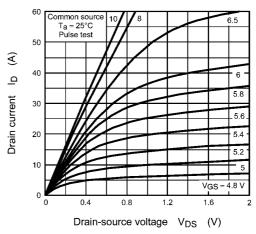


Fig. 8.2 I_D - V_{DS}

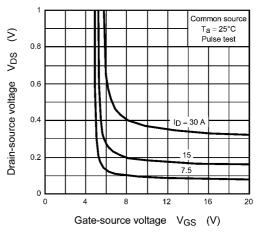


Fig. 8.4 V_{DS} - V_{GS}

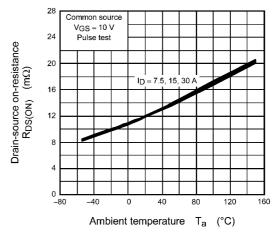


Fig. 8.6 R_{DS(ON)} - T_a

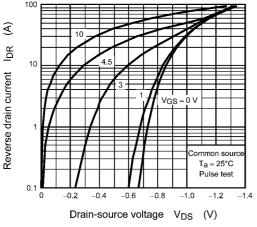


Fig. 8.7 IDR - VDS

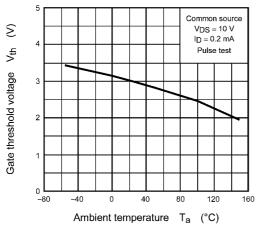


Fig. 8.9 V_{th} - T_a

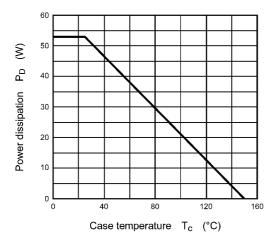


Fig. 8.11 P_D - T_c (Guaranteed Maximum)

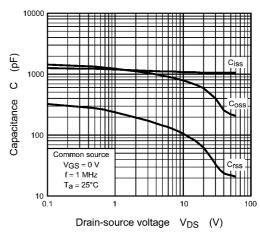


Fig. 8.8 Capacitance - V_{DS}

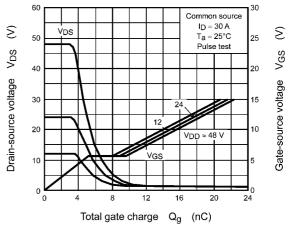


Fig. 8.10 Dynamic Input/Output Characteristics

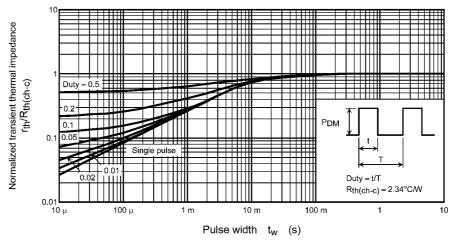


Fig. 8.12 r_{th}/R_{th(ch-c)} - t_w (Guaranteed Maximum)

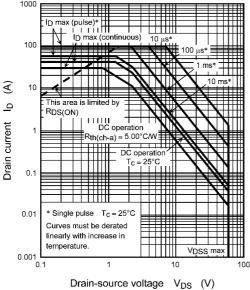


Fig. 8.13 Safe Operating Area (Guaranteed Maximum)

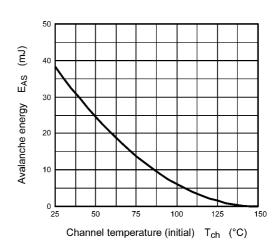


Fig. 8.14 E_{AS} - T_{ch} (Guaranteed Maximum)

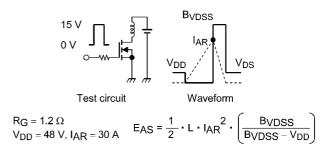


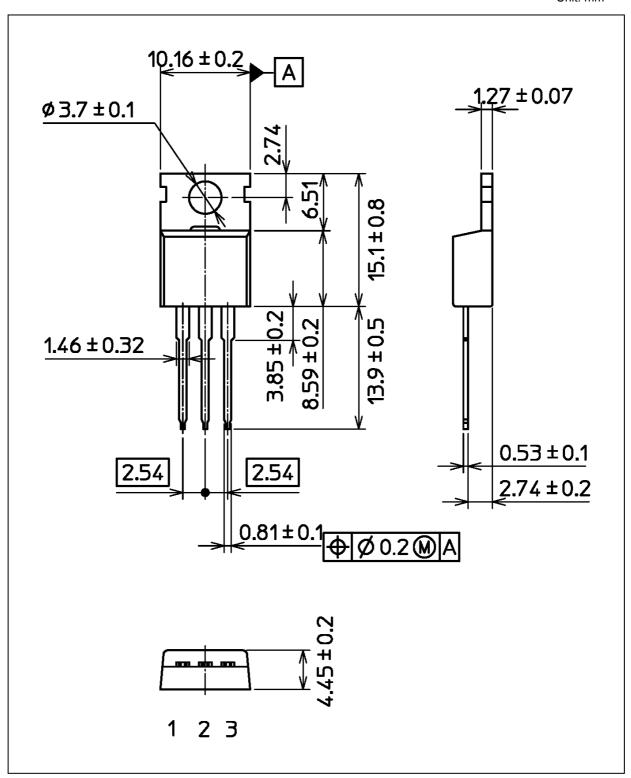
Fig. 8.15 Test Circuit/Waveform

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



Package Dimensions

Unit: mm



Weight: 1.93 g (typ.)

	Package Name(s)
TOSHIBA: 2-10X1A	
Nickname: TO-220	



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