Device Modeling Report

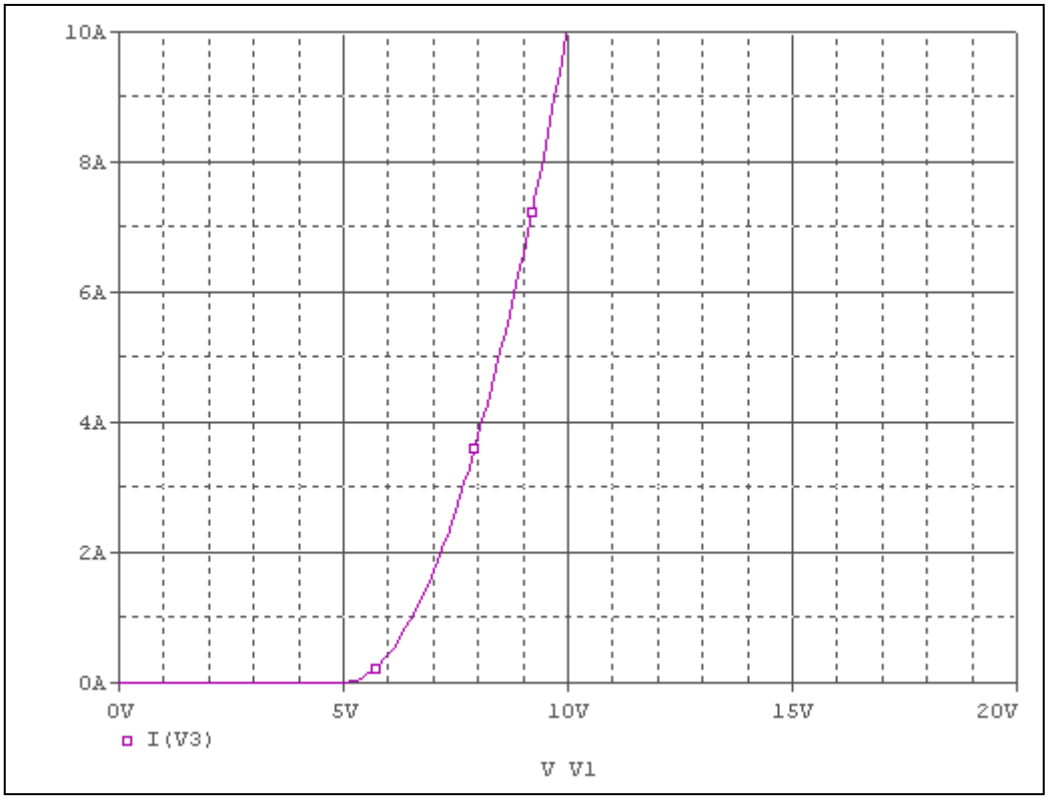
COMPONENTS: Insulated Gate Bipolar Transistor (IGBT)
PART NUMBER: GT8J102(SM)
MANUFACTURER: TOSHIBA

Bee Technologies Inc.

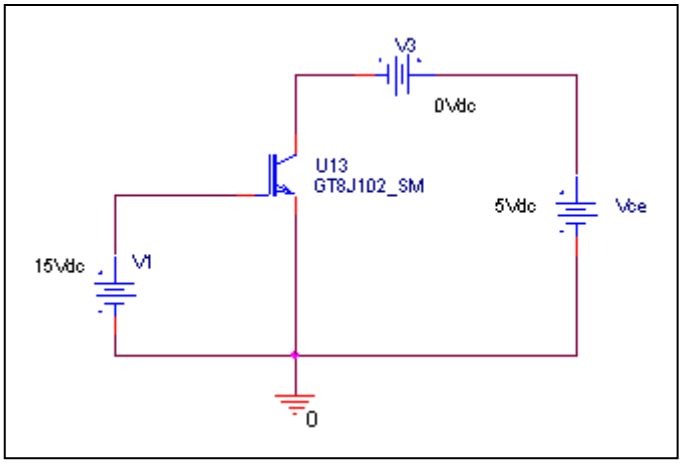
PSpice model parameter	Model description
TAU	Ambipolar Recombination Lifetime
KP	MOS Transconductance
AREA	Area of the Device
AGD	Gate-Drain Overlap Area
WB	Metallurgical Base Width
VT	Threshold Voltage
KF	Triode Region Factor
CGS	Gate-Source Capacitance per Unit Area
COXD	Gate-Drain Oxide Capacitance per Unit Area
VTD	Gate-Drain Overlap Depletion Threshold

Transfer Characteristics

Circuit Simulation result

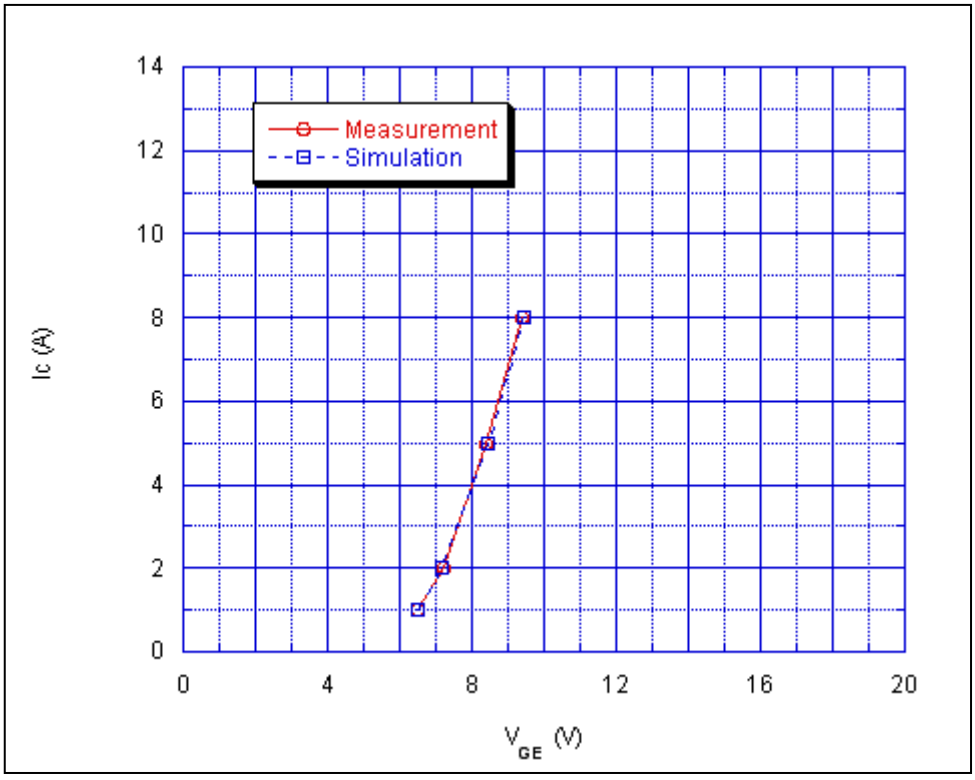


Evaluation circuit



Comparison Graph

Circuit Simulation Result



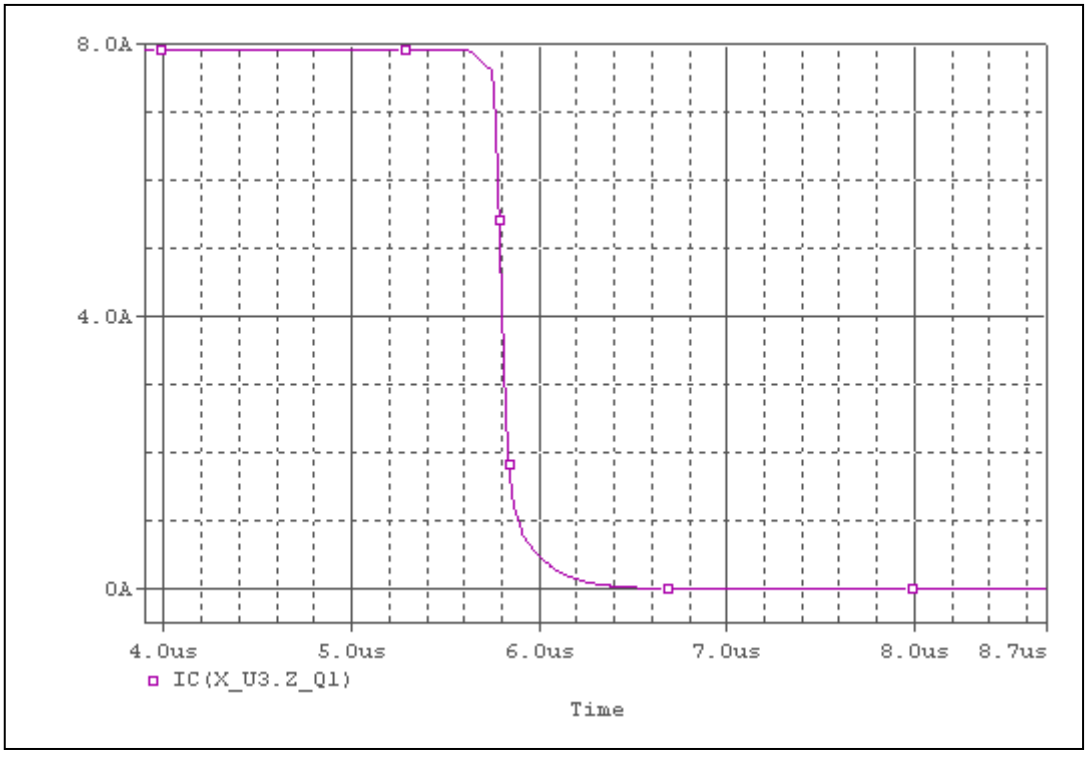
Simulation Result

Test condition : Vce = 5 V

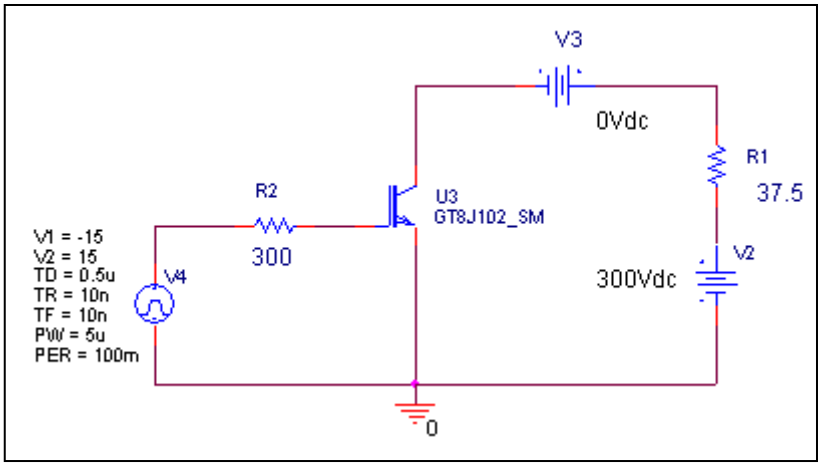
Ic(A)	Vge(V)		Error (%)
	Measurement	Simulation	
1	6.5	6.5169	0.26000
2	7.2	7.1605	-0.54861
5	8.4	8.4675	0.80357
8	9.4	9.4297	0.31596

Fall Time Characteristics

Circuit Simulation result



Evaluation circuit

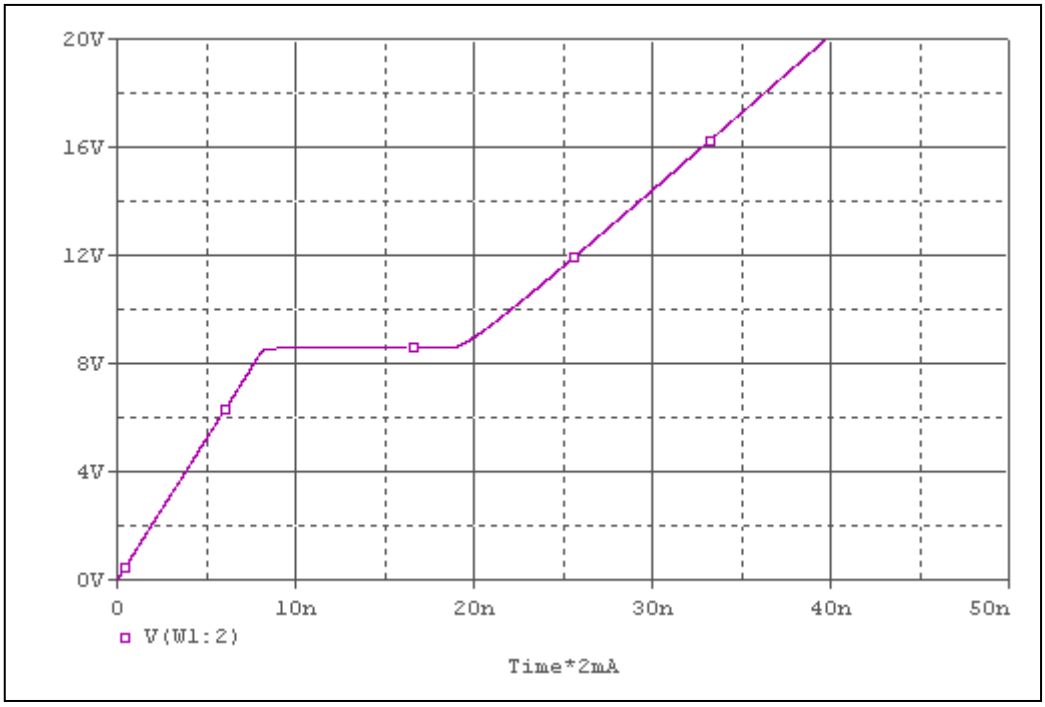


Test condition Ic=8(A) ,Vce=300(V)

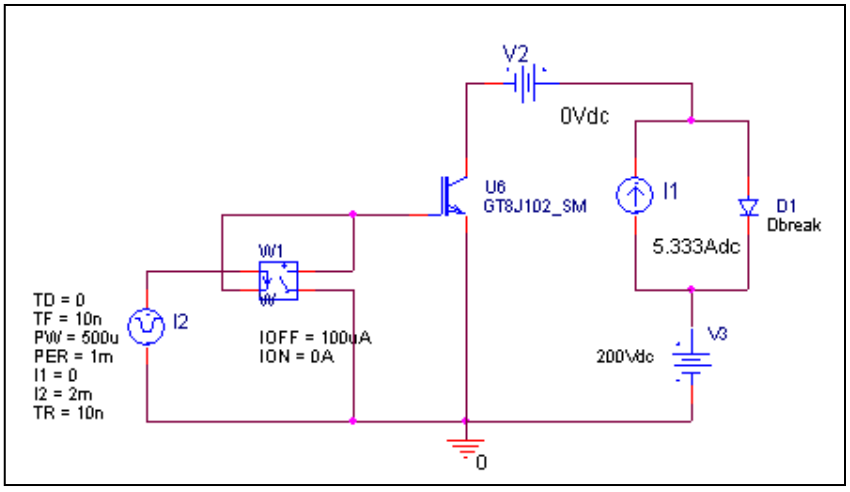
tf	Measurement		Simulation		Error
	0.15	us	0.155571	us	3.71400

Gate Charge Characteristics

Circuit Simulation result



Evaluation circuit

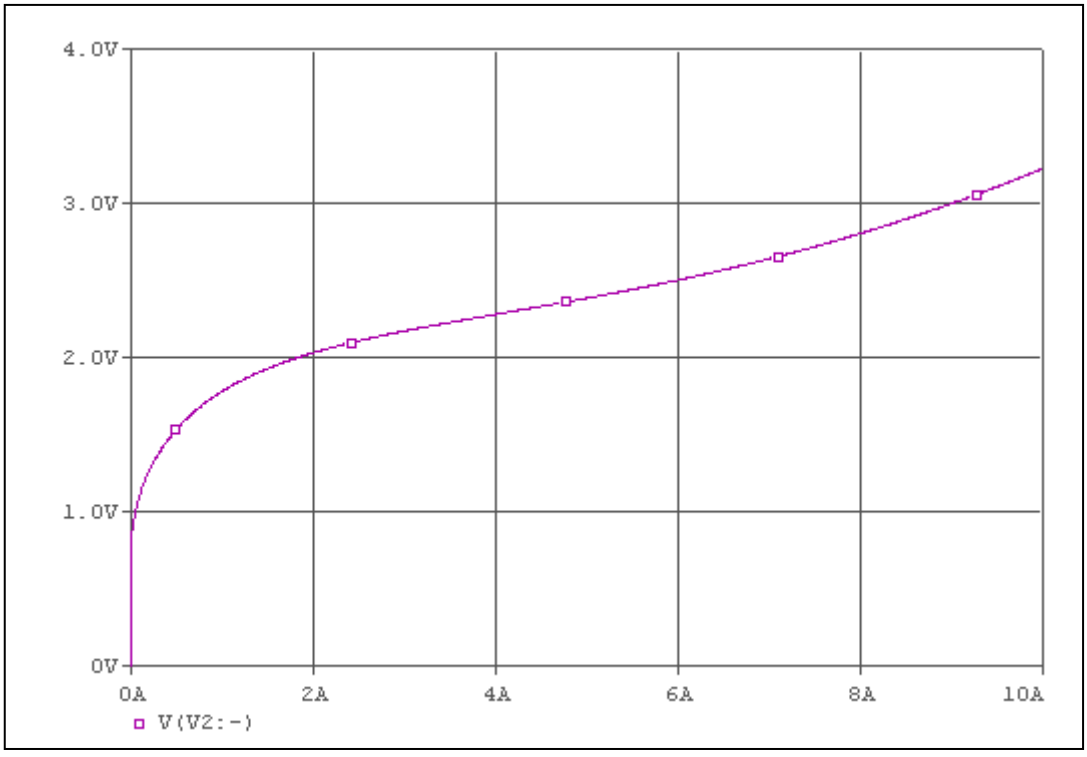


Test condition : Vcc=200(V) ,Ic=5.333(A) ,Vge=16(V)

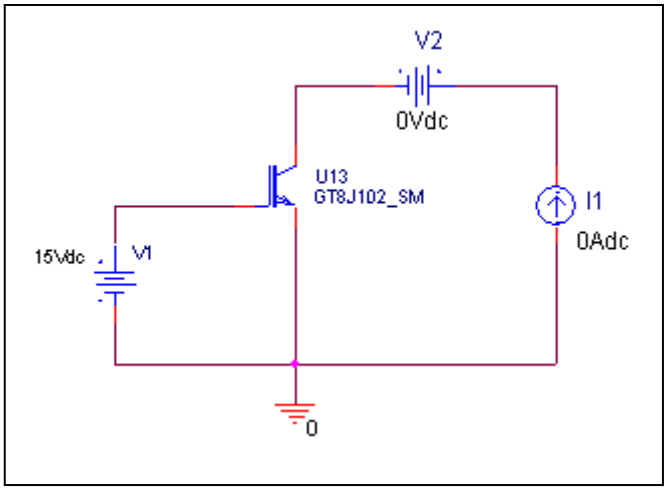
	Measurement		Simulation		Error(%)
Qge	8	nc	8.0871	nc	1.08875
Qgc	11	nc	11.070	nc	0.63636
Qg	33	nc	32.865	nc	-0.40909

Saturation Characteristics

Circuit Simulation result

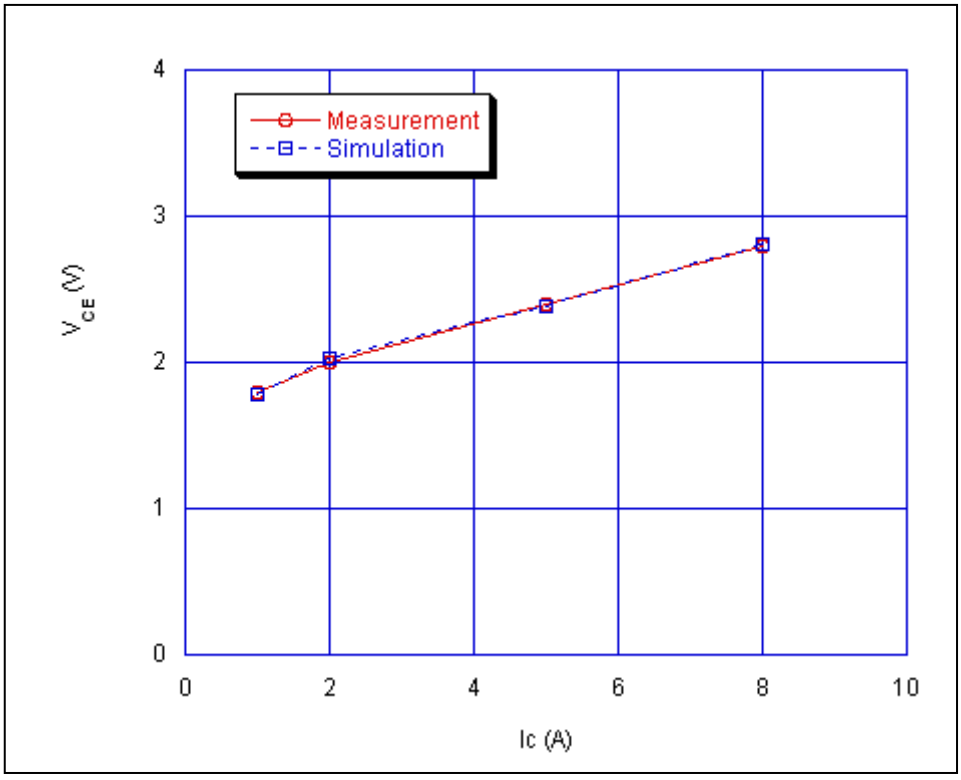


Evaluation circuit



Comparison Graph

Circuit Simulation Result



Simulation Result

Ic(A)	Vce(sat)(V)		Error (%)
	Measurement	Simulation	
1	1.8	1.7805	-1.08333
2	2	2.0304	1.52000
5	2.4	2.3848	-0.63333
8	2.8	2.8043	0.15357