

Device Modeling Report

COMPONENTS: Insulated Gate Bipolar Transistor (IGBT)
PART NUMBER: GT15J102
MANUFACTURER: TOSHIBA

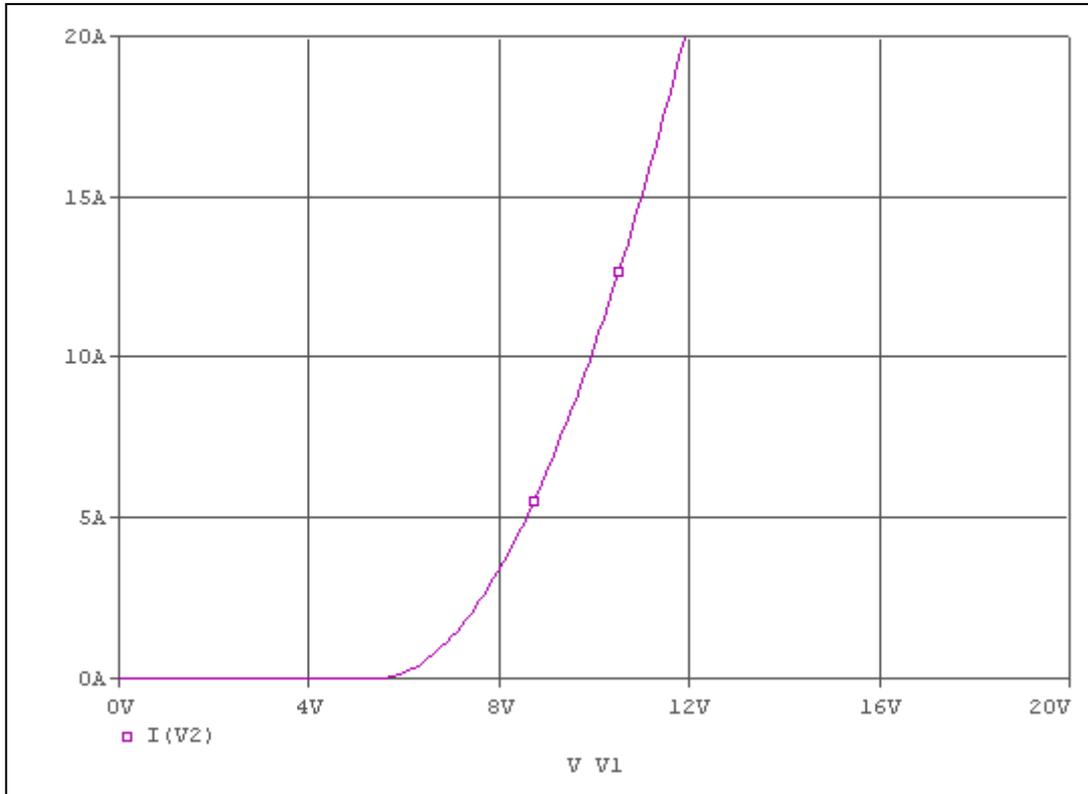


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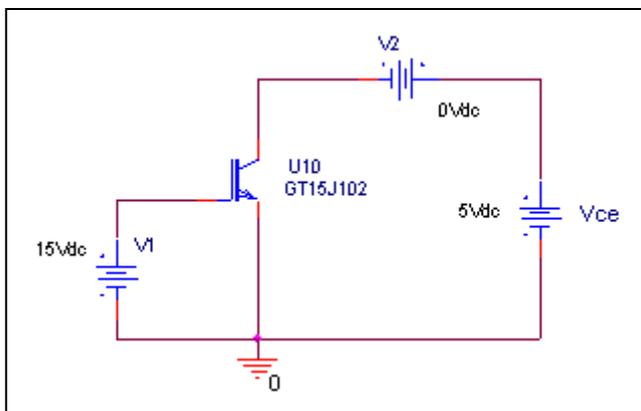
P Spice model parameter	Model description
TAU	Ambipolar Recombination Lifetime
KP	MOS Transconductance
AREA	Area of the Device
AGD	Gate-Drain Overlap Area
WB	Metallurgical Base Width
VT	Threshold Voltage
KF	Triode Region Factor
CGS	Gate-Source Capacitance per Unit Area
COXD	Gate-Drain Oxide Capacitance per Unit Area
VTD	Gate-Drain Overlap Depletion Threshold

Transfer Characteristics

Circuit Simulation result

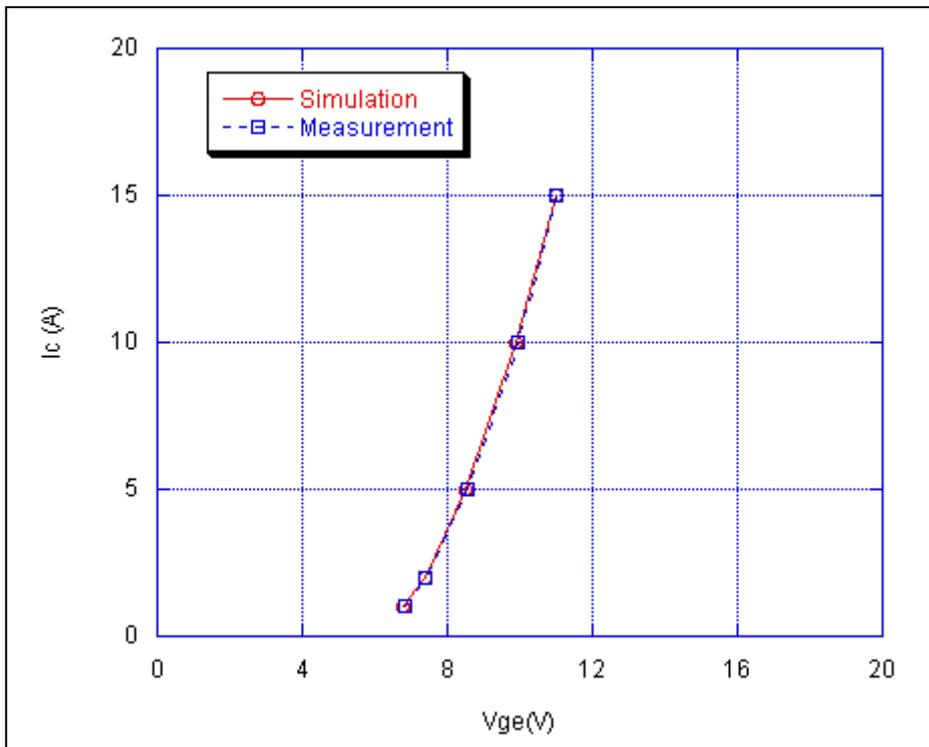


Evaluation circuit



Comparison Graph

Circuit Simulation Result



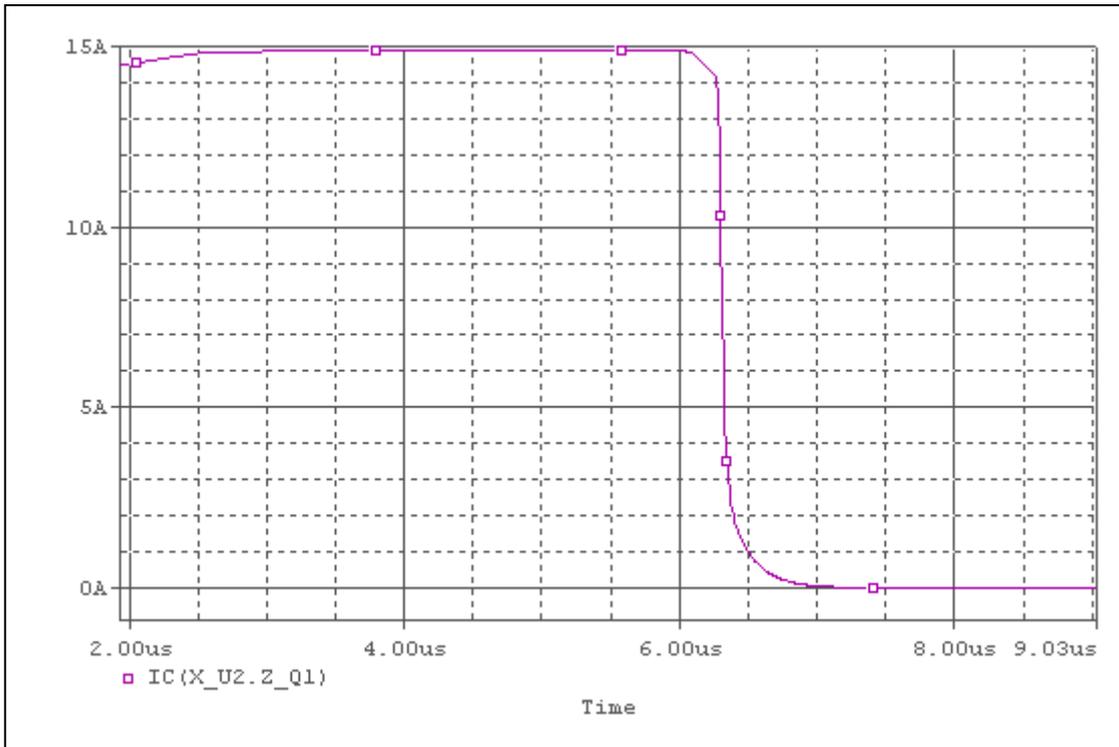
Simulation Result

Test condition : $V_{ce} = 5 \text{ V}$

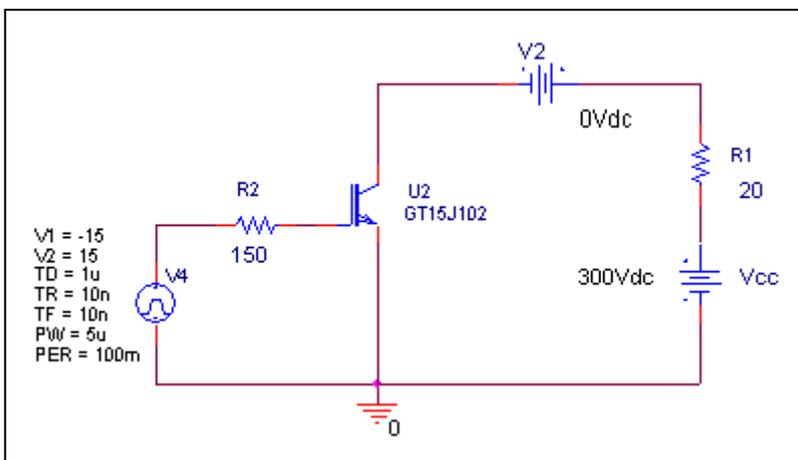
Ic(A)	Vge(V)		Error (%)
	Measurement	Simulation	
1	6.8	6.8090	0.13235
2	7.4	7.3933	-0.09054
5	8.5	8.5843	0.99176
10	9.9	9.925	0.25253
15	11	10.997	-0.02727

Fall Time Characteristics

Circuit Simulation result



Evaluation circuit

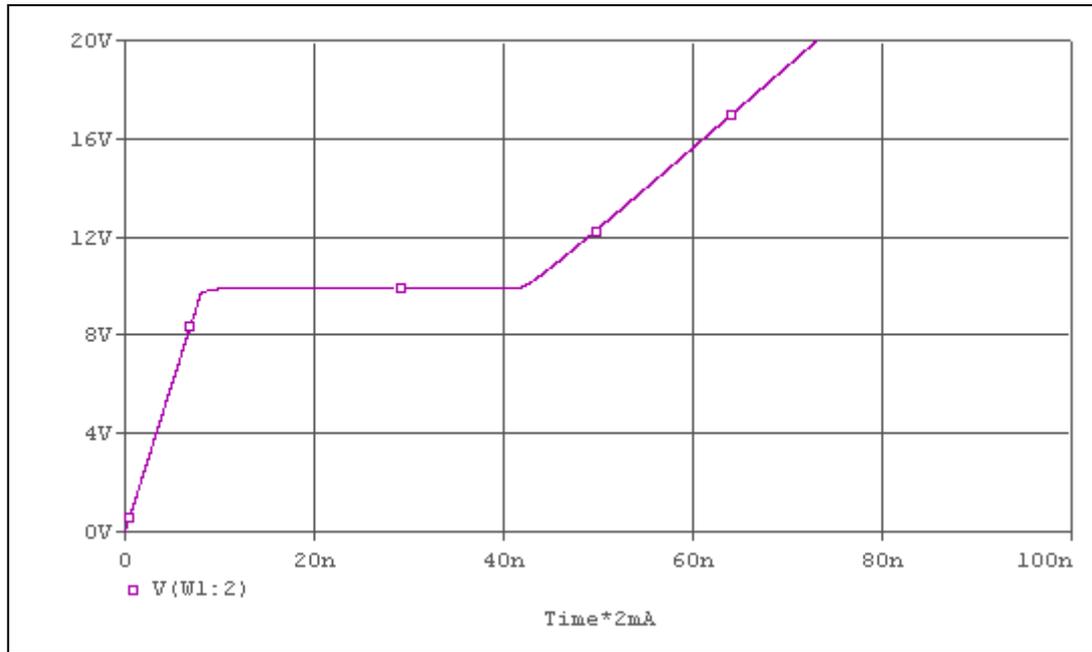


Test condition $I_c=15(\text{A})$, $V_{cc}=300(\text{V})$

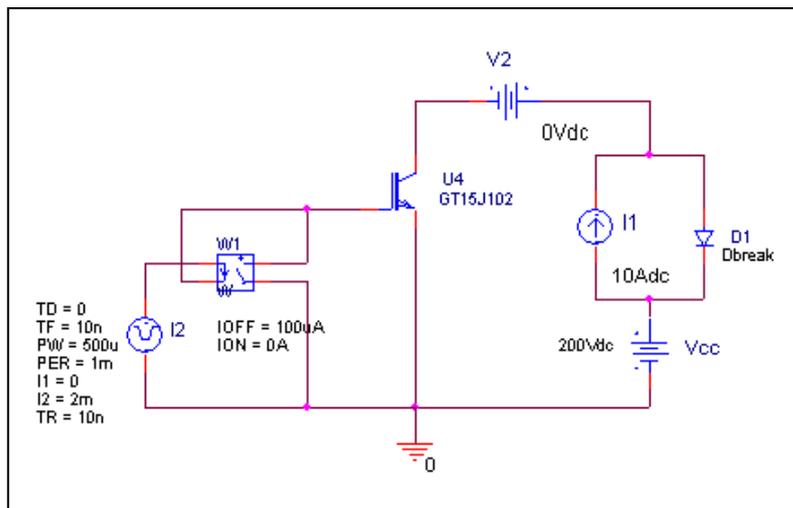
tf	Measurement		Simulation		Error
	150	ns	150.347	ns	

Gate Charge Characteristics

Circuit Simulation result



Evaluation circuit

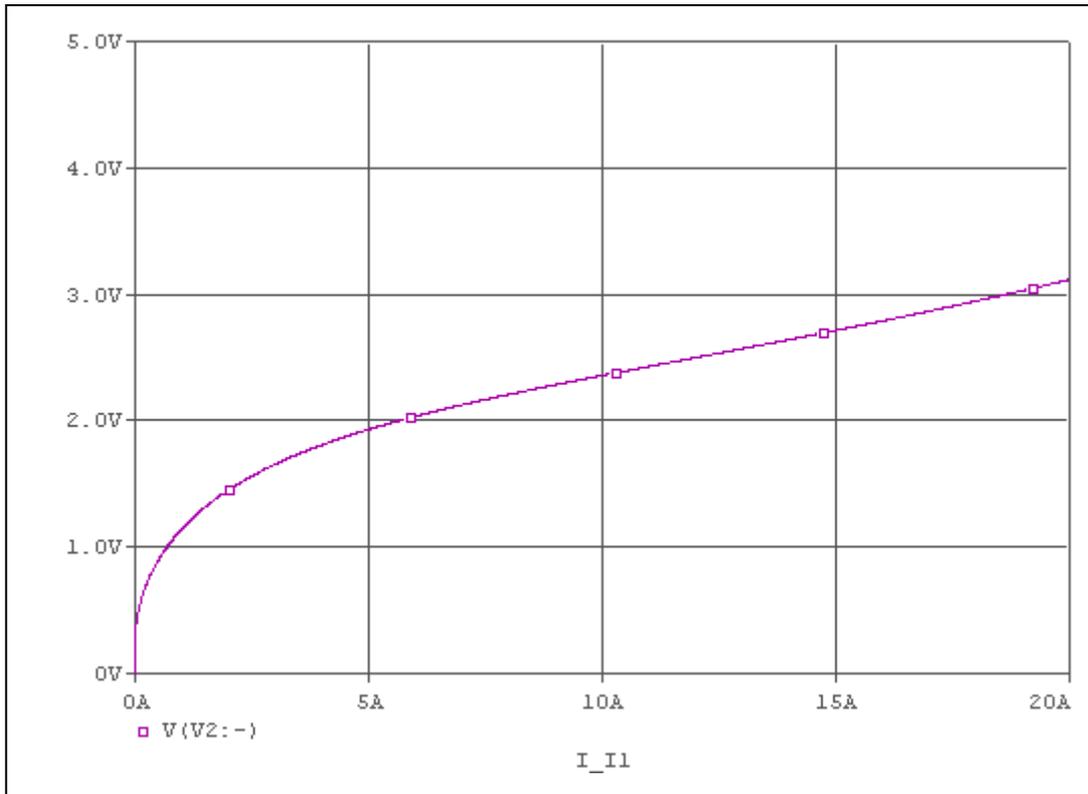


Test condition : $V_{cc}=200(V)$, $I_c=20(A)$, $V_{ge}=16(V)$

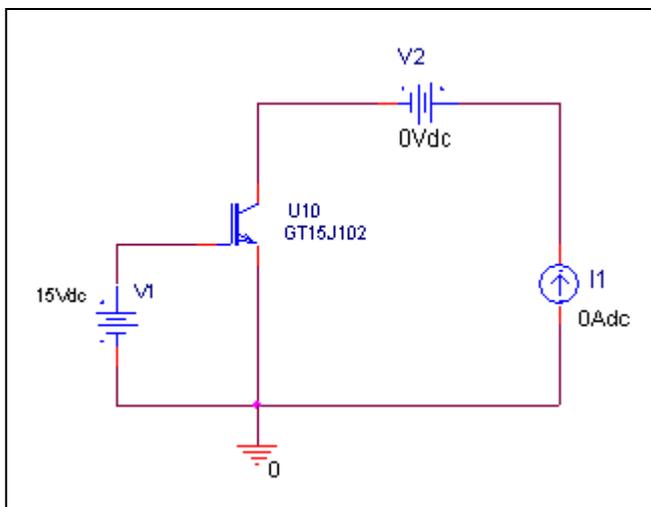
	Measurement		Simulation		Error(%)
Qge	8	nc	8.0899	nc	1.12375
Qgc	32	nc	33.371	nc	4.28438
Qg	61	nc	61.195	nc	0.31967

Saturation Characteristics

Circuit Simulation result

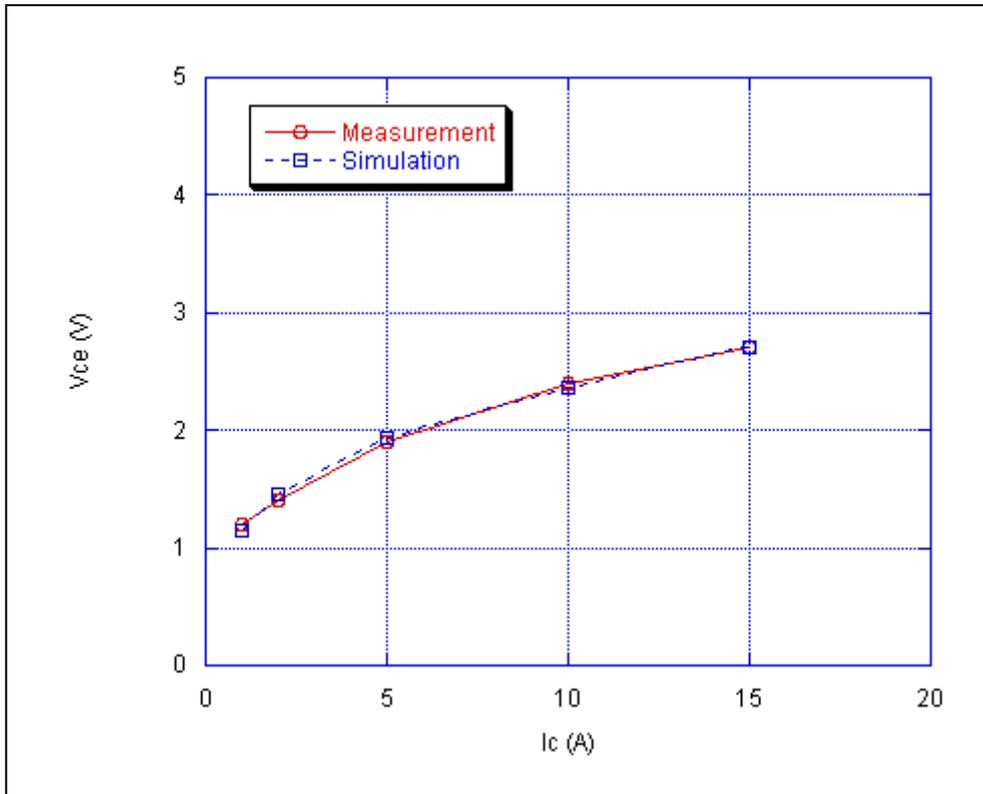


Evaluation circuit



Comparison Graph

Circuit Simulation Result



Simulation Result

Ic(A)	Vce(sat)(V)		Error (%)
	Measurement	Simulation	
1	1.2	1.1448	-4.60000
2	1.4	1.4522	3.72857
5	1.9	1.9306	1.61053
10	2.4	2.3577	-1.76250
15	2.7	2.7147	0.54444