Device Modeling Report

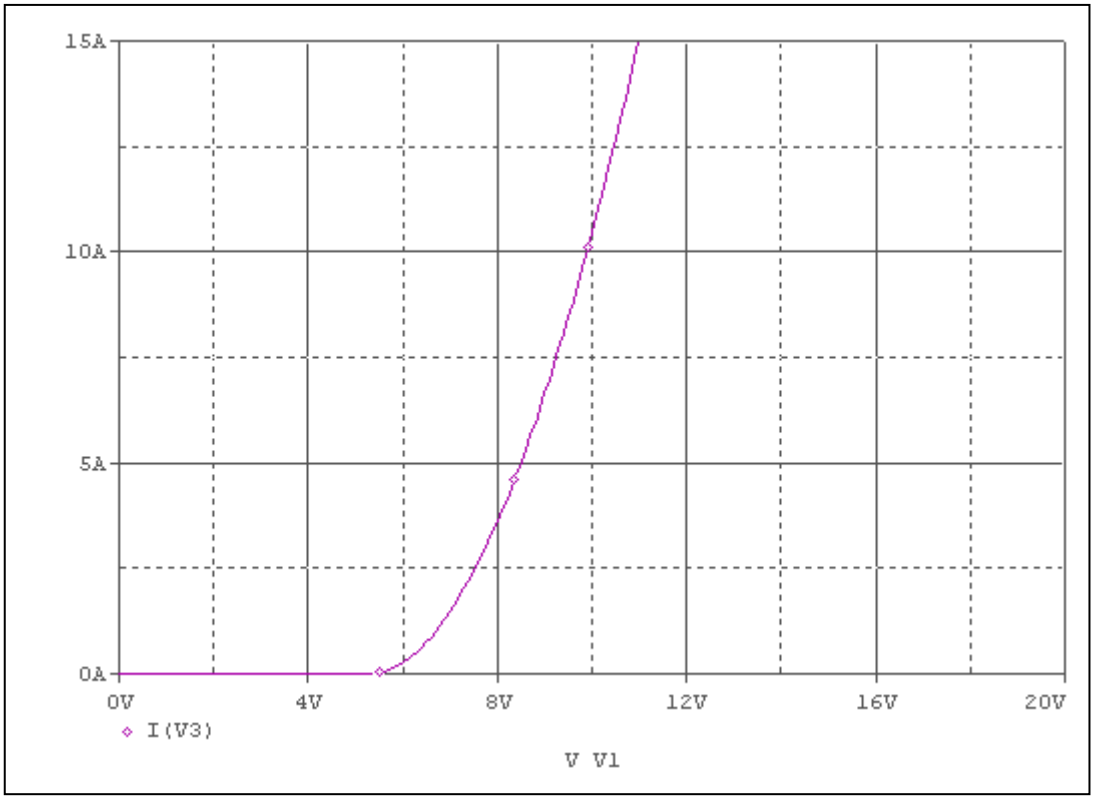
COMPONENTS: Insulated Gate Bipolar Transistor (IGBT)
PART NUMBER: GT15J103(SM)
MANUFACTURER: TOSHIBA

Bee Technologies Inc.

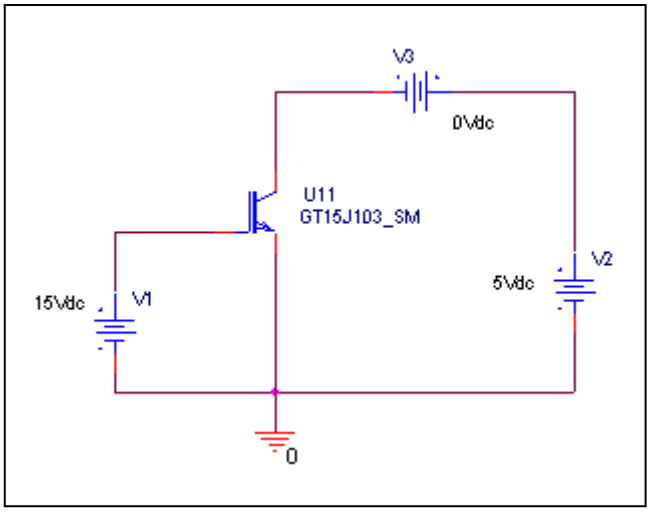
PSpice model parameter	Model description
TAU	Ambipolar Recombination Lifetime
KP	MOS Transconductance
AREA	Area of the Device
AGD	Gate-Drain Overlap Area
WB	Metallurgical Base Width
VT	Threshold Voltage
KF	Triode Region Factor
CGS	Gate-Source Capacitance per Unit Area
COXD	Gate-Drain Oxide Capacitance per Unit Area
VTD	Gate-Drain Overlap Depletion Threshold

Transfer Characteristics

Circuit Simulation result

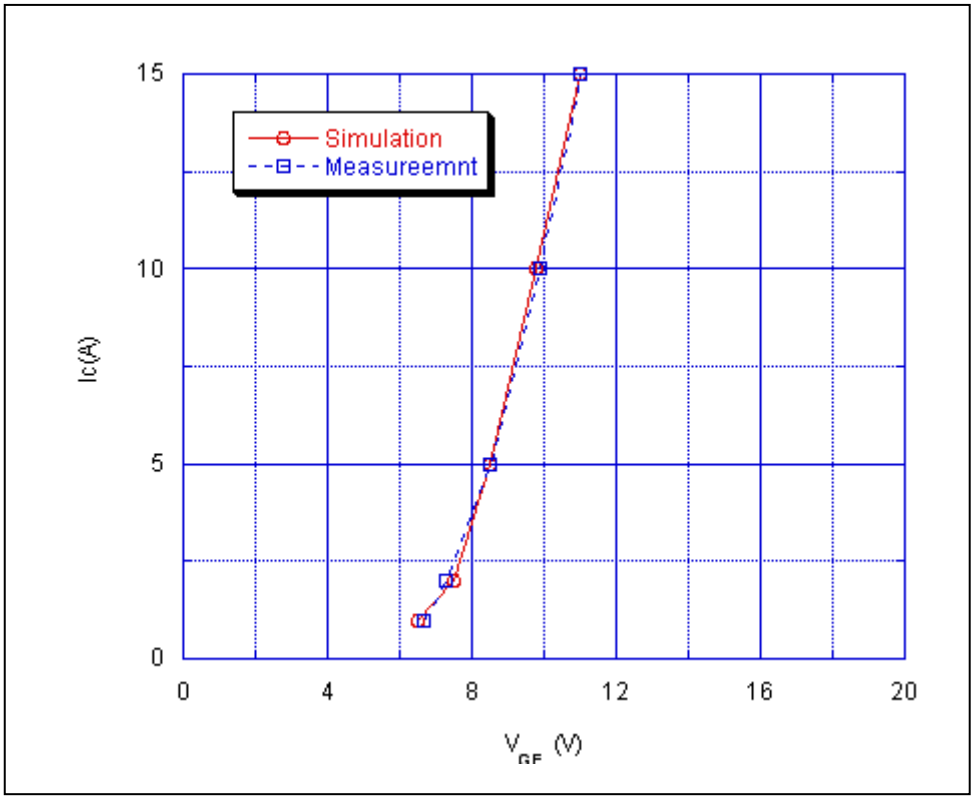


Evaluation circuit



Comparison Graph

Circuit Simulation Result



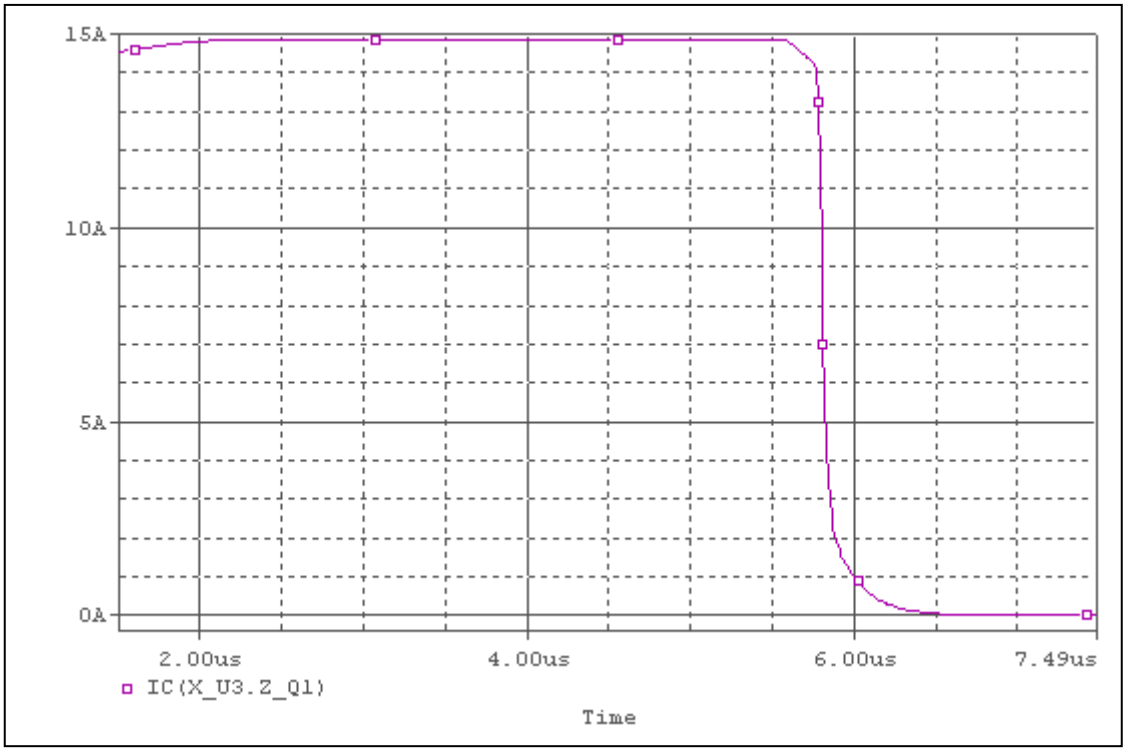
Simulation Result

Test condition : Vce = 5 V

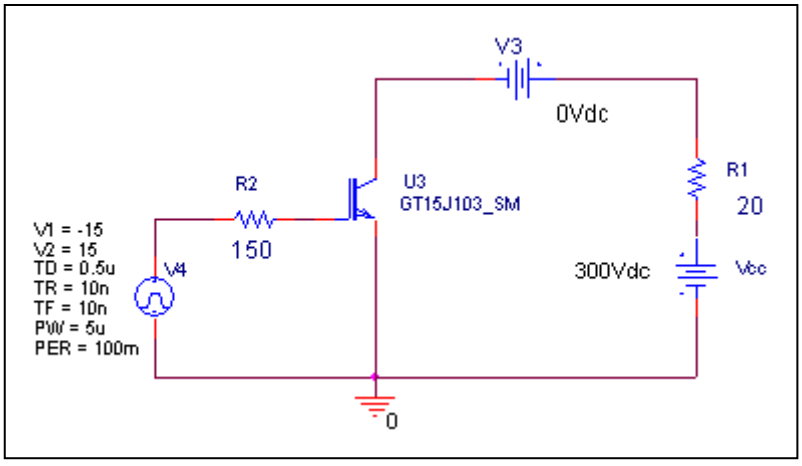
Ic(A)	Vge(V)		Error (%)
	Measurement	Simulation	
1	6.5	6.6966	3.02462
2	7.5	7.3034	-2.62133
5	8.5	8.5003	0.00353
10	9.8	9.896	0.97959
15	11	10.983	-0.15455

Fall Time Characteristics

Circuit Simulation result



Evaluation circuit

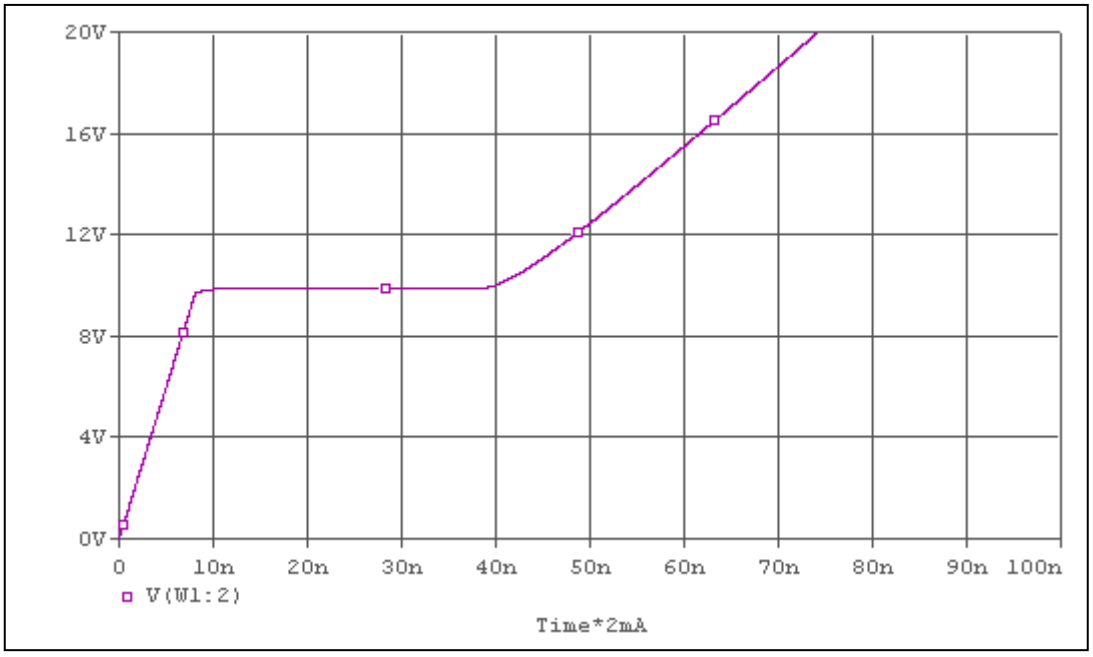


Test condition Ic=15(A) ,Vcc=300(V)

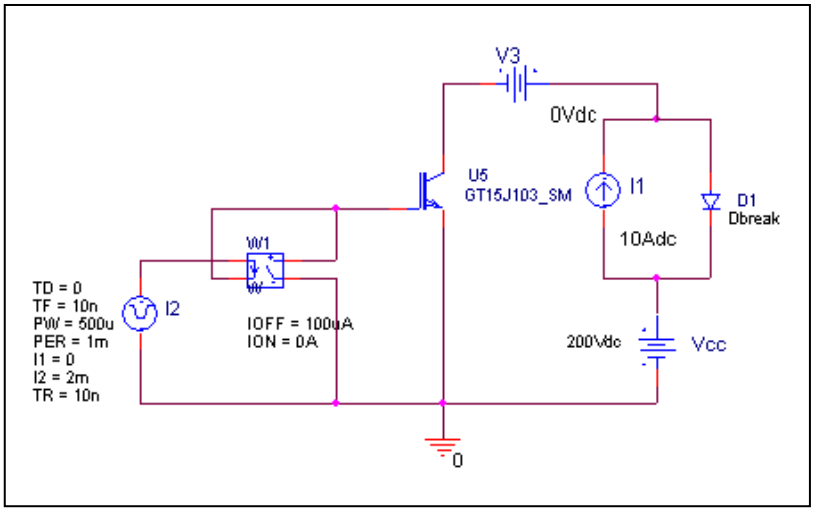
tf	Measurement		Simulation		Error
	150	ns	151.755	ns	1.17000

Gate Charge Characteristics

Circuit Simulation result



Evaluation circuit

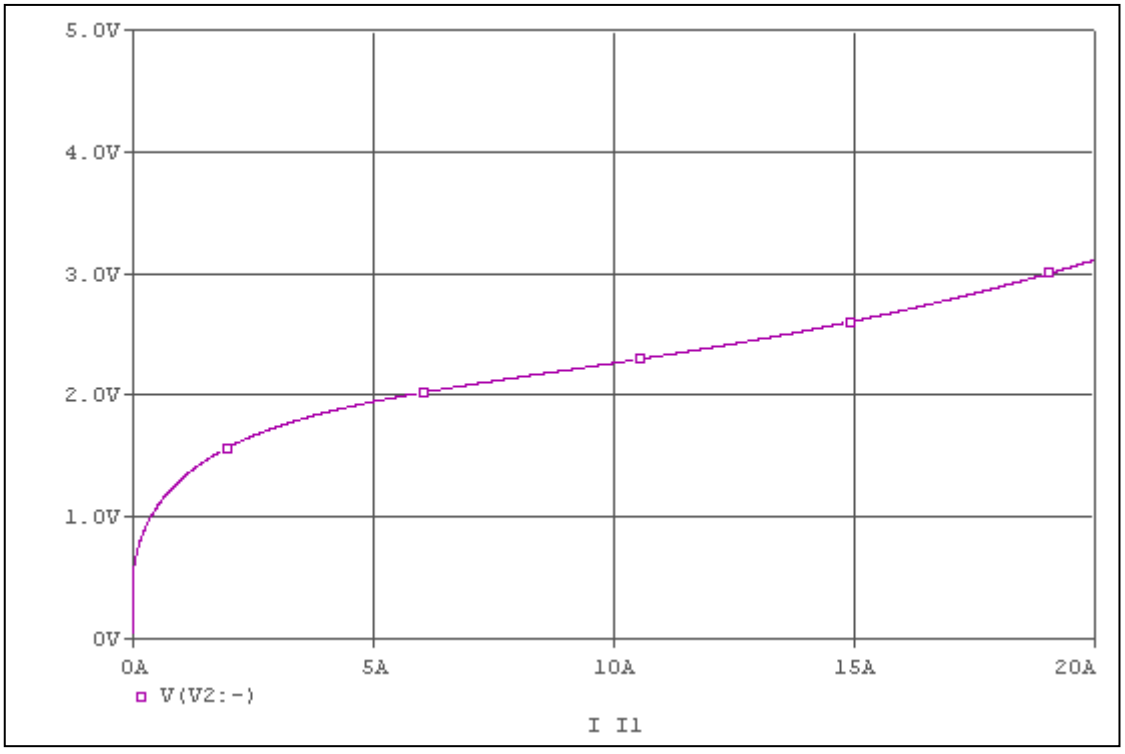


Test condition : Vcc=200(V) ,Ic=10(A) ,Vge=16(V)

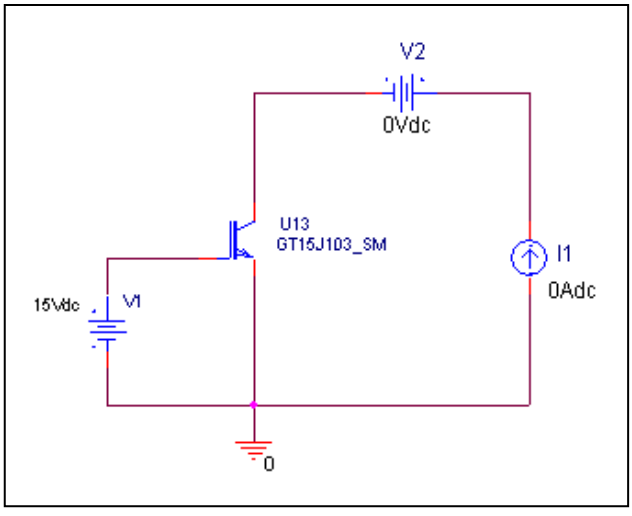
	Measurement		Simulation		Error(%)
Qge	8	nc	8.1140	nc	1.42500
Qgc	32	nc	31.549	nc	-1.40938
Qg	62	nc	61.727	nc	-0.44032

Saturation Characteristics

Circuit Simulation result

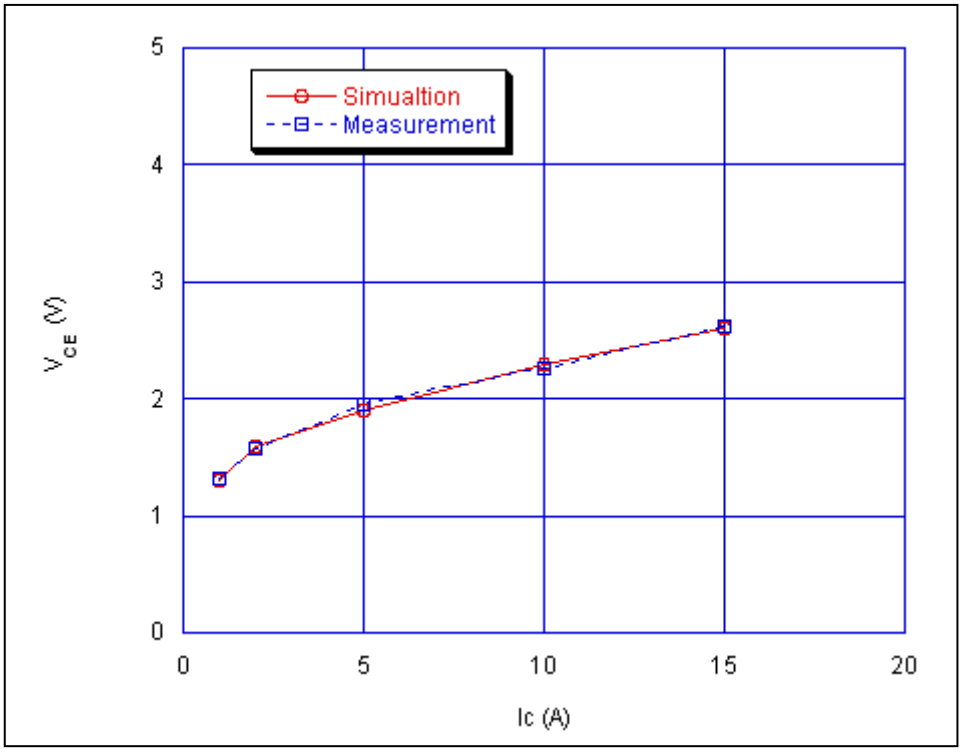


Evaluation circuit



Comparison Graph

Circuit Simulation Result



Simulation Result

Ic(A)	Vce(sat)(V)		Error (%)
	Measurement	Simulation	
1	1.3	1.3182	1.40000
2	1.6	1.5769	-1.44375
5	1.9	1.9474	2.49474
10	2.3	2.2645	-1.54348
15	2.6	2.6159	0.61154