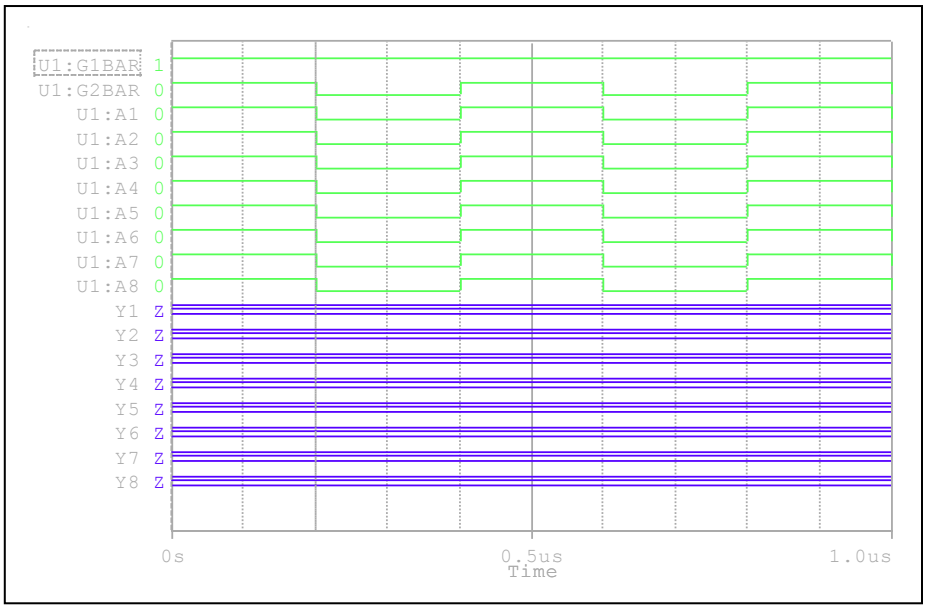
Device Modeling Report

COMPONENTS : CMOS DIGITAL INTEGRATED CIRCUIT
PART NUMBER : TC74VHCT541AFT
MANUFACTURER : TOSHIBA

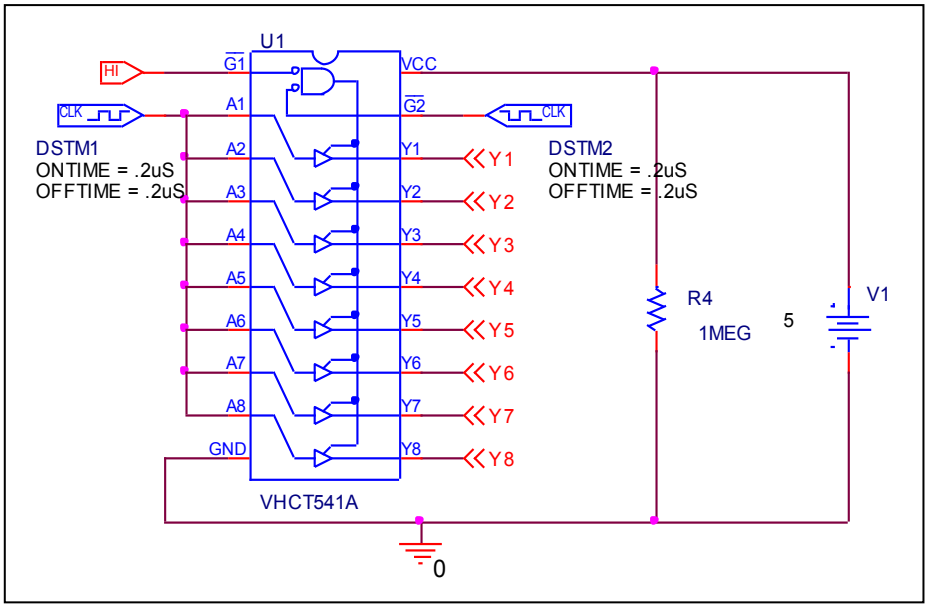
Bee Technologies Inc.

Truth Table

Circuit simulation result



Evaluation circuit

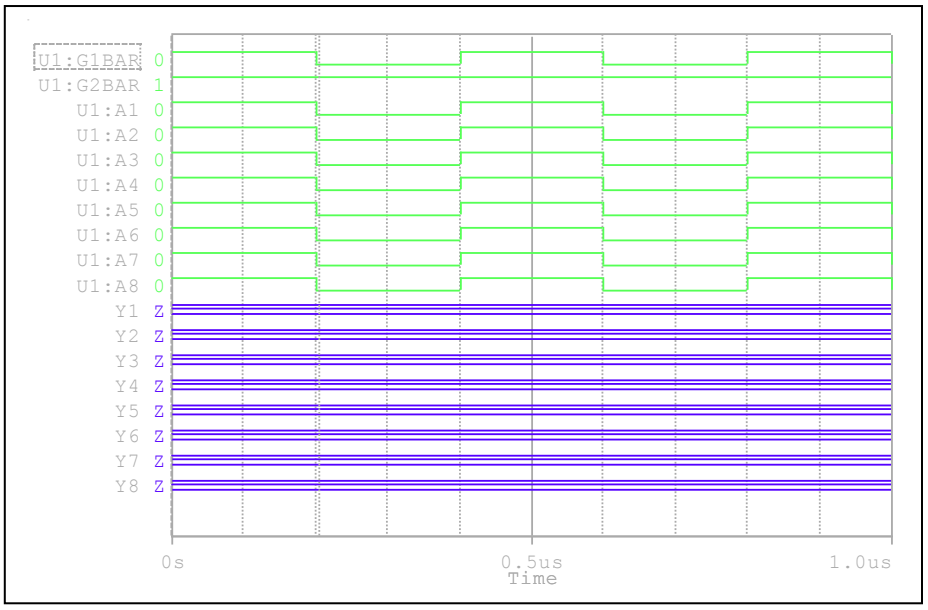


Comparison table

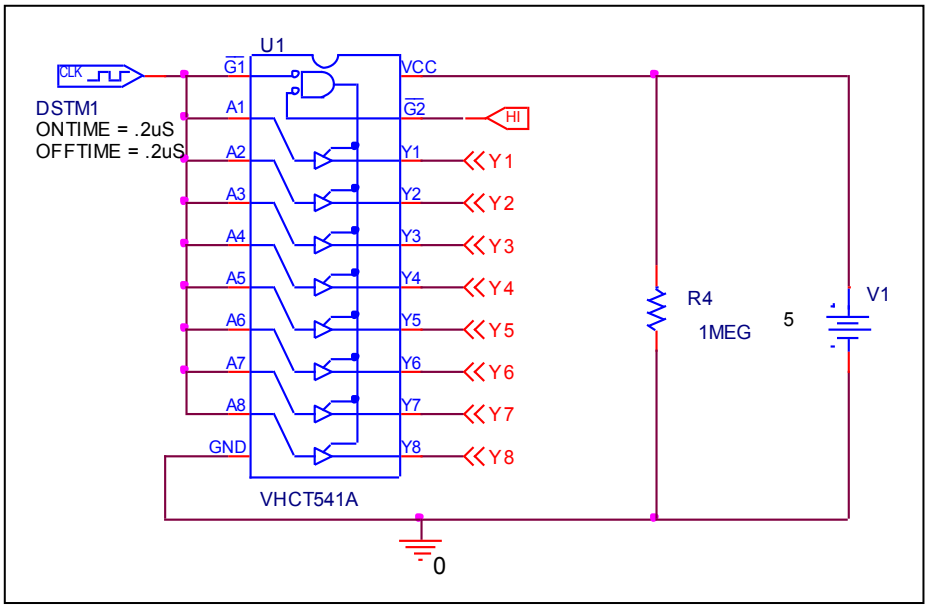
Input			Output		%Error
$\overline{OE1}$	$\overline{OE2}$	An	Yn (Measurement)	Yn (Simulation)	
H	X	X	Z	Z	0

Truth Table

Circuit simulation result



Evaluation circuit

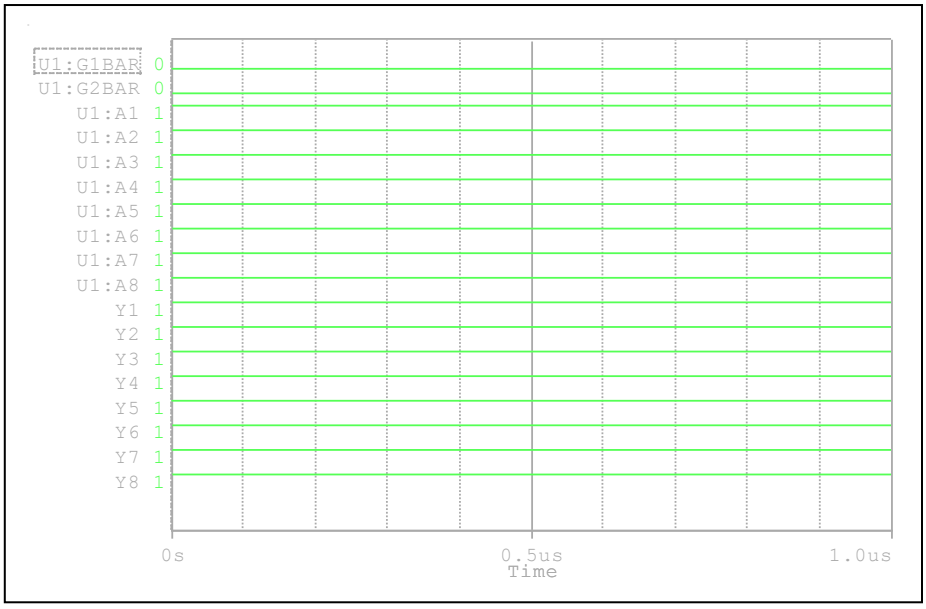


Comparison table

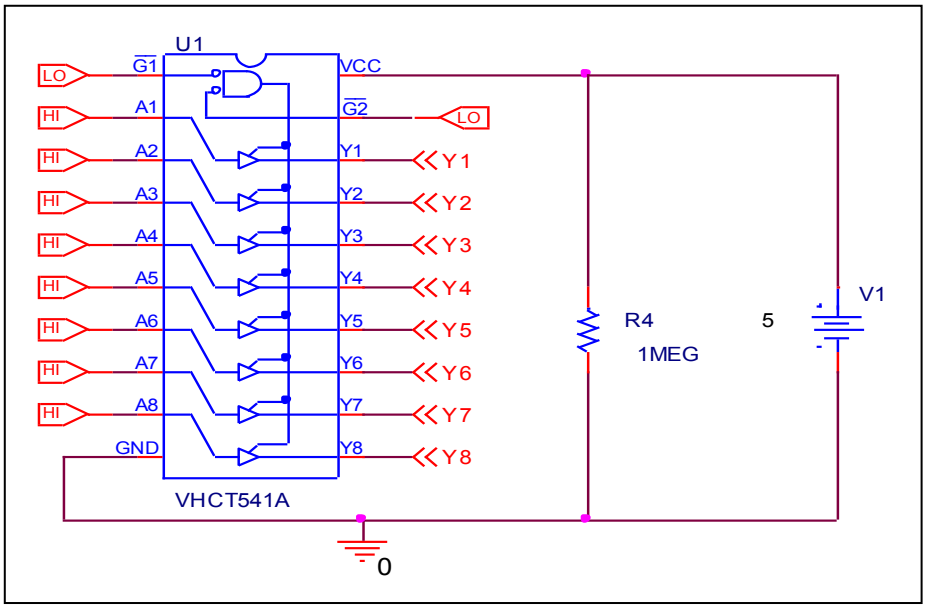
Input			Output		%Error
$\overline{OE1}$	$\overline{OE2}$	An	Yn (Measurement)	Yn (Simulation)	
X	H	X	Z	Z	0

Truth Table

Circuit simulation result



Evaluation circuit

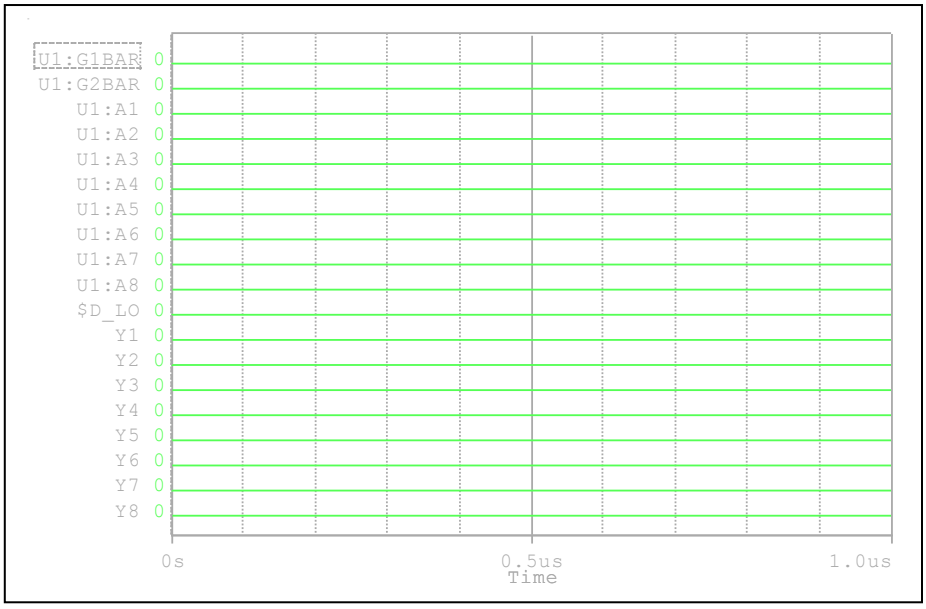


Comparison table

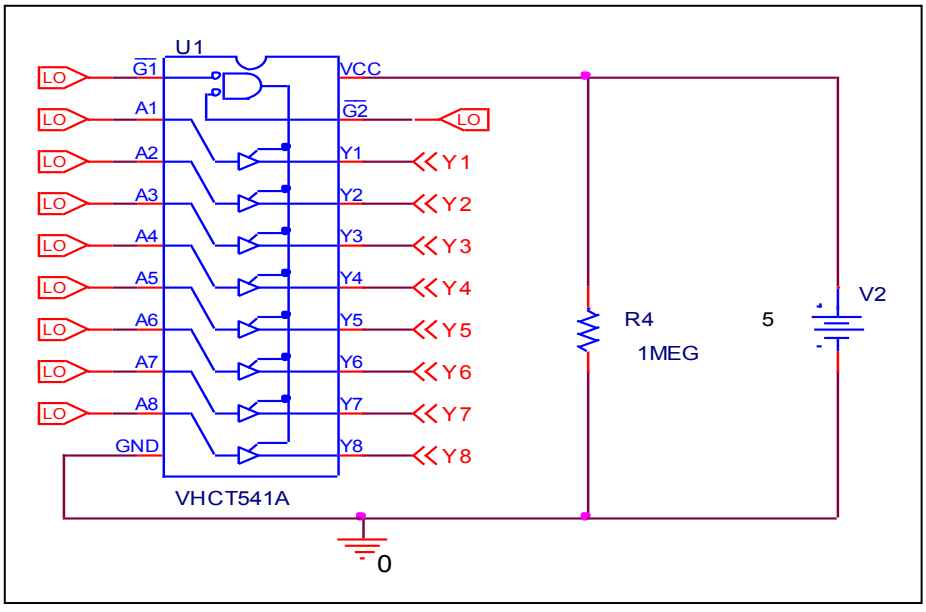
Input			Output		%Error
$\overline{OE1}$	$\overline{OE2}$	An	Yn (Measurement)	Yn (Simulation)	
L	L	H	H	H	0

Truth Table

Circuit simulation result



Evaluation circuit

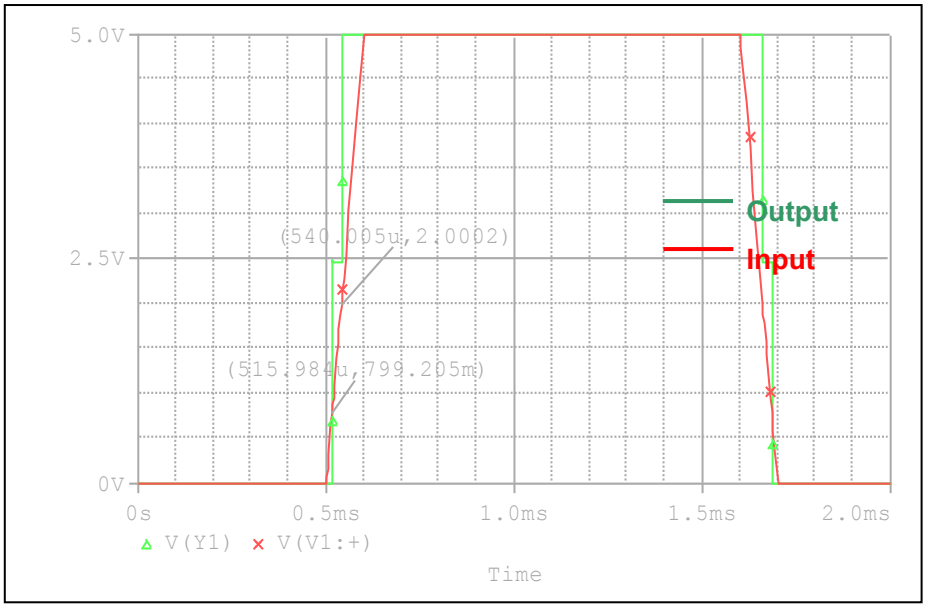


Comparison table

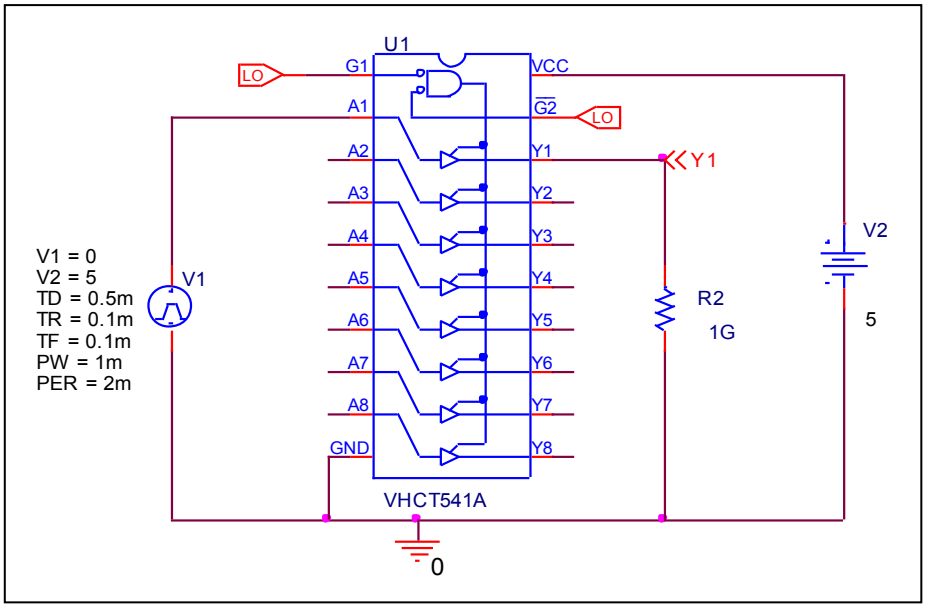
Input			Output		%Error
$\overline{OE1}$	$\overline{OE2}$	An	Yn (Measurement)	Yn (Simulation)	
L	L	L	L	L	0

High Level and Low Level Input Voltage

Circuit simulation result



Evaluation circuit

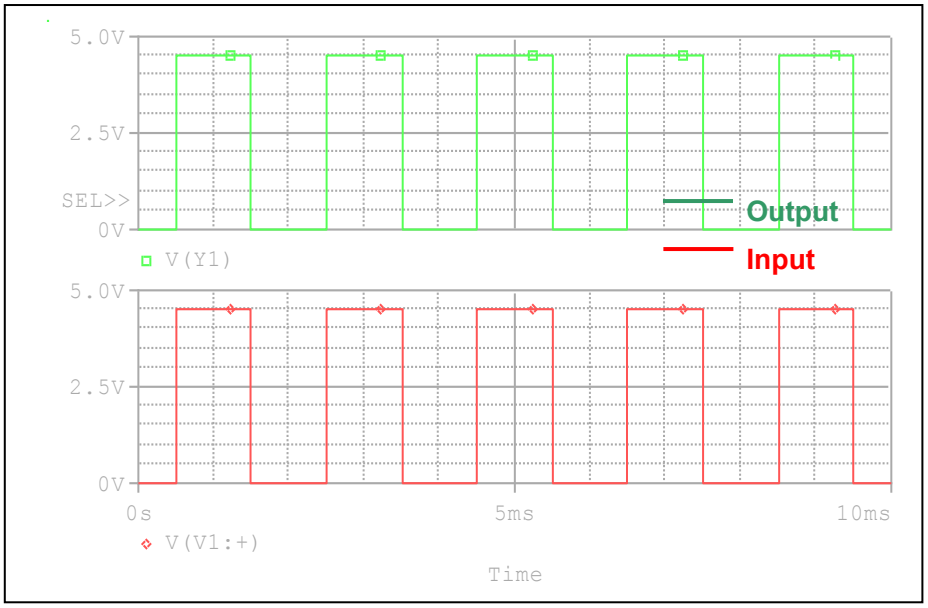


Comparison table

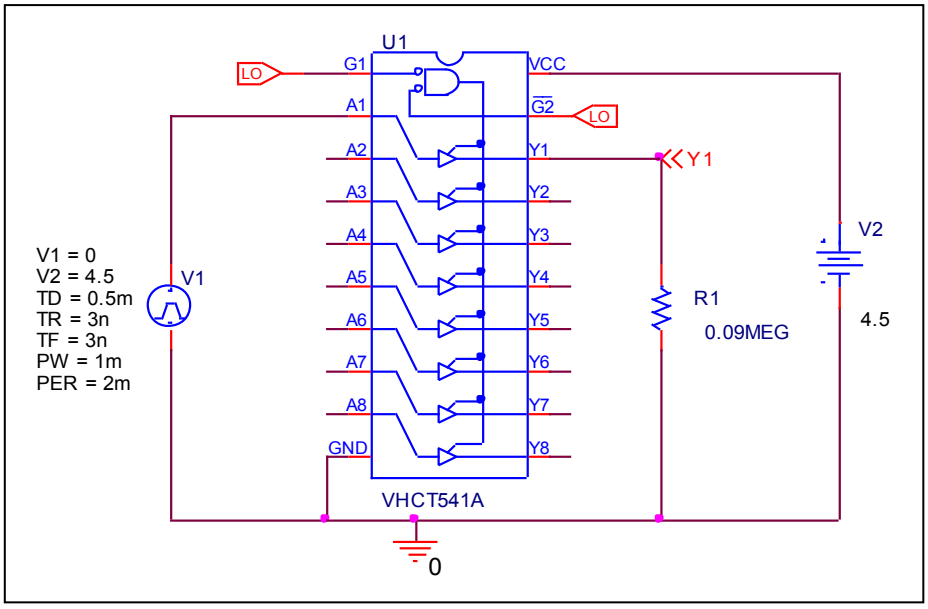
V_{CC} = 5V	Measurement	Simulation	%Error
V_{IH} (V)	2	2.0002	0.010
V_{IL} (V)	0.8	0.799205	-0.099

High Level and Low Level Output Voltage

Circuit simulation result



Evaluation circuit

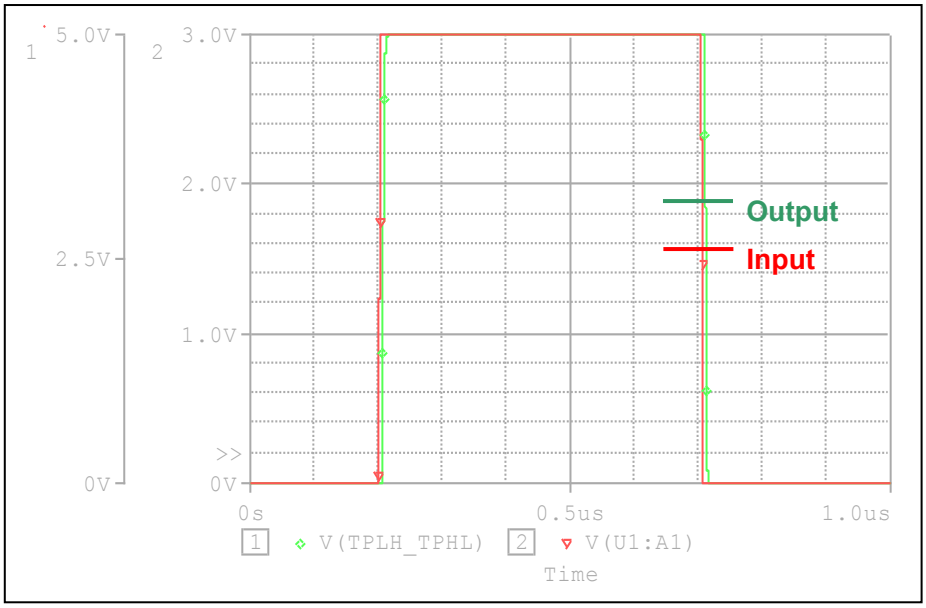


Comparison table

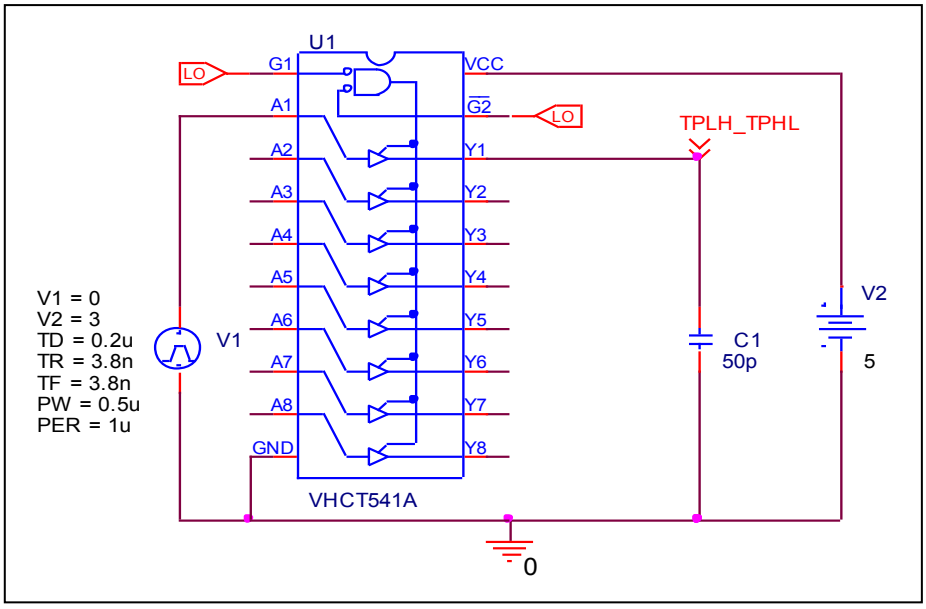
V_{CC} = 4.5V	Measurement	Simulation	%Error
V_{OH} (V)	4.5	4.4986	-0.031
V_{OL} (V)	0	0	0

Propagation Delay Time

Circuit simulation result



Evaluation circuit

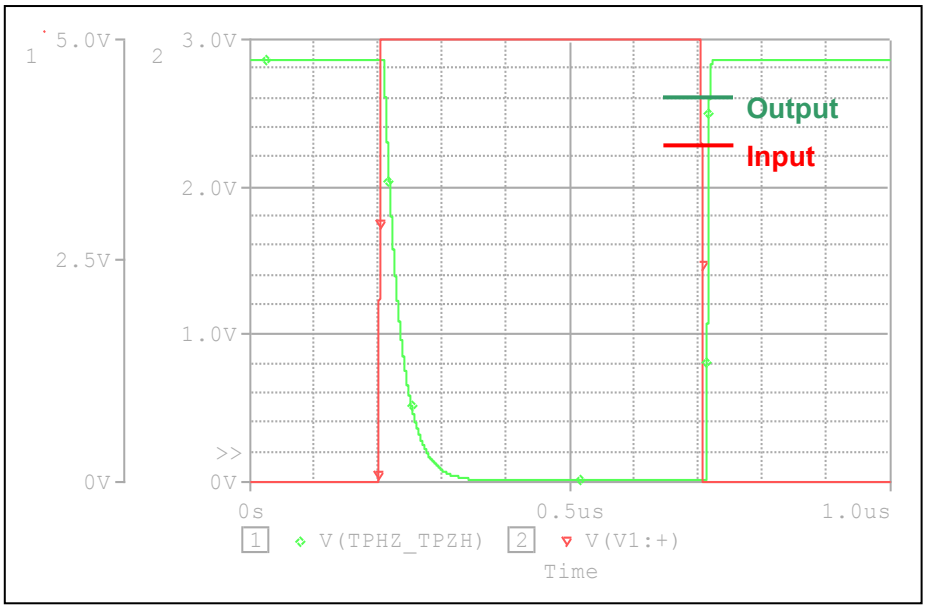


Comparison table **C_L = 50 pF**

V_{CC} = 5 V, $t_r = t_f$ = 3 ns	Measurement	Simulation	%Error
t_{pLH} (ns)	5.5	5.5761	1.384
t_{pHL} (ns)	5.5	5.5796	1.447

Output enable time, high impedance (off) to high output (t_{PZH})
Output disable time, high to high impedance (off) output (t_{PHZ})

Circuit simulation result



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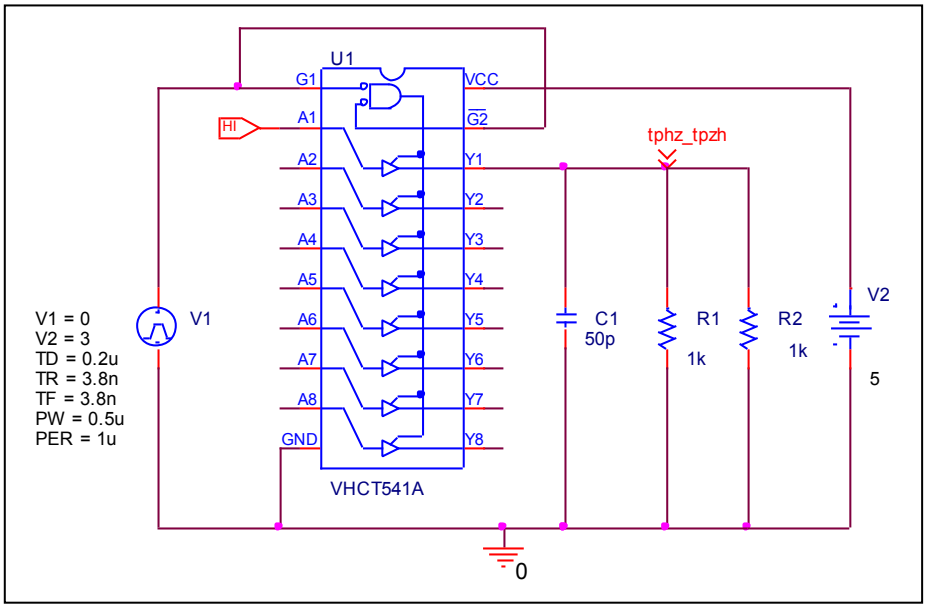
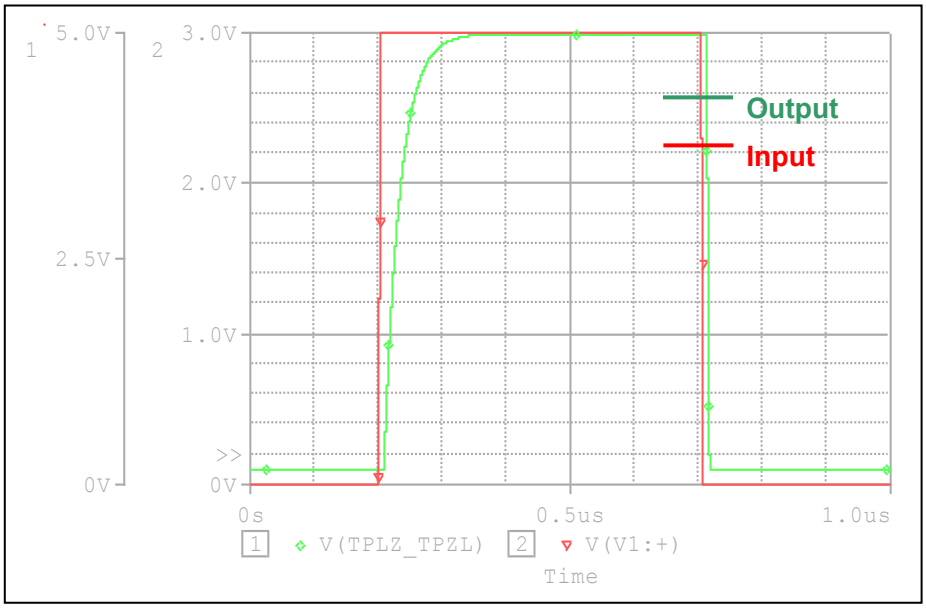


Comparison table $C_L = 50$ pF, $R_L = 1$ KΩ

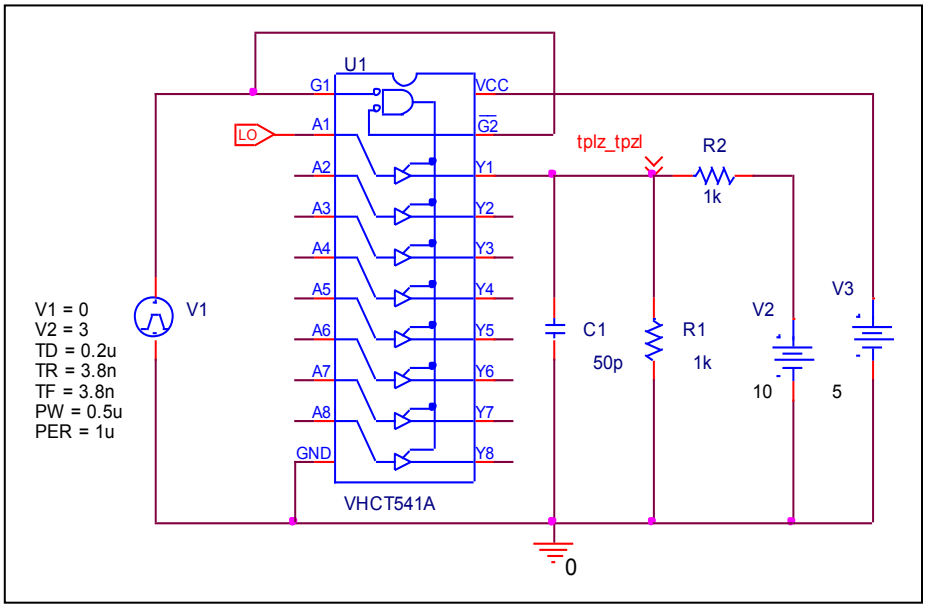
$V_{CC} = 5$ V, $t_r = t_f = 3$ ns	Measurement	Simulation	%Error
t_{PHZ} (ns)	9.4	9.4226	0.240
t_{pZH} (ns)	8.8	8.8452	0.514

Output enable time, high impedance (off) to low output (t_{PZL})
Output disable time, low to high impedance (off) output (t_{PLZ})

Circuit simulation result



Evaluation circuit



Comparison table C_L = 50 pF, R_L = 1 KΩ

V_{CC} = 5 V, t_r = t_f = 3 ns	Measurement	Simulation	%Error
t_{PLZ} (ns)	9.4	9.4062	0.066
t_{pZL} (ns)	8.8	8.8674	0.766