Device Modeling Report

COMPONENTS: Zener Diode
PART NUMBER: DF2S6.8UFS
MANUFACTURER: TOSHIBA

Bee Technologies Inc.

SPICE MODEL

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*PART NUMBER: DF2S6.8UFS
*MANUFACTURER: TOSHIBA
*REMARK: STANDARD MODEL
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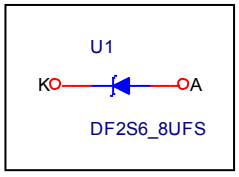
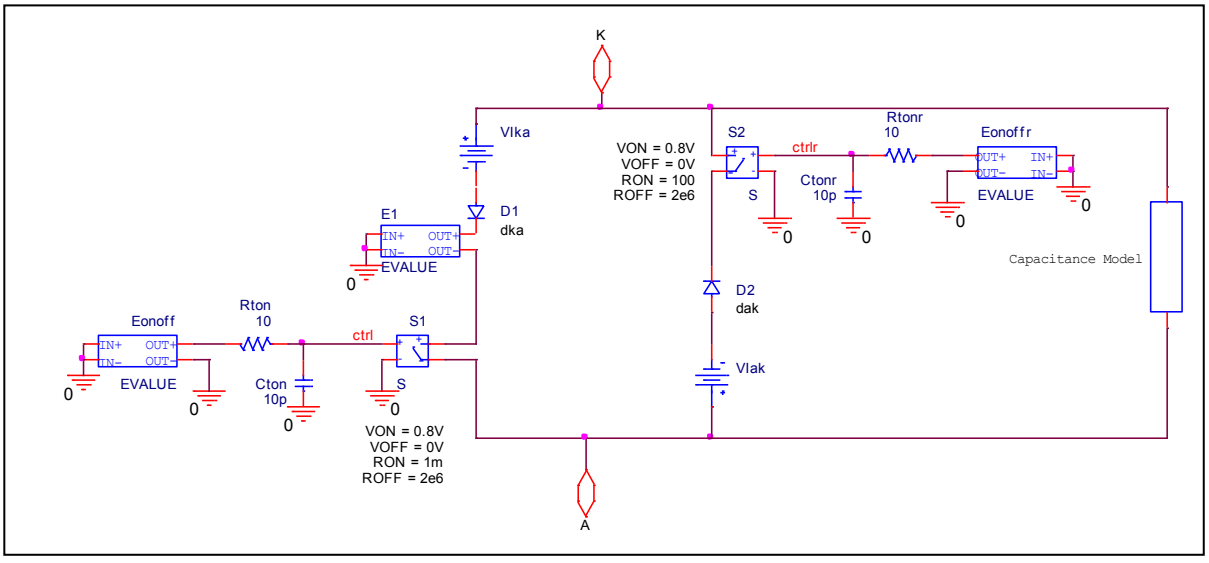
.SUBCKT DF2S6_8UFS    A K
V_Vlak              A N60967 24.9Vdc
D_D2              N60967 N60787 dak
X_S2       CTRLR 0 K N60787 SCHEMATIC1_S2
D_D3              A N605731 dc
E_E1              N606431 N60703 VALUE
{ IF(I(V_Vlka)<1u,I(V_Vlka),I(V_Vlka)*(-50)) }
D_D4              K N605731 dc
R_Rton              CTRL N61147    10
R_Rtonr              CTRLR N60917    10
C_Cton              CTRL 0    10p
V_Vlka              K N606211 6.57Vdc
C_Ctonr              CTRLR 0    10p
D_D1              N606211 N606431 dka
E_Eonoff              N61147 0 VALUE { IF(I(V_Vlka)>2.0uA,6.8,0) }
E_Eonoffr              N60917 0 VALUE { IF(I(V_Vlak)>0.5uA,5,0) }
X_S1       CTRL 0 N60703 A SCHEMATIC1_S1
.model dak d (N=0.001 Cjo=0.03pF Rs=100m)
.model dka d (N=0.001 Cjo=0.03pF Rs=100m)
.model dc d (N=0.001 CJO=1.5954E-12 M=.10138 VJ=1.5008)
.ENDS
*$
.subckt SCHEMATIC1_S2 1 2 3 4
S_S2              3 4 1 2 _S2
RS_S2              1 2 1G
.MODEL              _S2 VSWITCH Roff=2e6 Ron=100 Voff=0V Von=0.8V
.ends SCHEMATIC1_S2
*$
.subckt SCHEMATIC1_S1 1 2 3 4
S_S1              3 4 1 2 _S1
RS_S1              1 2 1G
.MODEL              _S1 VSWITCH Roff=2e6 Ron=1m Voff=0V Von=0.8V
.ends SCHEMATIC1_S1
*$
```

Circuit Configuration



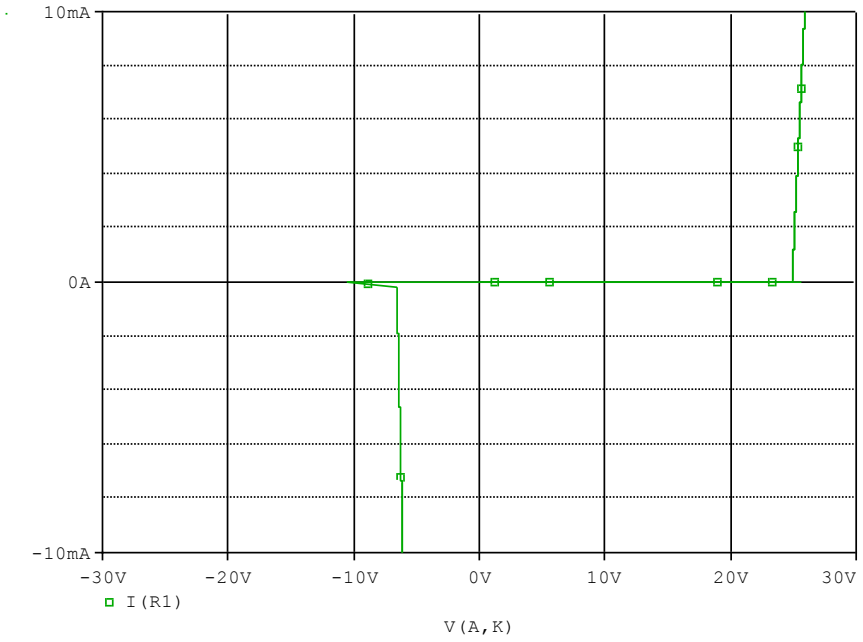
Equivalent circuit



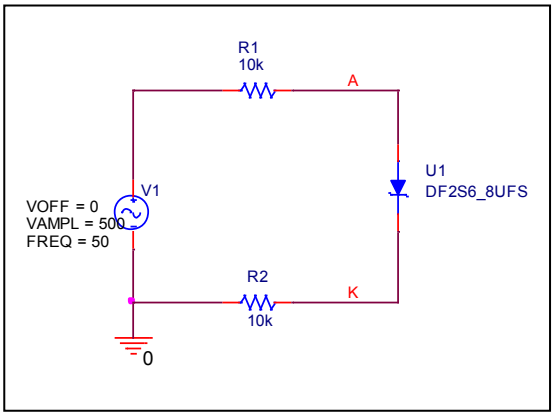
PSpice model parameter	Model description
IS	Saturation Current
N	Emission Coefficient
RS	Series Resistance
CJO	Zero-bias Junction Capacitance
M	Junction Grading Coefficient
VJ	Junction Potential
ISR	Recombination Current Saturation Value
TT	Transit Time

Forward-Reverse Voltage Characteristic

Circuit Simulation Result



Evaluation Circuit



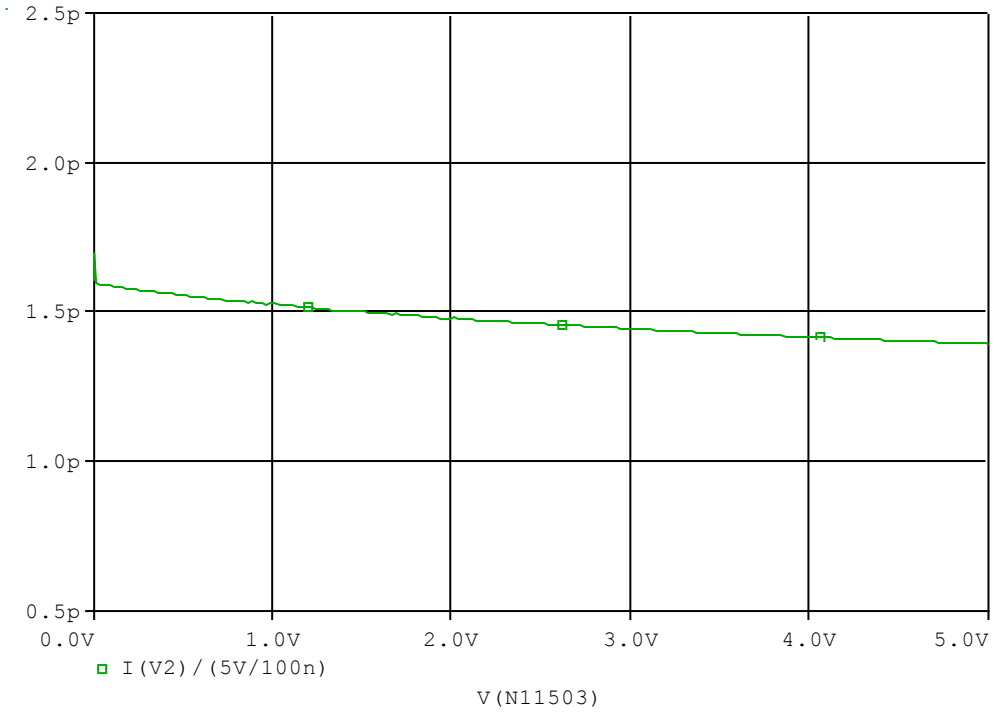
Compare Measurement vs. Simulation

Condition: I_R=1mA,I_F=1mA

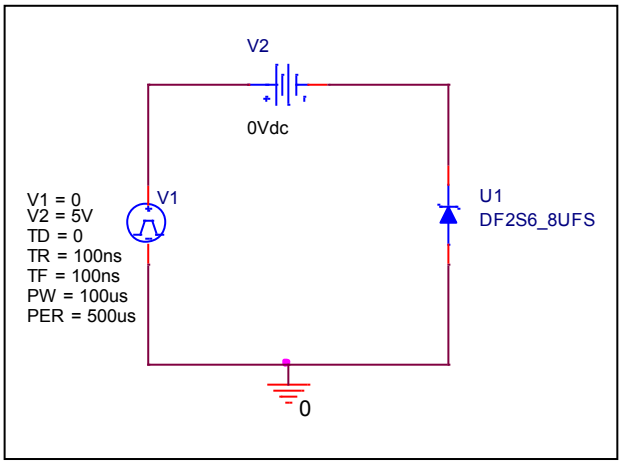
		Measurement	Simulation	%Error
V_R	V	6.800	6.521	-4.11
V_F	V	25.000	25.001	0.00

Capacitance Characteristic

Circuit Simulation Result

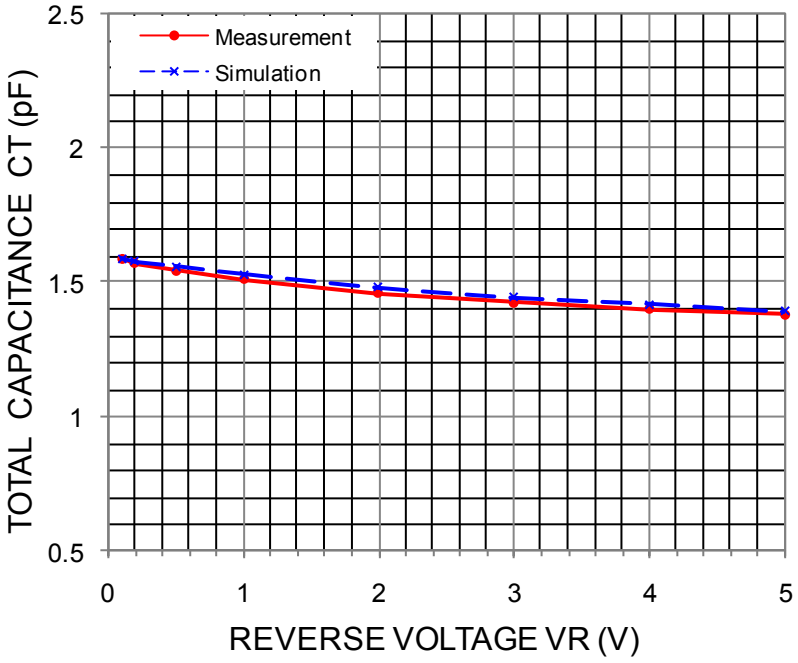


Evaluation Circuit



Comparison Graph

Circuit Simulation Result



Simulation Result

V_R (V)	C_T (pF)		%Error
	Measurement	Simulation	
0.1	1.590	1.587	-0.19
0.2	1.570	1.578	0.52
0.5	1.545	1.558	0.83
1	1.510	1.527	1.13
2	1.460	1.480	1.36
3	1.425	1.445	1.38
4	1.400	1.416	1.16
5	1.380	1.393	0.93