



# Intel Cyclone 10 LP FPGA Evaluation Kit User Guide

**UG-20082**  
**2017.08.23**



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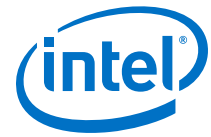
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## 1 Overview

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The Intel® Cyclone® 10 LP Evaluation Kit provides an easy-to-use platform for evaluating the performance and features of the Intel Cyclone 10 LP FPGA device.

### 1.1 General Evaluation Kit Description

The evaluation kit includes a RoHS and CE compliant Intel Cyclone 10 LP FPGA Evaluation Board with the following components.

#### Featured Devices

- Intel Cyclone 10 LP FPGA (10CL025, U256 package)
- Enpirion® EN5329QI/EN5339QI - 2A/3A PowerSoC Low Profile Synchronous Buck DC-DC Converter with Integrated Inductor
- Enpirion EP5358xUI 600 mA PowerSoC DC-DC Step-Down Converters with Integrated Inductor
- Intel XWAY PHY11G Gigabit Ethernet PHY PEF7071
- Intel MAX® 10 FPGA 10M08SAU169C8G (Embedded Intel FPGA Download Cable II and System Management)

#### Programming and Configuration

- Embedded Intel FPGA Download Cable II (JTAG)
- Optional JTAG direct via 10-pin header
- Active Serial x1 configuration from EPCQ flash

#### Memory Devices

- 128 Mb 8-bit HyperRAM with HBMC (Hyperbus Memory Controller) IP provided by Synaptic Labs
- 64 Mb EPCQ Flash

#### Communication Ports

- One Gigabit Ethernet (GbE) RJ-45 port
- One 2x20 GPIO Expansion Header
- One Arduino UNO R3 type connectors
- One 12-pin Digilent Pmod compatible connector

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### Clock Circuits

- Silicon Labs Si510 50 MHz crystal oscillator
- Silicon Labs Si5351 clock generator with programmable frequency GUI

### Power Supply

- USB Y-cable (USB Type-A to mini Type-B) for both on-board Intel FPGA Download Cable II and 5V power supply from USB port
- Supplemental 5V DC power adaptor option (5V power adaptor and cord are not included in the kit)

### Intel Quartus® Prime Standard Edition / Lite Edition

Intel Quartus® Prime Standard Edition / Lite Edition software can be downloaded from the Download Center at the Intel FPGA website.

### Related Links

[Intel FPGA Download Center](#)

## 1.2 Recommended Operating Conditions

- Recommended ambient operating temperature range: 0C to 45C
- Maximum VCCINT current: 0.6 A
- Maximum board power consumption: 3 A @ 5 V when powered by AC/DC adaptor

## 1.3 Handling the Board

When handling the board, it is important to observe static discharge precautions.

**Caution:** Without proper anti-static handling, the board could be damaged. Use anti-static handling precautions when touching the board.

**Caution:** This evaluation kit should not be operated in a Vibration environment.



## 2 Getting Started

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### 2.1 Installing Quartus Prime Software

The Intel Quartus Prime design software is a multiplatform design environment that easily adapts to your specific needs in all phases of FPGA, CPLD, and SoC designs. The Intel Quartus Prime software delivers the highest performance and productivity for Intel FPGAs, CPLDs, and SoCs.

Design software must enable dramatically increased design productivity in order to take advantage of devices with multi-million logic elements with increased capabilities that provide designers with an ideal platform to meet next-generation design opportunities.

The new Intel Quartus Prime Design Suite® design software includes everything needed to design for Intel FPGAs, SoCs and CPLDs from design entry and synthesis to optimization, verification and simulation. The Intel Quartus Prime Design Suite software includes an additional Spectra-Q® engine that is optimized for Intel Stratix® 10 and future devices. The Spectra-Q engine enables new levels of design productivity for next generation programmable devices with a set of faster and more scalable algorithms, a hierarchical database infrastructure and a unified compiler technology.

#### Intel Quartus Prime Software

The Intel Quartus Prime Design Suite software is available in three editions based on specific design requirements: Pro, Standard, and Lite Edition.

The Intel Quartus Prime Pro Edition is optimized to support the advanced features in Intel's next generation FPGAs and SoCs and requires a paid license.

Intel Quartus Prime Standard Edition includes the most extensive support for Intel's latest device families and requires paid license.

Intel Quartus Prime Lite Edition provides an ideal entry point to Intel's high-volume device families and is available as a free download with no license file required.

Included in the Intel Quartus Prime Pro Edition are the Intel Quartus Prime software, Nios® II EDS and the MegaCore IP Library.

To install Intel's development tools, download the Intel Quartus Prime Pro Edition software from the Quartus Prime Pro Edition page from the [Download Center](#) of Intel's website.



### Related Links

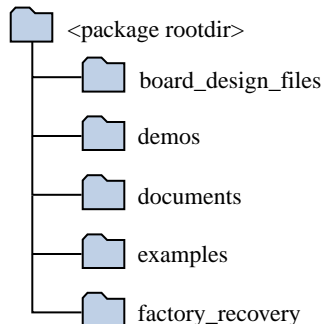
[Intel FPGA Download Center](#)

## 2.2 Development Board Package

To download the Intel Cyclone 10 LP FPGA Evaluation Board package, perform the following steps:

1. Download the evaluation kit package from the Intel Cyclone 10 LP FPGA Evaluation Kit link on the Intel website.
2. Unzip the Intel Cyclone 10 LP FPGA Evaluation Kit package contents to your machine's local hard drive.
3. The package creates the directory structure shown in the figure below.

**Figure 1. Evaluation Kit Directory Structure**



The table below lists the file directory names and a description of their contents

**Table 1. Directory Structure**

File Directory Name	Description of Directory Contents
board_design_files	Contains schematics, layout, assembly and bill of material board design files. Use these files as a starting point for a new prototype board design
demos	Contains demonstration applications when available
documents	Contains the evaluation kit documentation
examples	Contains the sample design files for the evaluation kit
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

### Related Links

[Intel Cyclone 10 LP FPGA Evaluation Kit](#)

## 2.3 Installing Intel FPGA Download Cable Driver

The Intel Cyclone 10 LP FPGA Evaluation Kit includes embedded Intel FPGA Download Cable circuits for FPGA programming. However, for the host computer and board to communicate, you must install the Intel FPGA Download Cable driver on the host computer.



Installation instructions for the Intel FPGA Download Cable driver for your operating system are available on the Intel website.

On the Intel website, navigate to the [Cable and Adapter Drivers Information](#) link to locate the table entry for your configuration and click the link to access the instructions.





## 3 Development Board Setup

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The instructions in this chapter explain how to setup the Intel Cyclone 10 LP FPGA Evaluation Kit.

### 3.1 Setting up the Evaluation Board

**To prepare and apply power to the board, perform the following steps:**

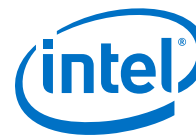
1. The Intel Cyclone 10 LP evaluation kit ships with its board switches pre-configured to support the design examples in this kit. If you suspect your board might not be correctly configured with the default settings, follow the instructions on the [Default Switch Settings](#) on page 9 to return the board to its factory settings before proceeding.
2. Connect either USB cable to J17 or 5V DC adaptor to J12 to power up the board.
3. After the board is powered up correctly, status LED illuminates. If you are using factory image stored in EPCQ Flash, the Blue LED will be ON to indicate power is good. Yellow LED D5 will be ON to indicate the FPGA is configured successfully. User LEDs D6, D7, D8, D9 will be blinking which is set in factory image.

### 3.2 Default Switch Settings

This section shows the factory DIP switch settings for the Intel Cyclone 10 LP FPGA evaluation kit.

**Table 2. DIP Switch Settings**

Switch	Board Label	Default Position	Function
SW1.4	BYPASS	OPEN/OFF/1	Virtual JTAG TAP Enable
SW1.3	DIP0	OPEN/OFF/1	Switch 0
SW1.2	DIP1	OPEN/OFF/1	Switch 1
SW1.1	DIP2	OPEN/OFF/1	Switch 2



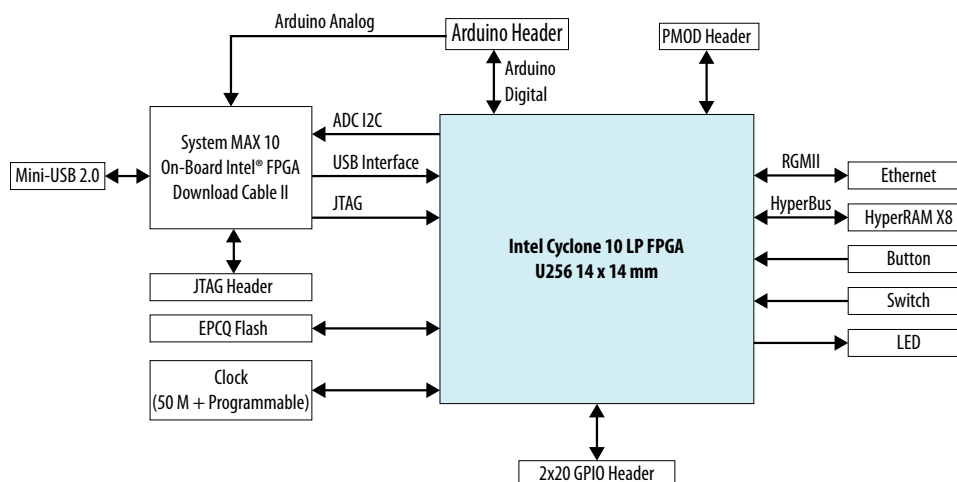
## 4 Evaluation Board Components

This chapter introduces all important components on the evaluation board.

### 4.1 Board Overview

This topic provides a high-level list of major components on the Intel Cyclone 10 LP FPGA evaluation board.

**Figure 2. Intel Cyclone 10 LP FPGA Evaluation Kit Block Diagram**



**Table 3. Board Components**

Board Reference	Type	Description
<b>Featured Devices</b>		
U1	FPGA	Intel Cyclone 10 LP FPGA 10CL025YU25617G, 25k LEs, U256 package
U3	FPGA	Intel MAX 10 10M08SAU169C8G for On-board Intel FPGA Download Cable II and System Management
U25	Power Regulator	Enpirion EN5329QI - 2A PowerSoC Low Profile Synchronous Buck DC-DC Converter with Integrated Inductor
U23	Power Regulator	Enpirion EN5339QI - 3A PowerSoC Low Profile Synchronous Buck DC-DC Converter with Integrated Inductor
<i>continued...</i>		

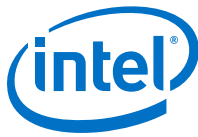
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Board Reference	Type	Description
U26, U27	Power Regulator	Enpirion EP5358HUI, 600 mA PowerSoC DC-DC step-down converters with integrated inductor.
U14	Gigabit Ethernet PHY	Intel XWAY PHY11G Single Port Gigabit Ethernet PHY (10/100/1000 Mbps) PEF7071
<b>Configuration and Setup Elements</b>		
J17	Embedded Intel FPGA Download Cable II	Type-B Mini USB Connector for programming and debugging the FPGA
J2	10-pin header	Optional JTAG direct via 10-pin header for external download cables
SW1.4	Virtual JTAG TAP Bypass Switch	ON/Closed/0: Bypass Virtual JTAG TAP OFF/Open/1: Enable Virtual JTAG TAP
S1	FPGA nCONFIG push button	Press this button to trigger reconfiguration
S2	FPGA reset push button	Press this button to reset all registers in the FPGA
<b>Status Elements</b>		
D4	Power LED (Blue)	Power Good LED (Detects VCC_3 . 3V and VCC_1 . 2V) ON: Detected Power is Good OFF: Detected Power is Bad
D5	Configuration LED (Yellow)	Config done status Indicator ON: FPGA configured successfully OFF: FPGA not configured
D10	Ethernet LED0 (Green)	Ethernet link status indicator ON: Link-up OFF: Link-down Blink: Link-up with traffic
D11	Ethernet LED1 (Green)	Ethernet link speed indicator ON: 100 Mbps OFF: 10/1000 Mbps or Link-down
D12	Ethernet LED2 (Green)	Ethernet link speed indicator ON: 1000 Mbps OFF: 10/1000 Mbps or Link-down
<b>Clock Circuits</b>		
U20	50 MHz Oscillator	50 MHz crystal oscillator for general purpose logic of Intel Cyclone 10 LP FPGA and Intel MAX 10 FPGA devices
U31	Programmable clock generator	Three channel Programmable clock generator. Default frequencies are 125 MHz, 100 MHz and 50 MHz
<b>General User Input/Output</b>		
S3, S4, S5, S6	General user push buttons	Four user push buttons. Driven low when pressed.
D6, D7, D8, D9	User LEDs	Four user LEDs. Illuminates when driven low.
<b>continued...</b>		



Board Reference	Type	Description
SW1.1 - SW1.3	User DIP Switches	3-bit user DIP switches
<b>Memory Devices</b>		
U13	HyperRAM Memory	128 Mb, x8 HyperRAM with 1.8V I/O
U2	EPCQ Flash	64 Mb
<b>I/O and Expansion Ports</b>		
J8	One Diligent PMOD Connector	12-pin interface with 8 I/O signal pins used to connect low frequency, low I/O peripheral modules
J4, J5, J6, J7, J18	Arduino UNO R3 type connector	Arduino UNO R3 type connectors with 3.3V digital I/O and six analog input channels
J10	2x20 GPIO Expansion Header	2x20 GPIO Expansion Header with 36 I/O
J16	One Gigabit Ethernet Port	RJ-45 connector provides a 10/100/1000 Ethernet connection via a Intel PEF7071 PHY and the FPGA-based Intel Triple Speed Ethernet MegaCore function in RGMII mode
<b>Power Supply</b>		
J12	DC input jack	Supplemental 5V DC power adaptor connector
J17	USB Mini-B Connector	For 5V power from USB port also used as Intel FPGA Download Cable communication port

## 4.2 Cyclone 10 FPGA Overview

The Intel Cyclone 10 LP FPGA Evaluation Kit features the Intel Cyclone 10 LP 10CL025YU256I7G FPGA device in a 256 pin FineLine BGA package.

The Intel Cyclone 10 LP FPGAs are optimized for low cost and low static power, making them ideal for high-volume and cost-sensitive applications.

**Table 4. Cyclone 10 LP FPGA**

Equivalent LEs	M9K Memory Blocks	M9K Memory Size (Kb)	18-bit x 18-bit multipliers	PLLs	Transceivers	Package Type
25K	66	594	66	4	---	256-pin UBGA (14 mm x 14 mm, 0.8 mm pitch)

### Intel Cyclone 10 LP FPGA Feature Summary

Intel Cyclone 10 LP FPGA devices provide a high density sea of programmable gates, on-board resources, and general purpose I/Os. These resources satisfies the requirements of I/O expansion and chip-to-chip interfacing. The Intel Cyclone 10 LP FPGA architecture suits smart and connected end applications across many market segments:



- Industrial and automotive
- Broadcast, wireline, and wireless
- Compute and storage
- Government, military, and aerospace
- Medical, consumer, and smart energy

**Table 5. Summary of Features for Intel Cyclone 10 LP FPGA Devices**

Feature	Description
Technology	<ul style="list-style-type: none"> <li>• Low-cost, low-power FPGA fabric</li> <li>• 1.0 V and 1.2 V core voltage options</li> <li>• Available in commercial, industrial, and automotive temperature grades</li> </ul>
Packaging	<ul style="list-style-type: none"> <li>• Several package types and footprints:               <ul style="list-style-type: none"> <li>– FineLine BGA (FBGA)</li> <li>– Enhanced Thin Quad Flat Pack (EQFP)</li> <li>– Ultra FineLine BGA (UBGA)</li> <li>– Micro FineLine BGA (MBGA)</li> </ul> </li> <li>• Multiple device densities with pin migration capability</li> <li>• RoHS6 compliance</li> </ul>
Core architecture	<ul style="list-style-type: none"> <li>• Logic elements (LEs)—four-input look-up table (LUT) and register</li> <li>• Abundant routing/metal interconnect between all LEs</li> </ul>
Internal memory blocks	<ul style="list-style-type: none"> <li>• M9K—9-kilobits (Kb) of embedded SRAM memory blocks, cascadable</li> <li>• Configurable as RAM (single-port, simple dual port, or true dual port), FIFO buffers, or ROM</li> </ul>
Embedded multiplier blocks	<ul style="list-style-type: none"> <li>• One 18 × 18 or two 9 × 9 multiplier modes, cascadable</li> <li>• Complete suite of DSP IPs for algorithmic acceleration</li> </ul>
Clock networks	<ul style="list-style-type: none"> <li>• Global clocks that drive throughout entire device, feeding all device quadrants</li> <li>• Up to 15 dedicated clock pins that can drive up to 20 global clocks</li> </ul>
Phase-locked loops (PLLs)	<ul style="list-style-type: none"> <li>• Up to four general purpose PLLs</li> <li>• Provides robust clock management and synthesis</li> </ul>
General-purpose I/Os (GPIOs)	<ul style="list-style-type: none"> <li>• Multiple I/O standards support</li> <li>• Programmable I/O features</li> <li>• True LVDS and emulated LVDS transmitters and receivers</li> <li>• On-chip termination (OCT)</li> </ul>
SEU mitigation	SEU detection during configuration and operation
Configuration	<ul style="list-style-type: none"> <li>• Active serial (AS), passive serial (PS), fast passive parallel (FPP)</li> <li>• JTAG configuration scheme</li> <li>• Configuration data decompression</li> <li>• Remote system upgrade</li> </ul>

#### Related Links

[Intel Cyclone 10 LP FPGA Device Overview](#)

### 4.3 MAX 10 System Controller Overview

The highlights of the Intel MAX 10 devices include:



- Internally stored dual configuration flash
- User flash memory
- Instant on support
- Integrated analog-to-digital converter (ADC)
- Single-chip Nios II soft core processor support

Intel MAX 10 devices are the ideal solution for system management, I/O expansion, communication control planes, industrial, automotive, and consumer applications.

**Table 6. Summary of Features for Intel MAX 10 Devices**

Feature	Description
Technology	55 nm TSMC Embedded Flash (Flash + SRAM) process technology
Packaging	<ul style="list-style-type: none"> <li>• Low cost, small form factor packages—support multiple packaging technologies and pin pitches</li> <li>• Multiple device densities with compatible package footprints for seamless migration between different device densities</li> <li>• RoHS6-compliant</li> </ul>
Core architecture	<ul style="list-style-type: none"> <li>• 4-input look-up table (LUT) and single register logic element (LE)</li> <li>• LEs arranged in logic array block (LAB)</li> <li>• Embedded RAM and user flash memory</li> <li>• Clocks and PLLs</li> <li>• Embedded multiplier blocks</li> <li>• General purpose I/Os</li> </ul>
Internal memory blocks	<ul style="list-style-type: none"> <li>• M9K—9 kilobits (Kb) memory blocks</li> <li>• Cascadable blocks to create RAM, dual port, and FIFO functions</li> </ul>
User flash memory (UFM)	<ul style="list-style-type: none"> <li>• User accessible non-volatile storage</li> <li>• High speed operating frequency</li> <li>• Large memory size</li> <li>• High data retention</li> <li>• Multiple interface option</li> </ul>
Embedded multiplier blocks	<ul style="list-style-type: none"> <li>• One 18 × 18 or two 9 × 9 multiplier modes</li> <li>• Cascadable blocks enabling creation of filters, arithmetic functions, and image processing pipelines</li> </ul>
ADC	<ul style="list-style-type: none"> <li>• 12-bit successive approximation register (SAR) type</li> <li>• Up to 16 analog inputs</li> <li>• Cumulative speed up to 1 million samples per second (MSPS)</li> <li>• Integrated temperature sensing capability</li> </ul>
Clock networks	<ul style="list-style-type: none"> <li>• Global clocks support</li> <li>• High speed frequency in clock network</li> </ul>
Internal oscillator	Built-in internal ring oscillator
PLLs	<ul style="list-style-type: none"> <li>• Analog-based</li> <li>• Low jitter</li> <li>• High precision clock synthesis</li> <li>• Clock delay compensation</li> <li>• Zero delay buffering</li> <li>• Multiple output taps</li> </ul>
<i>continued...</i>	



Feature	Description
General-purpose I/Os (GPIOs)	<ul style="list-style-type: none"> <li>Multiple I/O standards support</li> <li>On-chip termination (OCT)</li> <li>Up to 830 megabits per second (Mbps) LVDS receiver, 800 Mbps LVDS transmitter</li> </ul>
External memory interface (EMIF)	Supports up to 600 Mbps external memory interfaces: <ul style="list-style-type: none"> <li>DDR3, DDR3L, DDR2, LPDDR2</li> <li>SRAM (Hardware support only)</li> </ul> <i>Note:</i> For 600 Mbps performance, –6 device speed grade is required. Performance varies according to device grade (commercial, industrial, or automotive) and device speed grade (–6 or –7). Refer to the <a href="#">MAX 10 Device Data Sheet</a> or <a href="#">External Memory Interface Spec Estimator</a> for more details.
Configuration	<ul style="list-style-type: none"> <li>Internal configuration</li> <li>JTAG</li> <li>Advanced Encryption Standard (AES) 128-bit encryption and compression options</li> <li>Flash memory data retention of 20 years at 85 °C</li> </ul>
Flexible power supply schemes	<ul style="list-style-type: none"> <li>Single- and dual-supply device options</li> <li>Dynamically controlled input buffer power down</li> <li>Sleep mode for dynamic power reduction</li> </ul>

### Related Links

[MAX 10 FPGA Device Overview](#)

## 4.4 FPGA Configuration

The Intel Cyclone 10 LP FPGA Evaluation Kit supports two configuration methods:

- Configuration by downloading a .sof file to the FPGA. Any power cycling of the FPGA or reconfiguration will power up the FPGA to a blank state.
- Programming of the board EPCQ flash via .jic file. Any power cycling of the FPGA or reconfiguration will lead to reconfigure from EPCQ flash with AS mode.

You can use two different Intel FPGA Download Cable hardware components to program the .sof or .jic files:

- Embedded Intel FPGA Download Cable II type-B mini-USB connector (J17)
- JTAG header (J2). Use an external Intel FPGA Download Cable, Intel FPGA Download Cable II or Ethernet Blaster download cable. The external download cable connects to the board through the JTAG header (J2).

### 4.4.1 Using the Quartus Prime Programmer

You can use the Intel Quartus Prime Programmer to configure the FPGA with a .sof.

#### Before configuring the FPGA

- Ensure that the Intel Quartus Prime Programmer and the Intel FPGA Download Cable driver are installed on the host computer.
- The USB cable is connected to the kit.
- Power to the board is on, and no other applications that use the JTAG chain are running.



### To configure the Intel Cyclone 10 LP FPGA

1. Start the Intel Quartus Prime Programmer.
2. Click Add File and select the path to the desired .sof.
3. Turn on the Program/Configure option for the added file.
4. Click Start to download the selected file to the FPGA. Configuration is complete when the progress bar reaches 100%.

## 4.4.2 Program on-board EPCQ flash

The FPGA is set to Active Serial configuration mode by default. You can use the Intel Quartus Prime Programmer to program a .jic file to EPCQ flash.

### Program the EPCQ Flash

1. Ensure the DIP switch SW1.4 is ON to bypass virtual JTAG TAP and then power on the board.
2. Open Intel Quartus Prime Programmer and ensure that JTAG is detected under Hardware Setup.
3. Select **Auto Detect** and choose the correct FPGA device.
4. Right-click on the FPGA device and select **Edit ► Attach Flash Device**.
5. Select **ASC Devices ► EPCQ64** in the pop-up window and then click **OK**.
6. Right-click on the EPCQ64 device and select **Edit ► Change File**. Next, choose the generated .jic file you want to program.
7. Select the **Program/Configure** checkboxes for FPGA and EPCQ devices. Click **Start** to begin programming the FPGA.
8. EPCQ is programmed successfully when the progress bar reaches 100% and displays **Successful**.

**Attention:** Please set SW1.4 to OFF if your following operations need to enable virtual JTAG TAP.

## 4.4.3 Active Serial Configuration

1. After all steps in the previous section are completed, press push button S1 C10\_NCONFIG or power cycle the board.
2. Yellow LED D5 will turn ON. This indicates that the FPGA is configured with image in EPCQ Flash under Active Serial Mode.

## 4.5 Status Elements

Table 7. LEDs

Board Reference	Schematic Signal Name	Color	Description
D4	PWR_GD_LED	Blue	Power Good LED (Detects VCC_3.3V and VCC_1.2V) ON: Detected Power is good

*continued...*





Board Reference	Schematic Signal Name	Color	Description
			OFF: Detected Power is bad
D5	SYS_CONF_DONE	Yellow	Configuration Done Status Indicator ON: FPGA configured successfully OFF: FPGA not configured
D10	ENET_LED0	Green	Ethernet link status indicator ON: Link-up OFF: Link-down Blink: Link-up with traffic
D11	ENET_LED1	Green	Ethernet link speed indicator ON: 100 Mbps OFF: 10/1000 Mbps or Link-down
D12	ENET_LED2	Green	Ethernet link speed indicator ON: 1000 Mbps OFF: 10/100 Mbps or Link-down

## 4.6 Setup Elements

**Table 8. DIP Switches**

Board Reference	Schematic Signal Name	Description
SW1.4	VTAP_BYPASSn	Pull low to disable Virtual JTAG TAP in device chain

**Table 9. Push Buttons**

Board Reference	Schematic Signal Name	Description
S1	C10_nCONFIG	Press this push button to reconfigure Intel Cyclone 10 LP FPGA device
S2	C10_RESETh	Press to do device-wide reset, connect to Intel Cyclone 10 LP FPGA DEV_CLRn

## 4.7 General User Input/Output

**Table 10. DIP Switches**

Board Reference	Schematic Signal Name	Description
SW1.3	USER_DIP0	User-defined Switch0
SW1.2	USER_DIP1	User-defined Switch1
SW1.1	USER_DIP2	User-defined Switch2

**Table 11. Push Buttons**

Board Reference	Schematic Signal Name	Description
S3	USER_PB0	User-defined PB0
S4	USER_PB1	User-defined PB1
S5	USER_PB2	User-defined PB2
S6	USER_PB3	User-defined PB3

**Table 12. LEDs**

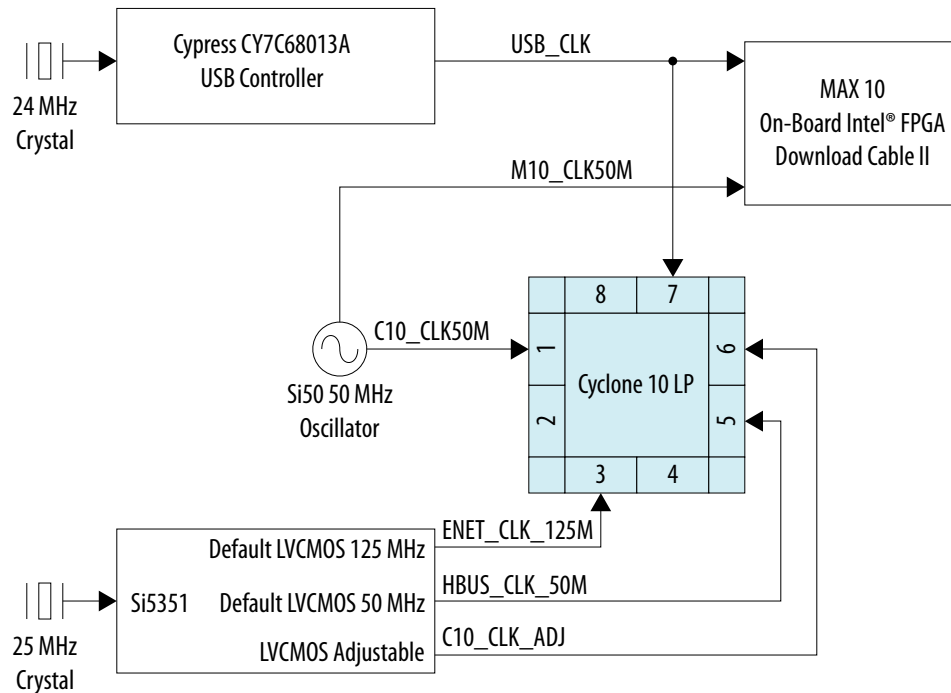
Board Reference	Schematic Signal Name	Color	Description
D6	USER_LED0	Green	User-defined LED0 , active low
D7	USER_LED1	Green	User-defined LED1 , active low
D8	USER_LED2	Green	User-defined LED2 , active low
D9	USER_LED3	Green	User-defined LED3 , active low

### 4.8 Clocks

Si5351 is a programmable clock generator that users can use Intel Clock GUI to program output frequency. It is controlled from Intel MAX 10 with I<sup>2</sup>C bus.

The clock tree is shown in the figure below.

**Figure 3. Cyclone 10 LP FPGA Clock Tree**





## 4.9 Connectors and Interfaces

This section describes the evaluation kit's communication ports and interface cards related to the Intel Cyclone 10 LP FPGA Evaluation Kit.

### 4.9.1 Gigabit Ethernet PHY

The evaluation kit supports single port Ethernet via Intel XWAY PHY11G PEF7071 Ethernet PHY chips. This physical layer device has general applications using RJ-45 connector.

**Figure 4. MAC-to-PHY connection by PEF7071 device**

Specific to the Intel Cyclone 10 LP FPGA evaluation kit, the MAC-to-PHY interface is configured to a RGMII interface connection with MDIO interface as management.

**Table 13. Ethernet PHY Table**

Schematic Signal Name	Schematic Shared Bus Signal Name	FPGA Pin Number	I/O Standard	Direction @ FPGA	Description
ENET_RG_TXCLK	C10_RG_TXCLK	D3	3.3V	Out	RGMII TX clock
ENET_RG_TXD0	C10_RG_TXD0	E6	3.3V	Out	RGMII TX data 0
ENET_RG_TXD1	C10_RG_TXD1	A3	3.3V	Out	RGMII TX data 1
ENET_RG_TXD2	C10_RG_TXD2	B3	3.3V	Out	RGMII TX data 2
ENET_RG_TXD3	C10_RG_TXD3	A2	3.3V	Out	RGMII TX data 3
ENET_RG_TXCTL	C10_RG_TXCTL	D6	3.3V	Out	RGMII TX control
ENET_RG_RXCLK	RG_RXCLK	B8	3.3V	In	RGMII RX Clock
ENET_RG_RXD0	RG_RXD0	A7	3.3V	In	RGMII RX data 0
ENET_RG_RXD1	RG_RXD1	B7	3.3V	In	RGMII RX data 1
ENET_RG_RXD2	RG_RXD2	A6	3.3V	In	RGMII RX data 2
ENET_RG_RXD3	RG_RXD3	B6	3.3V	In	RGMII data 3
ENET_RG_RXCTL	RG_RXCTL	A5	3.3V	In	RGMII RX Control
ENET_INT		B5	3.3V	In	Management Interrupt
ENET_MDC		B4	3.3V	Out	MDIO clock
ENET_MDIO		A4	3.3V	I/O	MDIO data
ENET_RSTn		C6	3.3V	Out	Device Reset
ENET_XTAL1					
ENET_XTAL2					
ENET_LED0			3.3V	Out	Status LED0, Green
ENET_LED1			3.3V	Out	Status LED1, Green

*continued...*



Schematic Signal Name	Schematic Shared Bus Signal Name	FPGA Pin Number	I/O Standard	Direction @ FPGA	Description
ENET_LED2			3.3V	Out	Status LED2, Green
TPIAP					Twisted-Pair A, positive
TPIAN					Twisted-Pair A, negative
TPIBP					Twisted-Pair B, positive
TPIBN					Twisted-Pair B, negative
TPICP					Twisted-Pair C, positive
TPICN					Twisted-Pair C, negative
TPIDP					Twisted-Pair D, positive
TPIDN					Twisted-Pair D, negative

**Note:** 10/100/1000 Ethernet will not be supported in the current version until Intel Quartus Prime v17.1 software release.

### 4.9.2 2x20 GPIO Expansion Header

The Intel Cyclone 10 LP FPGA evaluation kit provides one 40-pin expansion GPIO header with up to 36 GPIO signals. This 2x20 GPIO Header is compatible with some Terasic 2x20 GPIO cards.

There are also +5V (VCC\_5V\_GPIO) and +3.3V(VCC\_3.3V) and two GND pins on 2x20 GPIO expansion header. All GPIO signals GPIO[0:35] are 3.3V single-ended LVCMOS/LVTTL signals who are connected to Intel Cyclone 10 LP FPGA directly.

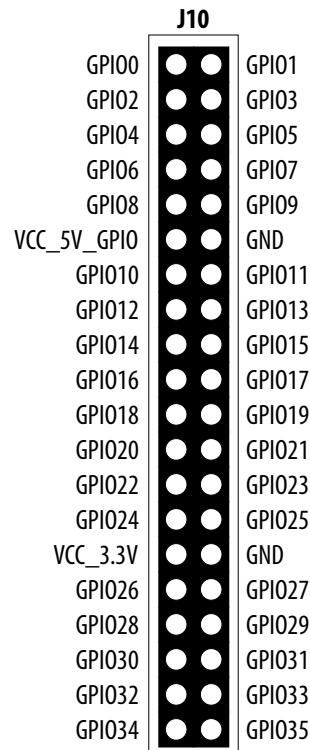
**Table 14. 2X20 GPIO Header Signals**

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard	Direction @ FPGA	Description
J10.1	GPIO0	L13	3.3V	IO	GPIO Signal 0
J10.2	GPIO1	L16	3.3V	IO	GPIO Signal 1
J10.3	GPIO2	L15	3.3V	IO	GPIO Signal 2
J10.4	GPIO3	K16	3.3V	IO	GPIO Signal 3
J10.5	GPIO4	P16	3.3V	IO	GPIO Signal 4
J10.6	GPIO5	R16	3.3V	IO	GPIO Signal 5
J10.7	GPIO6	N16	3.3V	IO	GPIO Signal 6
J10.8	GPIO7	N15	3.3V	IO	GPIO Signal 7
J10.9	GPIO8	N14	3.3V	IO	GPIO Signal 8
<i>continued...</i>					



Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard	Direction @ FPGA	Description
J10.10	GPIO9	P15	3.3V	IO	GPIO Signal 9
J10.11	VCC_5V_GPIO	---	---	---	Short to VCC_5V
J10.12	GND	---	---	---	Ground
J10.13	GPIO10	N8	3.3V	IO	GPIO Signal 10
J10.14	GPIO11	P8	3.3V	IO	GPIO Signal 11
J10.15	GPIO12	M8	3.3V	IO	GPIO Signal 12
J10.16	GPIO13	L8	3.3V	IO	GPIO Signal 13
J10.17	GPIO14	R7	3.3V	IO	GPIO Signal 14
J10.18	GPIO15	T7	3.3V	IO	GPIO Signal 15
J10.19	GPIO16	L7	3.3V	IO	GPIO Signal 16
J10.20	GPIO17	M7	3.3V	IO	GPIO Signal 17
J10.21	GPIO18	R6	3.3V	IO	GPIO Signal 18
J10.22	GPIO19	T6	3.3V	IO	GPIO Signal 19
J10.23	GPIO20	T2	3.3V	IO	GPIO Signal 20
J10.24	GPIO21	M6	3.3V	IO	GPIO Signal 21
J10.25	GPIO22	R5	3.3V	IO	GPIO Signal 22
J10.26	GPIO23	T5	3.3V	IO	GPIO Signal 23
J10.27	GPIO24	N5	3.3V	IO	GPIO Signal 24
J10.28	GPIO25	N6	3.3V	IO	GPIO Signal 25
J10.29	VCC_3.3V	---	---	---	VCC_3.3V
J10.30	GND	---	---	---	Ground
J10.31	GPIO26	R4	3.3V	IO	GPIO Signal 26
J10.32	GPIO27	T4	3.3V	IO	GPIO Signal 27
J10.33	GPIO28	N3	3.3V	IO	GPIO Signal 28
J10.34	GPIO29	P3	3.3V	IO	GPIO Signal 29
J10.35	GPIO30	R3	3.3V	IO	GPIO Signal 30
J10.36	GPIO31	T3	3.3V	IO	GPIO Signal 31
J10.37	GPIO32	P6	3.3V	IO	GPIO Signal 32
J10.38	GPIO33	P2	3.3V	IO	GPIO Signal 33
J10.39	GPIO34	P1	3.3V	IO	GPIO Signal 34
J10.40	GPIO35	R1	3.3V	IO	GPIO Signal 35

Figure 5. GPIO



The maximum power output capability is shown in the table below. When using 2x20 GPIO Header, USB may not provide sufficient power. Hence, use an external adaptor connector (J12) to power up the board.

Table 15. 2X20 GPIO Header Power Output Capability

PowerRail	Output Pin Location	Max Current	Note
VCC_5V_GPIO	J10.11	0.5 A	VCC_5V output capability to card (depends on the power adaptor capability)
VCC_3.3V	J10.29	0.5 A	VCC_3.3V output capability to daughter card

### 4.9.3 Arduino Connectors

The Intel Cyclone 10 LP FPGA Evaluation Kit features an Arduino UNO R3 type interface which is comprised of headers J4, J5, J6, J7, J18.

The header's location is compatible with Arduino UNO R3. This interface contains 17 digital IOs (include one Reset) and six Analog inputs.

The header's location and definition are shown in the figure below.



Figure 6. Arduino Connector

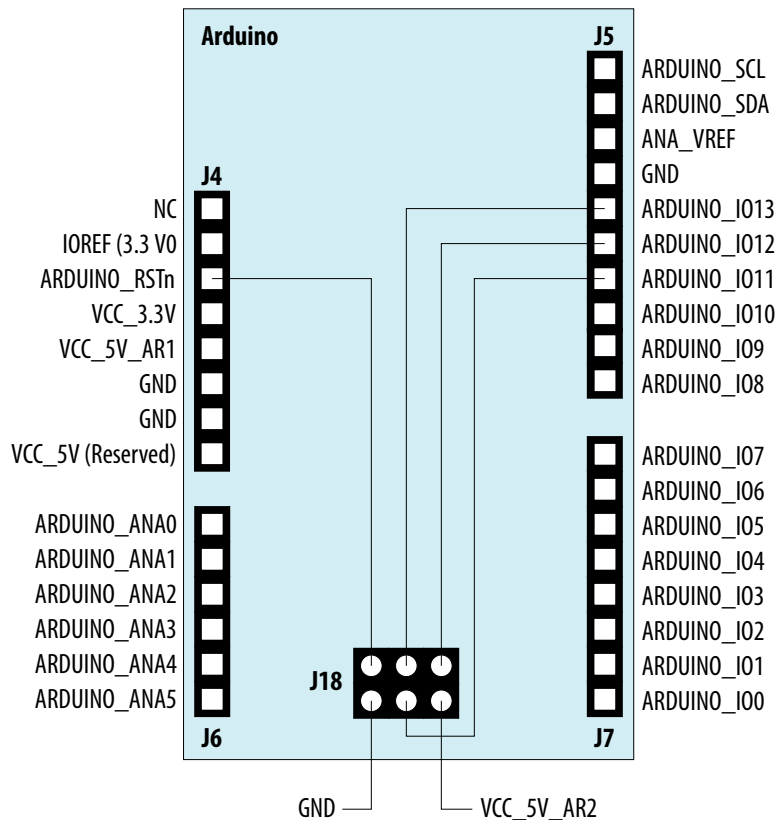


Table 16. Arduino Connector

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard	Direction @ FPGA	Description
Header 1 (PWR) J4.1	NC	---			
J4.2	IOREF	---	---	---	Connected to VCC_3.3V
J4.3	ARDUINO_RSTn	L3	3.3V	In	Arduino Reset Input
J4.4	VCC_3.3V	---			3.3V Power for Arduino shield
J4.5	VCC_5V_AR1				5V Power for Arduino shield shared with VCC_5V
J4.6	GND				
J4.7	GND				
J4.8	NC				Reserve option to 5V
Header 2 (Analog) J6.1	ARDUINO_ANA0	---	Analog	In	Arduino Analog Channel 0

continued...



Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard	Direction @ FPGA	Description
J6.2	ARDUINO_ANA1	---	Analog	In	Arduino Analog Channel 1
J6.3	ARDUINO_ANA2	---	Analog	In	Arduino Analog Channel 2
J6.4	ARDUINO_ANA3	---	Analog	In	Arduino Analog Channel 3
J6.5	ARDUINO_ANA4	---	Analog	In	Arduino Analog Channel 4
J6.6	ARDUINO_ANA5	---	Analog	In	Arduino Analog Channel 5
Header 3 (Digital) J5.1	ARDUINO_IO8	K2	3.3V	IO	Arduino Digital Bit 8
J5.2	ARDUINO_IO9	K5	3.3V	IO	Arduino Digital Bit 9
J5.3	ARDUINO_IO10	L4	3.3V	IO	Arduino Digital Bit 10
J5.4	ARDUINO_IO11	K1	3.3V	IO	Arduino Digital 11
J5.5	ARDUINO_IO12	L2	3.3V	IO	Arduino Digital 12
J5.6	ARDUINO_IO13	L1	3.3V	IO	Arduino Digital 13
J5.7	GND	---	GND	---	---
J5.8	ANA_VREF	---	Analog	In	Arduino Analog Reference Voltage Reserved
J5.9	ARDUINO_SDA	N2	3.3 V	IO	Arduino I <sup>2</sup> C Data
J5.10	ARDUINO_SCL	N1	3.3 V	IO	Arduino I <sup>2</sup> C Clock
Header 4 (Digital) J7.1	ARDUINO_IO0	B1	3.3 V	IO	Arduino Digital Bit 0
J7.2	ARDUINO_IO1	C2	3.3 V	IO	Arduino Digital Bit 1
J7.3	ARDUINO_IO2	F3	3.3 V	IO	Arduino Digital Bit 2
J7.4	ARDUINO_IO3	D1	3.3 V	IO	Arduino Digital Bit 3
J7.5	ARDUINO_IO4	G2	3.3 V	IO	Arduino Digital Bit 4
J7.6	ARDUINO_IO5	G1	3.3 V	IO	Arduino Digital Bit 5
J7.7	ARDUINO_IO6	J2	3.3 V	IO	Arduino Digital Bit 6
J7.8	ARDUINO_IO7	J1	3.3 V	IO	Arduino Digital Bit 7
Header 5 (ICSP) J18.1	ARDUINO_IO12	L2	3.3 V	IO	Short to Arduino Digital Bit 12

**continued...**





Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard	Direction @ FPGA	Description
J18.2	VCC_5V_AR2	---	---	---	5V Power for Arduino shield, shared with VCC_5v
J18.3	ARDUINO_IO13	L1	3.3 V	IO	Short to Arduino Digital Bit 13
J18.4	ARDUINO_IO11	K1	3.3 V	IO	Short to Arduino Digital Bit 11
J18.5	ARDUINO_RSTn	L3	3.3 V	In	Short to Arduino Reset Input
J18.6	GND	---	---	---	---

### Digital IOs

There are 17 bit Arduino digital IOs on Arduino connectors which are connected to the FPGA on the board. They are all 3.3V single-ended IOs.

**Caution:** The Arduino interface only supports 3.3 V I/O. Care must be taken when you connect a shield into the connectors.

### Analog Inputs

There are six analog inputs can be sourced through the Arduino header J6. These analog signals are first divided and filtered by operational amplifier MCP6242 and related components. This circuit scales the maximum allowable analog input to 5V which meets standard Aduino UNO R3.

There is one ADC block in Intel FPGA Download Cable II Intel MAX 10 device (U3), ADC block has one dedicated analog input and 8 dual function pins. Six of the nine analog input pins are used for Arduino analog input interface, other three are used for current sense.

**Table 17. Arduino Channel Connections**

Arduino Connector	ADC Channel	MAX 10 ADC Name	MAX10 Pin
ARDUINO_ANA0 (J6.1)	ADC1 Channel5	ADC1IN5	U3.C1
ARDUINO_ANA1 (J6.2)	ADC1 Channel0 (Dedicated Channel)	ANAIN1	U3.D2
ARDUINO_ANA2 (J6.3)	ADC1 Channel1	ADC1IN1	U3.D1
ARDUINO_ANA3 (J6.4)	ADC1 Channel8	ADC1IN8	U3.E1
ARDUINO_ANA4 (J6.5)	ADC1 Channel7	ADC1IN7	U3.F1
ARDUINO_ANA5 (J6.6)	ADC1 Channel4	ADC1IN4	U3.E4

Intel Cyclone 10 LP FPGA device communicates with the ADC block in the Intel MAX 10 device on the board through the ADC I<sup>2</sup>C interface, which supports both 100 KHz and 400 KHz I<sup>2</sup>C clock frequency. The ADC output value is 12-bit data and I<sup>2</sup>C data is 8-bit. Hence two register addresses are used to store 12-bit ADC output data. These registers are all read only. The ADC I<sup>2</sup>C slave address of ADC block is 0x5E.

**Table 18. Register Addresses for Arduino Channels**

Arduino Connector	Register Address
ARDUINO_ANA0 (J6.1)	0x31, 0x30
ARDUINO_ANA1 (J6.2)	0x27, 0x26
ARDUINO_ANA2 (J6.3)	0x29, 0x28
ARDUINO_ANA3 (J6.4)	0x37, 0x36
ARDUINO_ANA4 (J6.5)	0x35, 0x34
ARDUINO_ANA5 (J6.6)	0x2F, 0x2E

Use the formula to convert ADC output value to voltage:

$$\text{Voltage} = (\text{ADC\_Output\_Value}/4096) * \text{VREF} * \text{R\_Divider}$$

- ADC\_Output\_Value is the value in Decimal read from ADC I<sup>2</sup>C bus as described above.
- VREF is the MAX 10 ADC reference voltage. Use 3.3V when using MAX 10 internal reference source.
- R\_Divider<sup>(1)</sup> is a resistors divider value along with operational amplifier MCP6242 in order to allow tolerance up to 5V analog input. By default, it is 2.

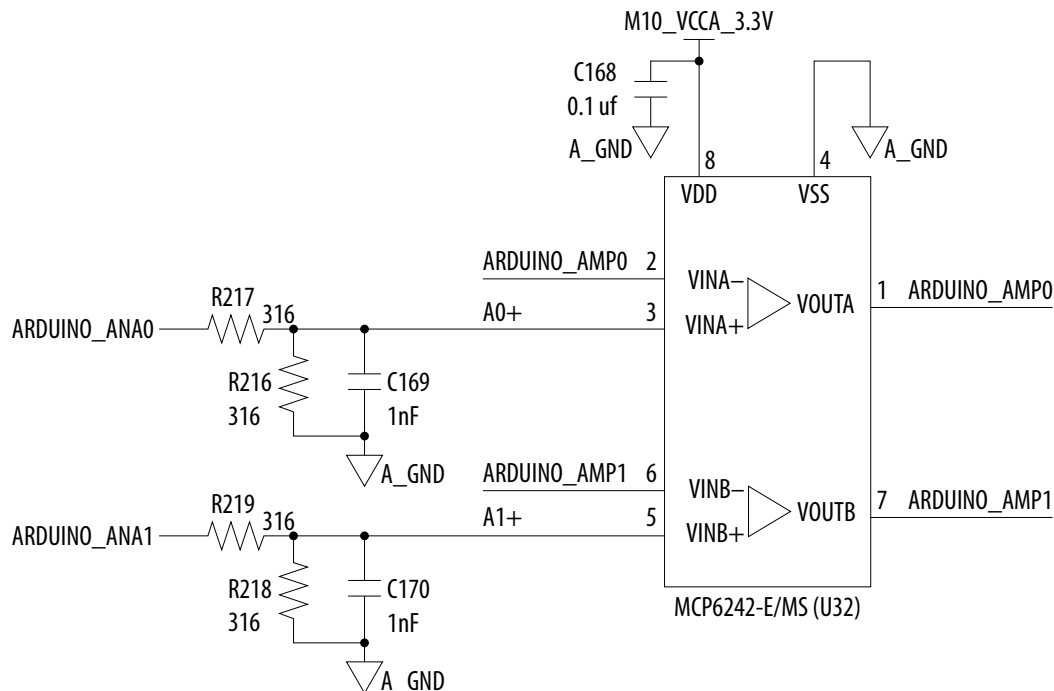
---

<sup>(1)</sup> Different analog outputs on Arduino shield have different output impedance, these divider resistor values may need to be adjusted based on your application.



Arduino Analog

Figure 7. Arduino Example



For example, if you want to measure analog input value on ARDUINO\_ANA0 (J6.1).

1. Read value of 0x30 register address is 0xB9 and read value of 0x31 register address is 0x3, then the ADC output value is 0x3B9, which is 953 decimal. Hence,

```
ADC_Output_Value=953
```

2. MAX 10 internal reference voltage is used so

```
VREF = 3.3 V
```

3. Divider resistor values are R217 = 316 ohm and R216 = 316 ohm, so

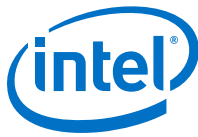
```
R_Divider = R217/R216 + 1 = 2
```

4. Calculated the analog signal voltage on ARDUINO\_ANA0 (J6.1) is

```
Voltage @ ARDUINO_ANA0 = (953/4096) * 3.3 * 2 = 1.54 V
```

Table 19. Arduino Power Output Capability

Power Rail	Output Pin Location	Maximum Current	Note
VCC_5V_AR1 VCC_5V_AR2	J4.5 J18.2	0.5 A	5V output capability to Arduino Shield, shared with VCC_5V (depends on the power adaptor specification)
VCC_3.3V	J4.4	0.05 A	VCC_3.3V output capability to Arduino Shield
IOREF	J4.2	0.05 A	Connected to VCC_3.3V



### Arduino Power

There are several power rails on the Arduino connectors.

- **IOREF**: 3.3V for digital I/Os. It must be 3.3V. 5V is forbidden as it may damage devices on the board.
- **VCC\_3.3V**: 3.3V power generated by Intel Cyclone 10 LP FPGA Evaluation Kit.
- **VCC\_5V\_AR1/2**: 5V power from Intel Cyclone 10 LP FPGA Evaluation Kit.
- **ARDUINO\_AREF**: Reserved analog reference voltage. Care must be taken that the range can be 0 ~3.3V. 5V is forbidden.

When using Arduino connector, USB may not provide sufficient power so we suggest you use external adaptor connector (J12) to power up the board.

Arduino UNO R3 did not specify limitation of output current capability. Here is the maximum output current for this Intel Cyclone 10 LP FPGA Evaluation Kit.

### 4.9.4 PMOD Connectors

The Intel Cyclone 10 LP FPGA Evaluation Kit features one Digilent Pmod™ Compatible header which is used to connect low frequency, low I/O pin count peripheral module.

The 12-pin version PMOD connector is chosen and this provides 8 I/O signal pins. The peripheral module interface also encompasses a variant using I2C interface and two or four wire MTE cables. The PMOD signals are connected to FPGA Bank 6.

**Table 20. PMOD Signals**

Board Reference	Schematic Signal Name	Schematic Share Bus Signal Name	FPGA Pin Number	I/O Standard	Direction @ FPGA	Description
PMOD (J8)	PMOD_D0	PMOD_IO0	D16	3.3V	IO	PMOD IO 0
	PMOD_D1	PMOD_IO1	F13	3.3V	IO	PMOD IO 1
	PMOD_D2	PMOD_IO2	D15	3.3V	IO	PMOD IO 2
	PMOD_D3	PMOD_IO3	F16	3.3V	IO	PMOD IO 3
	PMOD_D4	PMOD_IO4	C16	3.3V	IO	PMOD IO 4
	PMOD_D5	PMOD_IO5	F15	3.3V	IO	PMOD IO 5
	PMOD_D6	PMOD_IO6	C15	3.3V	IO	PMOD IO 6
	PMOD_D7	PMOD_IO7	B16	3.3V	IO	PMOD IO 7

PMOD Specification has not specified module power consumption but assumed no more than approximately 100 mA. On this kit, the PMOD connector can offer up to 250 mA @ 3.3V when the board is powered from external adaptor connector (J12).

When using PMOD module, USB may not provide sufficient power so we suggest you to use the external adaptor connector (J12) to power up the board.

**Table 21. PMOD Header Power Output Capability**

Power Rail	Output Pin Location	Maximum Current	Note
VCC_3.3V	J8.6, J8.12	0.25A	VCC_3.3V output capability to PMOD module

## 4.10 Memory

### 4.10.1 HyperRAM

HyperRAM is a portfolio of high-speed, low-pin-count memory product that uses the HyperBus interface technology. The Intel Cyclone 10 LP FPGA Evaluation Kit supports HyperRAM with HyperBus Controller (HBMC) IP provided by Synaptic Labs.

ISSI IS66WVH16M8ALL-166B1LI is used which is organized by 16M words x 8 bits with 1.8V interface.

**Table 22. HyperRAM Signals List**

Schematic Signal Name	FPGA Pin Number	I/O Standard	Direction @ FPGA	Description
HBUS_DQ7	R13	1.8V	IO	Data Inout/Output Bit 7
HBUS_DQ6	R12	1.8V	IO	Data Inout/Output Bit 6
HBUS_DQ5	R11	1.8V	IO	Data Inout/Output Bit 5
HBUS_DQ4	T10	1.8V	IO	Data Inout/Output Bit 4
HBUS_DQ3	R10	1.8V	IO	Data Inout/Output Bit 3
HBUS_DQ2	T11	1.8V	IO	Data Inout/Output Bit 2
HBUS_DQ1	T13	1.8V	IO	Data Inout/Output Bit 1
HBUS_DQ0	T12	1.8V	IO	Data Inout/Output Bit 0
HBUS_CKp	P14	1.8V	OUT	Differential Clock, Positive Node
HBUS_CKn	R14	1.8V	OUT	Differential Clock, Negative Node
HBUS_CS2n	P9	1.8V	OUT	Chip Select for HyperRAM
HBUS_RWDS	T14	1.8V	IO	Read Write Data Strobe
HBUS_RSTn	N9	1.8V	OUT	Hardware Reset

*continued...*



Schematic Signal Name	FPGA Pin Number	I/O Standard	Direction @ FPGA	Description
HBUS_CS1n	N12	1.8V	OUT	Chip Select for Hyper FLASH (Reserved Only)
HBUS_RST0n	T15	1.8V	IN	Reset Output from slave to master (Reserved Only)
HBUS_INTn	P11	1.8V	IN	Interrupt Output from slave to master (Reserved Only)

**Note:** If you have any questions about Hyperbus Controller (HBMC) IP, please contact Synaptic Labs at the links given below.

#### Related Links

- [Synaptic Labs Website](#)
- [Email Synaptic Labs](#)

### 4.10.2 EPCQ Flash Memory

The Intel Cyclone 10 LP FPGA Evaluation Kit has a 64 Mb Intel EPCQ64 in-system programmable NOR flash for non-volatile storage of the FPGA configuration data, board information, test application data and user code space.

Although EPCQ64 is a quad-serial flash with x4 data width, use only x1 data width because Intel Cyclone 10 LP FPGA only support AS x1 configuration scheme. Other data signals are tied to 3.3V power required by EPCQ64 data sheet.

The table below shows the memory map for this EPCQ64 flash memory. This memory provides non-volatile storage for FPGA bit stream, Nios II factory software and other information.

**Table 23. Flash Memory Map**

Block Description	Size (KB)	Address	Comments
Board Test System Scratch	512	0x0073.0000 - 0x007A.FFFF	BTS System Testing
Board Information	64	0x0072.0000 - 0x0072.FFFF	Board Information
Ethernet Option Bits	64	0x0071.0000 - 0x0071.FFFF	MAC Address Information
User Design Reset Vector	64	0x0070.0000 - 0x0070.FFFF	Nios II Reset Vector Information
Factory Software (ELF)	4096	0x0030.0000 - 0x006F.FFFF	Software File
Factory Hardware (sof)	3072	0x0000.0000 - 0x002F.FFFF	SOF File
Total	7872		

The signal connections between the Intel Cyclone 10 LP FPGA and EPCQ64 comply with the AS x1 configuration requirements.

**Table 24. Signal Connections**

Flash Pin Number	Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
U2.16	C10_AS_DCLK	U1.H1	3.3 V	FPGA Clock Output
U2.7	C10_AS_CS <sub>n</sub>	U1.D2	3.3 V	FPGA Chip Select Output
U2.8	C10_AS_DATA0	U1.H2	3.3 V	FPGA Data Input
U2.15	C10_AS_AS <sub>DO</sub>	U1.C1	3.3 V	FPGA Data and Control Signals Output

**Note:** When using SFL core and Intel Quartus Prime Programmer to program/erase the EPCQ64 flash, Virtual JTAG must be bypassed that set SW1.4 to ON. Signal Net VTAP\_BYPASS<sub>n</sub> is logic 0.

## 4.11 System Power

### 4.11.1 Power Supply Options

There are two power supply options provided for the Intel Cyclone 10 LP FPGA Evaluation Kit. The first is USB powered and the second is external AC/DC adaptor powered. These two options can be used for different applications. There is an ORING circuit on-board to select suitable power source from USB power or DC jack.

#### USB-Power

For most applications without Arduino, 2x20 GPIO, PMOD daughter cards, using an USB Cable offers sufficient current. A standard A to Mini-B USB Y-Cable is shipped with the evaluation kit. There are three USB ports as shown in the image below.

**Table 25. USB Ports**

Port	Description
P1	<ul style="list-style-type: none"> <li>• USB Standard A Plug.</li> <li>• Connects to USB host</li> <li>• Used for both USB signals and USB VBUS 5V</li> </ul>
P2	<ul style="list-style-type: none"> <li>• Complementary USB Standard A plug for additional USB VBUS 5V power.</li> <li>• No signal connection.</li> </ul>
P3	<ul style="list-style-type: none"> <li>• USB Mini-B Plug</li> <li>• Connected to USB Port J17</li> </ul>

When P1 and P2 are plugged into USB Host ports at the same time, it can supply up to 1A current to the Intel Cyclone 10 LP FPGA Evaluation Kit.

**Figure 8. USB Y-Cable**

#### AC/DC Adaptor Power

For some applications, daughter cards may draw high power consumption that USB port cannot offer sufficient current. A common 5V AC/DC adaptor can be plugged into the DC Jack J12 to offer higher current. The DC Jack uses Wurth Elektronik P/N 694106301002 as power input connector.

The required DC mate plug is required to meet the parameters below

- Inner Diameter (ID): 2.1 mm
- Outer Diameter (OD): 5.5 mm
- Voltage: 5V
- Center Polarity: Positive (5V)

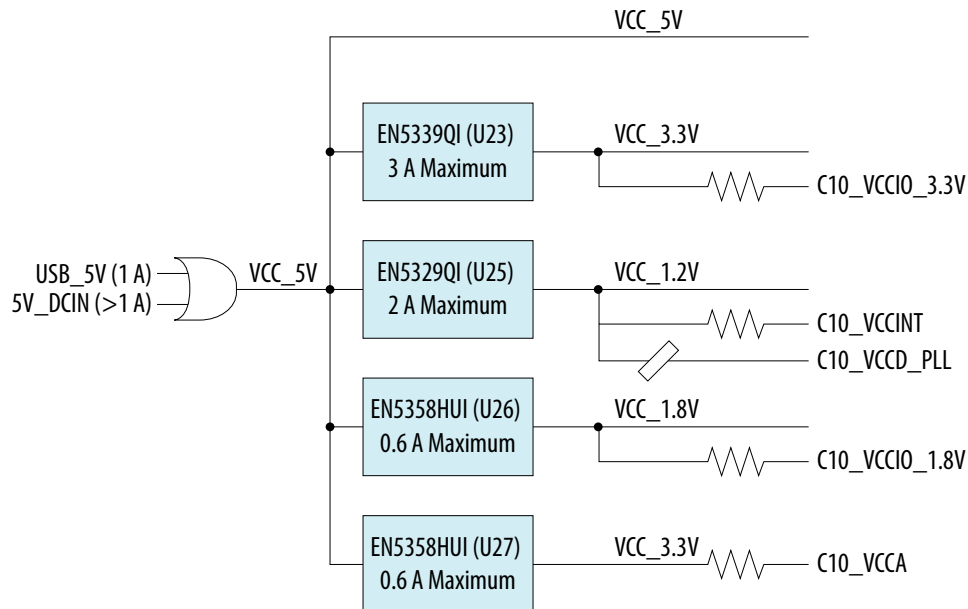
**Caution:** Use 5V adaptor for DC Jack J12 only. Components on the board can get damaged by power supplies with greater voltage.





### 4.11.2 Power Tree

Figure 9. Cyclone 10 LP FPGA Evaluation Kit Power Tree



No special power up or down sequence control used because the Intel Cyclone 10 LP FPGA can be powered up and down in any sequence.

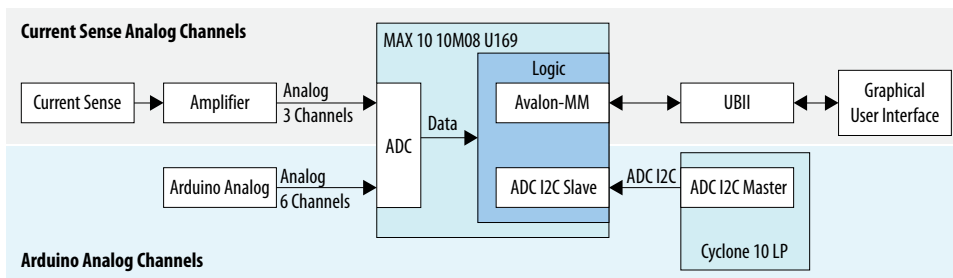
### 4.11.3 Current Measurement

To demonstrate low power feature, Intel Cyclone 10 LP FPGA power rails are isolated with resistors for voltage drop measurement either manually or automatically.

VCCINT, VCCA and VCCIO\_3.3V supports automatic current measurement. The voltage drop across sense resistors are connected to Intel MAX 10 integrated ADC with current sense amplifiers. Refer to the figure below.

The selected Intel MAX 10 10M08SA-U169 contains one ADC with 9 analog input channels. Three channels are used for Intel Cyclone 10 LP FPGA current measurement and six channels are used for Arduino analog.

Figure 10. Current Measurement





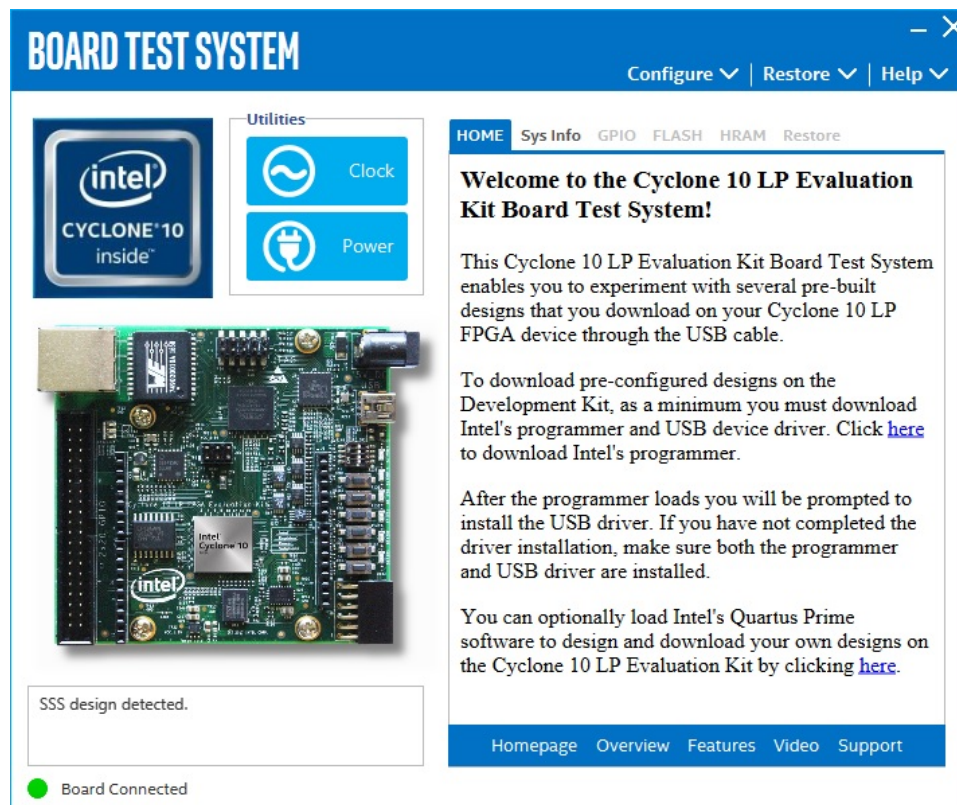
Other Intel Cyclone 10 LP FPGA power rails support manual measurement by measure voltage drop across sensing resistors with a multi-meter.



## 5 Board Test System

The evaluation kit includes an application called the Board Test System (BTS). The BTS provides an easy-to-use interface to alter the functional settings and observe the results. You can use the BTS to test board components, modify functional parameters, observe performance and measure power usage. While using the BTS, you can reconfigure the FPGA several times with test designs specific to the functionality you are testing.

**Figure 11. Board Test System (BTS) Graphical User Interface (GUI)**



Several designs are provided to test major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears that allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

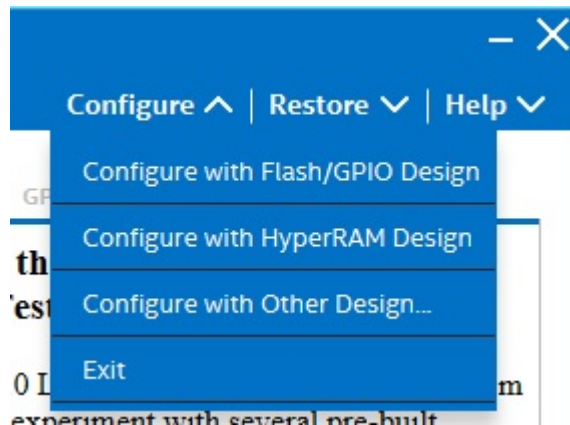
The BTS communicates over the JTAG bus to a test design running in the FPGA. The BTS and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the Signal Tap Embedded Logic Analyzer. As the Intel Quartus Prime uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time-out.

*Note:* Close other applications before attempting to reconfigure the FPGA using the Intel Quartus Prime Programmer.

## 5.1 The Configure Menu

Use the Configure menu to select the design you want to use. Each design example tests different board features. Choose a design from this menu and the corresponding tabs become active for testing.

**Figure 12. The Configure Menu**



To configure the FPGA with a test system design, perform the following steps:

1. On the Configure menu, click the configure command that corresponds to the functionality you wish to test.
2. In the dialog box that appears, click Configure to download the corresponding design to the FPGA.
3. When configuration finishes, the design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled.

If you use the Intel Quartus Prime Programmer for configuration, rather than the BTS GUI, you may need to restart the GUI.

## 5.2 The System Info Tab

The **System Info** tab shows the board's current configuration. The tab displays the JTAG chain, the board's MAC address and other details stored on the board.



Figure 13. The System Info Tab

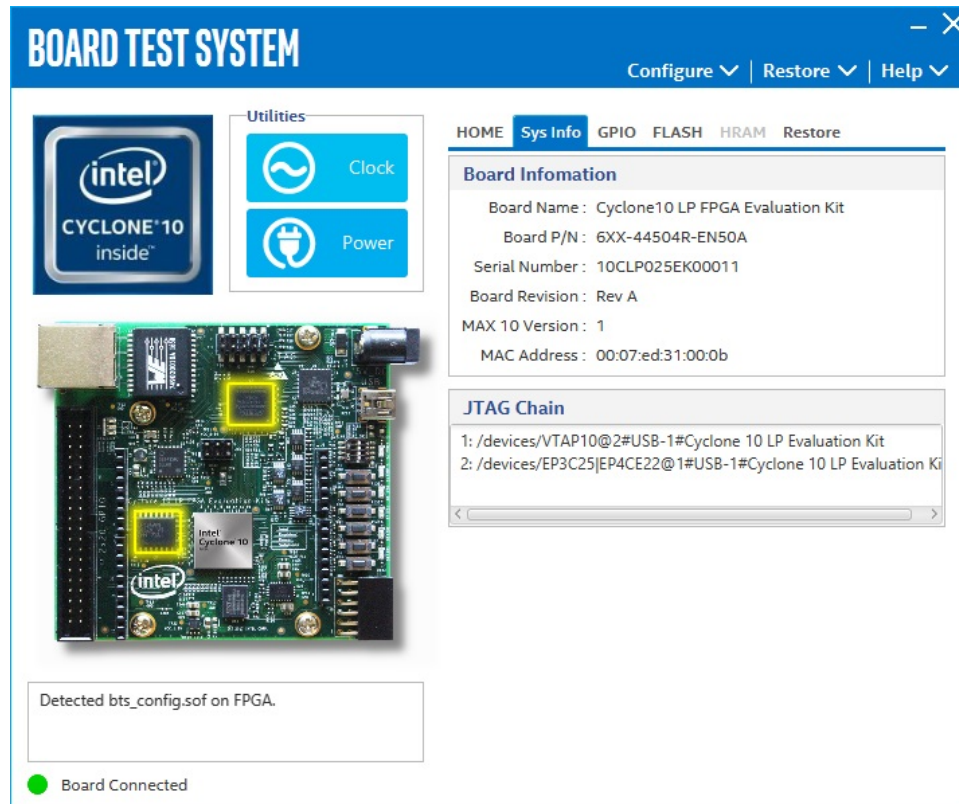


Table 26. The System Info Tab Controls

Controls	Description
Board Information	The board information is updated once the GPIO design is configured. Otherwise, this control displays the default static information about your board.
Board Name	Indicates the official name of the board, given by the Board Test System.
Board P/N	Indicates the part number of the board.
Serial Number	Indicates the serial number of the board.
Board Revision	Indicates the version of the Board.
MAX 10 Version	Indicates the version of MAX code currently running on the board.
MAC Address	Indicates the Ethernet MAC address of the board.
JTAG Chain	Shows all the devices currently in the JTAG chain.

### 5.3 The GPIO Tab

The **GPIO** tab allows you to interact with all the general purpose user I/O components on your board. You can read DIP switch settings, turn LEDs on or off, detect push button presses and Platform Designer (Standard) Memory Map of GPIO design is displayed here.

Figure 14. The GPIO Tab

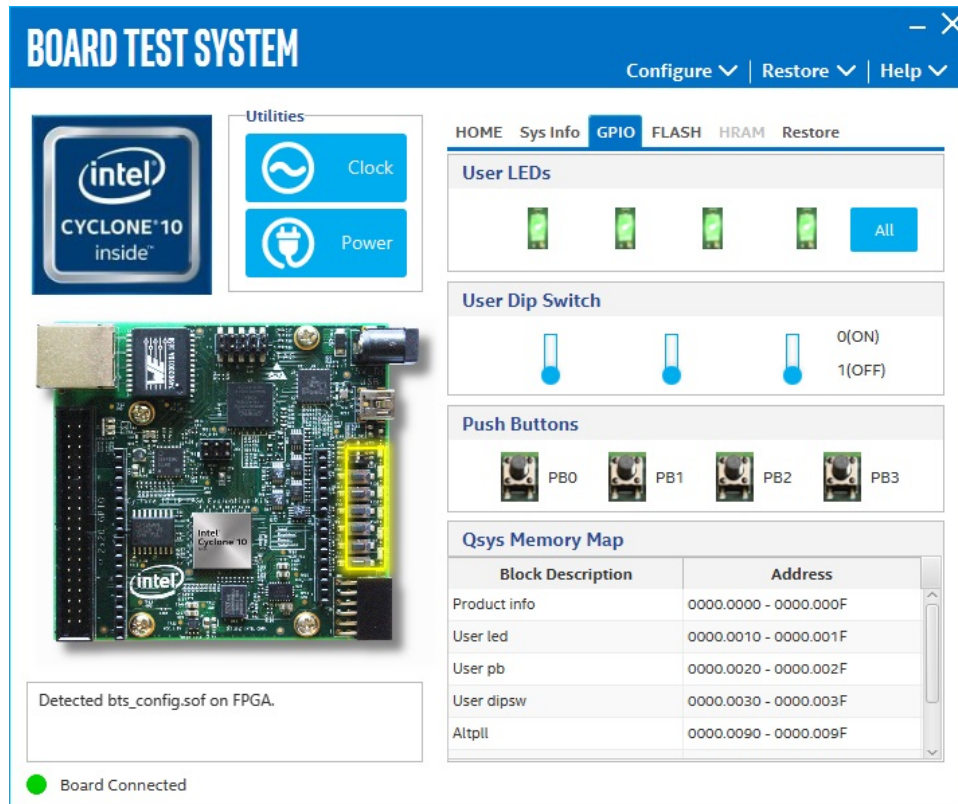


Table 27. The GPIO Tab Controls

Control	Description
User LEDs	Displays the current state of the user LEDs for the FPGA. To toggle the board LEDs, click the <b>0</b> to <b>3</b> buttons to toggle red or green LEDs, or click the <b>All</b> button.
User DIP Switch	Displays the current positions of the switches in the user DIP switch banks. Change the switches on the board to see the graphical display change accordingly.
Push Buttons	Read-only control displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly.
Platform Designer (Standard) Memory Map	Shows the memory map of the Platform Designer (Standard) system on your board.

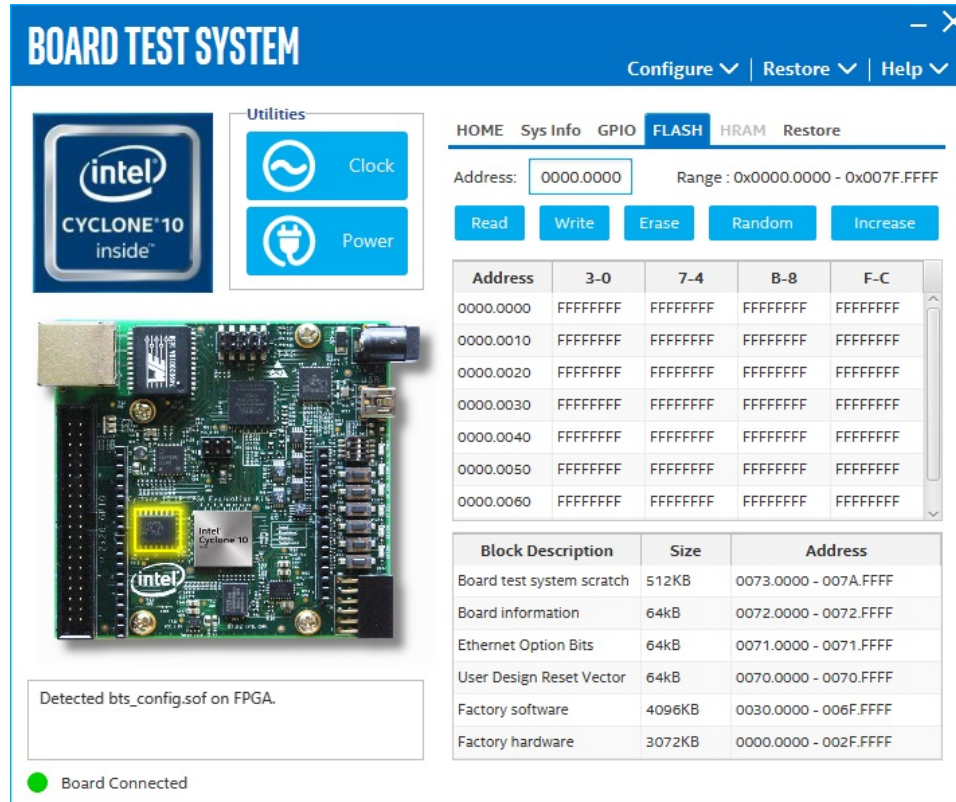
## 5.4 The Flash Tab

The **Flash** Tab allows you to read and write flash memory on your board.





Figure 15. The Flash Tab



Control	Description
<b>Read</b>	Reads the flash memory on your board. To see the flash memory contents, type a starting address in the text box and click Read. Values starting at the specified address appear in the table.
<b>Write</b>	Writes the flash memory on your board. To update the flash memory contents, change values in the table and click Write. The application writes the new values to flash memory and then reads the values back to guarantee that the graphical display accurately reflects the memory contents.
<b>Erase</b>	Erases flash memory.
<b>Increase</b>	Starts an incrementing data pattern test to flash memory, limited to the 512 K test system scratch page.
<b>Random</b>	Starts a random data pattern test to flash memory, limited to the 512 K test system scratch page.
<b>Flash Memory Map</b>	Displays the flash memory map for the development board.

## 5.5 The HyperRAM Tab

The **HyperRAM** tab allows you to test the HyperRAM by reading and writing to a selected amount of addresses.

Figure 16. The HyperRAM Tab

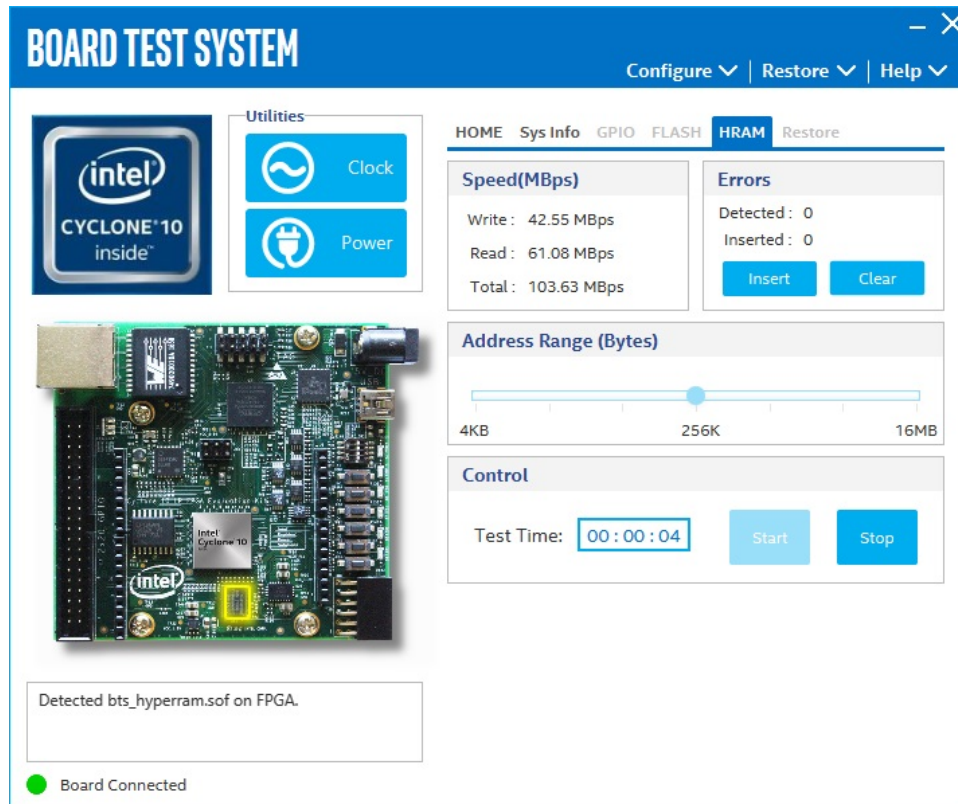


Table 28. The HyperRAM Tab Controls

Control	Description
Speed (MBps)	<ul style="list-style-type: none"> <li><b>Write (MBps), Read (MBps), and Total (MBps)</b>—Show the number of bytes of data analyzed per second.</li> <li>Data bus: 8 bit wide and the frequency is 150 MHz double data rate. 300 Megabits per second (Mbps) per pin. Equating to a theoretical maximum bandwidth of 2400 Mbps or 300 MBps.</li> </ul>
Errors	<p>This control displays data errors detected during analysis and allows you to insert errors:</p> <ul style="list-style-type: none"> <li><b>Detected</b>—Displays the number of data errors detected in the hardware.</li> <li><b>Inserted</b>—Displays the number of errors inserted into the transaction stream.</li> <li><b>Insert</b>—Inserts a one-word error into the transaction stream each time you click the button. Insert Error is only enabled during transaction performance analysis.</li> </ul> <p><i>Note:</i> For Address Range of 16 MB, ensure the interval between two clicks on <b>Insert</b> button is larger than the one during testing.</p> <ul style="list-style-type: none"> <li><b>Clear</b>—Resets the Detected errors and Inserted errors counters to zeroes.</li> </ul>
Address Range (Bytes)	Determines the number of addresses to use in each iteration of reads and writes.
Control	These controls display test times since you last clicked <b>Start</b> .





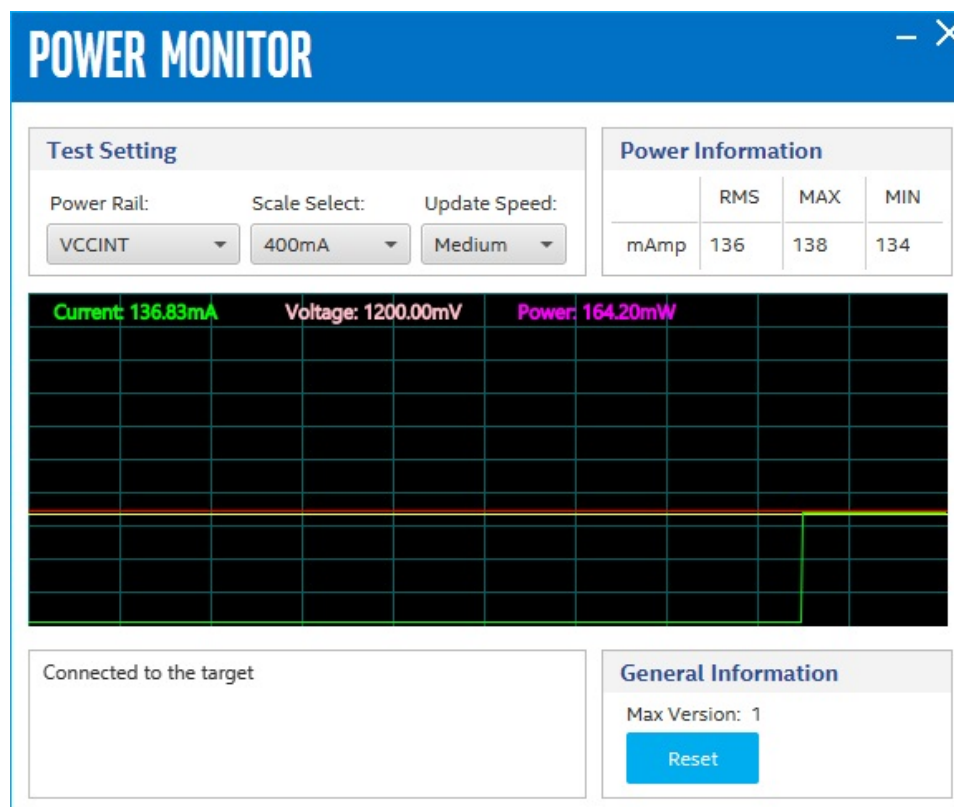
## 5.6 The Power Monitor

The Power Monitor measures and reports current power information and communicates with the Intel MAX 10 device on the board through the JTAG bus. A power monitor circuit attached to the Intel MAX 10 device allows you to measure the power that the FPGA is consuming.

To start the application, click the Power Monitor icon in the Board Test System application. You can also run the Power Monitor as a stand-alone application. The PowerMonitor.exe resides in the <package\_dir>\examples\board\_test\_system directory.

**Caution:** You cannot run the stand-alone power application and the BTS application at the same time.

**Figure 17.** The Power Monitor



This window displays Intel Cyclone 10 LP current monitors.

**Current** shows the current value of each power rail:

- 3.3 V VCCIO
- 2.5 V VCCA
- 1.2 V VCCINT

**Voltage** shows the typical voltage value of each power rail. It is not read from ADC.

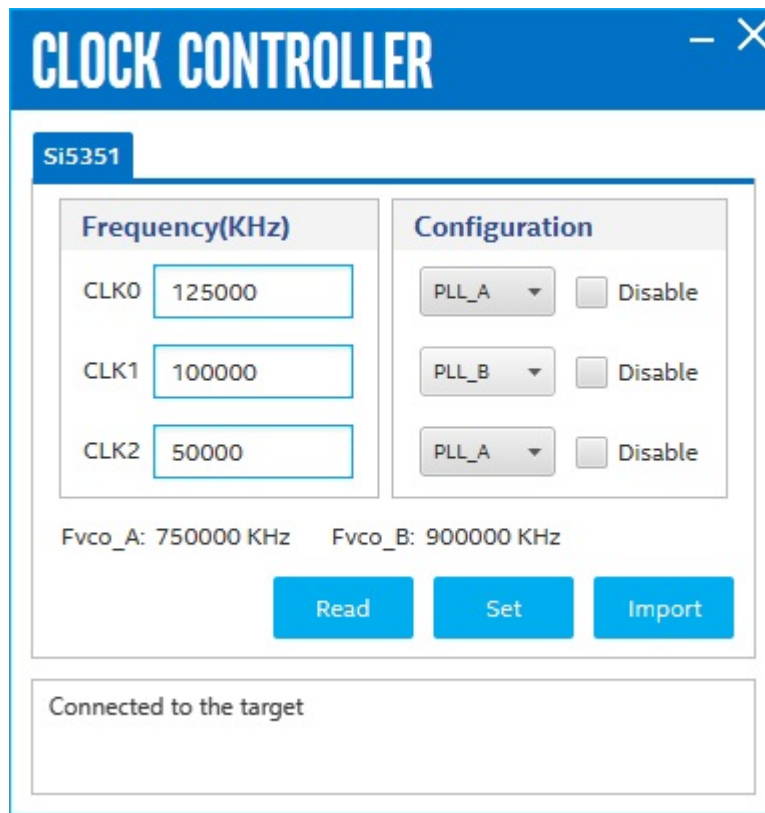
**Update Speed** allows you to select **Slow** at 5 seconds, or **Fast**: at 1 second (default).

## 5.7 The Clock Control

The Intel Cyclone 10 LP FPGA Evaluation Kit Clock Control application sets the programmable oscillator to any frequency between 3 KHz and 200 MHz.

The Clock Control communicates with the Intel MAX 10 device on the board through the JTAG bus. The programmable oscillator is connected to the Intel MAX 10 device through a 2-wire serial bus.

**Figure 18. The Si5351 Tab**



**Table 29. The Si5351 Tab Controls**

Control	Description
Fvco_A/Fvco_B	Displays the generating signal value of the voltage-controlled oscillator.
Frequency (KHz)	Allows you to specify the frequency of the clock.
PLL Choose	Allows you to specify the PLL used by the clock.
Disable	Disable each clock output as required.

*continued...*



Control	Description
Read	Reads the current frequency setting for the oscillator associated with the active tab.
Set	Sets the programmable oscillator frequency for the selected clock to the value in the <code>CLK0</code> to <code>CLK2</code> controls. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Intel recommends resetting the FPGA logic after changing frequencies.
Import	Allows you to import a register table file generated by Clock Builder. You can reset the clock to default by importing the default register file " <code>Si5351A-Registers.txt</code> " in the application folder.



## A Safety and Regulatory Information

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### **ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE**

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

### **A.1 Safety Warnings**

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\*Other names and brands may be claimed as the property of others.

**ISO  
9001:2008  
Registered**





**Power Supply Hazardous Voltage**

AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.


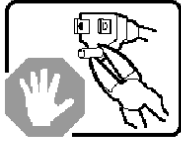
**Power Connect and Disconnect**

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.

	<b>WARNING</b>	
	<b>RISK OF ELECTRIC SHOCK</b>	
<p>Connect only to a properly earth grounded outlet.                  Apparaten skall anslutas till jordat uttag när den ansluts till ett nätverk.</p>		

**System Grounding (Earthing)**

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product will be attached is also connected to properly wired and grounded receptacles.

	<b>WARNING</b>	
	<b>RISK OF ELECTRIC SHOCK</b>	
<p>Do not attempt to modify or use the supplied AC power cord if it is not the exact type and rating required.</p>		

**Power Cord Requirements**

The connector that plugs into the wall outlet must be a grounding-type male plug designed for use in your region. It must have marks showing certification by an agency in your region. The connector that plugs into the AC receptacle on the power

supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord and do not use it with adapters.



### Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

### Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

## A.2 Safety Cautions

	CAUTION	
	Hot Surfaces and Sharp Edges	
Integrated Circuits and heat sinks may be hot if the system has been running. Also, there might be sharp pins and edges on some boards. Contact should be avoided.		

**Caution:** Hot Surfaces and Sharp Edges. Integrated Circuits and heat sinks may be hot if the system has been running. Also, there might be sharp edges on some boards. Contact should be avoided.

### Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.



### Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

### Electro-Magnetic Interference (EMI)

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment on and off, the user is required to take measures to eliminate this interference.

### Telecommunications Port Restrictions

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obtained.



### **Electrostatic Discharge (ESD) Warning**

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

**Attention:** Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.





## B Additional Information

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### B.1 User Guide Revision History

**Table 30. Intel Cyclone 10 LP FPGA Evaluation Kit User Guide Revision History**

Date	Version	Description
August 2017	2017.08.23	Preliminary Release

### B.2 Compliance and Conformity Statements

#### CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2004/108/EC. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.

