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Kind regards,

Team Nexperia

# 74AVCH4T245

## 4-bit dual supply translating transceiver with configurable voltage translation; 3-state

Rev. 5 — 17 December 2015

Product data sheet

### 1. General description

The 74AVCH4T245 is a 4-bit, dual supply transceiver that enables bidirectional level translation. The device can be used as two 2-bit transceivers or as a 4-bit transceiver. It features two 2-bit input-output ports (nAn and nBn), a direction control input (nDIR), an output enable input ( $\overline{\text{nOE}}$ ) and dual supply pins ( $V_{\text{CC(A)}}$  and  $V_{\text{CC(B)}}$ ). Both  $V_{\text{CC(A)}}$  and  $V_{\text{CC(B)}}$  can be supplied at any voltage between 0.8 V and 3.6 V making the device suitable for translating between any of the low voltage nodes (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V). Pins nAn,  $\overline{\text{nOE}}$  and nDIR are referenced to  $V_{\text{CC(A)}}$  and pins nBn are referenced to  $V_{\text{CC(B)}}$ . A HIGH on nDIR allows transmission from nAn to nBn and a LOW on nDIR allows transmission from nBn to nAn. The output enable input ( $\overline{\text{nOE}}$ ) can be used to disable the outputs so the buses are effectively isolated.

The device is fully specified for partial power-down applications using  $I_{\text{OFF}}$ . The  $I_{\text{OFF}}$  circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either  $V_{\text{CC(A)}}$  or  $V_{\text{CC(B)}}$  are at GND level, both nAn and nBn outputs are in the high-impedance OFF-state. The bus hold circuitry on the powered-up side always stays active.

The 74AVCH4T245 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

### 2. Features and benefits

- Wide supply voltage range:
  - ◆  $V_{\text{CC(A)}}$ : 0.8 V to 3.6 V
  - ◆  $V_{\text{CC(B)}}$ : 0.8 V to 3.6 V
- Complies with JEDEC standards:
  - ◆ JESD8-12 (0.8 V to 1.3 V)
  - ◆ JESD8-11 (0.9 V to 1.65 V)
  - ◆ JESD8-7 (1.2 V to 1.95 V)
  - ◆ JESD8-5 (1.8 V to 2.7 V)
  - ◆ JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - ◆ HBM JESD22-A114E Class 3B exceeds 8000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
  - ◆ CDM JESD22-C101C exceeds 1000 V
- Maximum data rates:
  - ◆ 380 Mbit/s ( $\geq 1.8$  V to 3.3 V translation)



- ◆ 200 Mbit/s ( $\geq 1.1$  V to 3.3 V translation)
- ◆ 200 Mbit/s ( $\geq 1.1$  V to 2.5 V translation)
- ◆ 200 Mbit/s ( $\geq 1.1$  V to 1.8 V translation)
- ◆ 150 Mbit/s ( $\geq 1.1$  V to 1.5 V translation)
- ◆ 100 Mbit/s ( $\geq 1.1$  V to 1.2 V translation)
- Suspend mode
- Bus hold on data inputs
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and  $-40$  °C to  $+125$  °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AVCH4T245D	$-40$ °C to $+125$ °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AVCH4T245PW	$-40$ °C to $+125$ °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AVCH4T245BQ	$-40$ °C to $+125$ °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body $2.5 \times 3.5 \times 0.85$ mm	SOT763-1
74AVCH4T245GU	$-40$ °C to $+125$ °C	XQFN16	plastic, extremely thin quad flat package; no leads; 16 terminals; body $1.80 \times 2.60 \times 0.50$ mm	SOT1161-1

### 4. Marking

Table 2. Marking codes

Type number	Marking code
74AVCH4T245D	74AVCH4T245D
74AVCH4T245PW	CH4T245
74AVCH4T245BQ	H4T245
74AVCH4T245GU	K4

5. Functional diagram

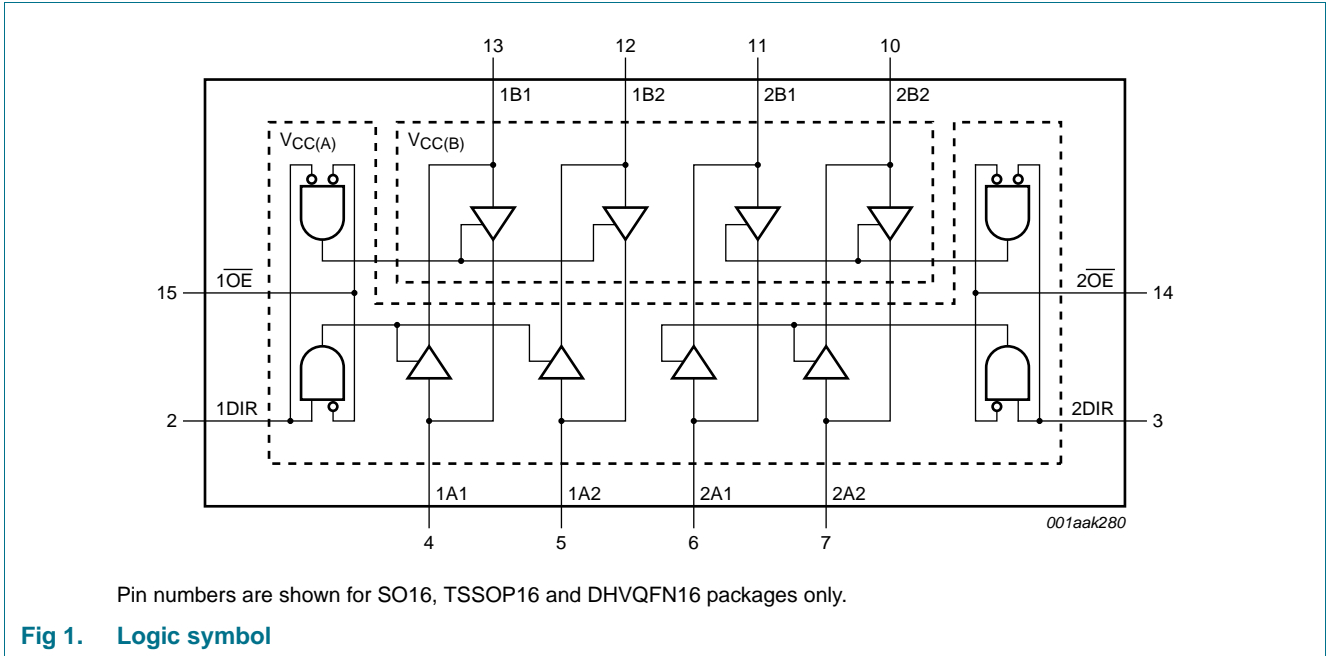


Fig 1. Logic symbol

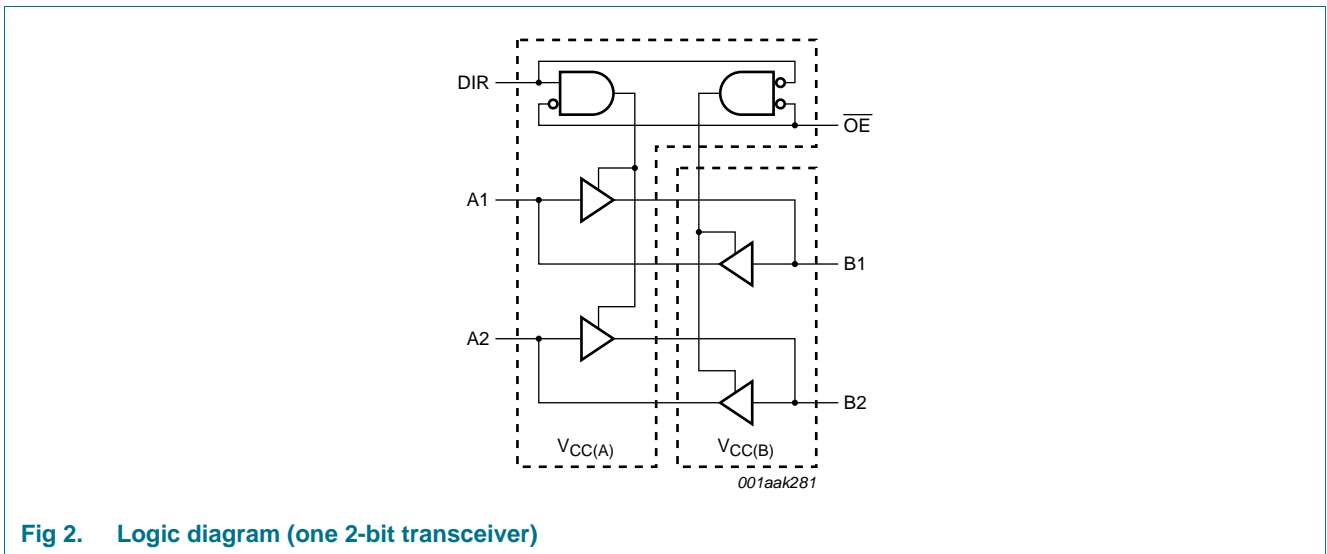


Fig 2. Logic diagram (one 2-bit transceiver)

6. Pinning information

6.1 Pinning

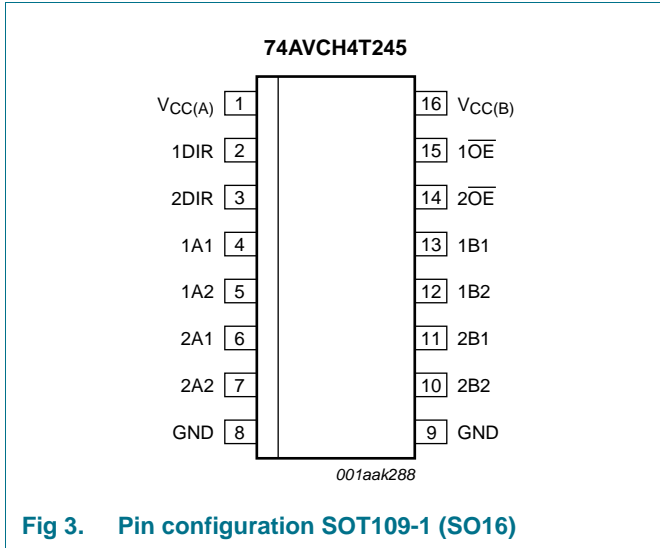


Fig 3. Pin configuration SOT109-1 (SO16)

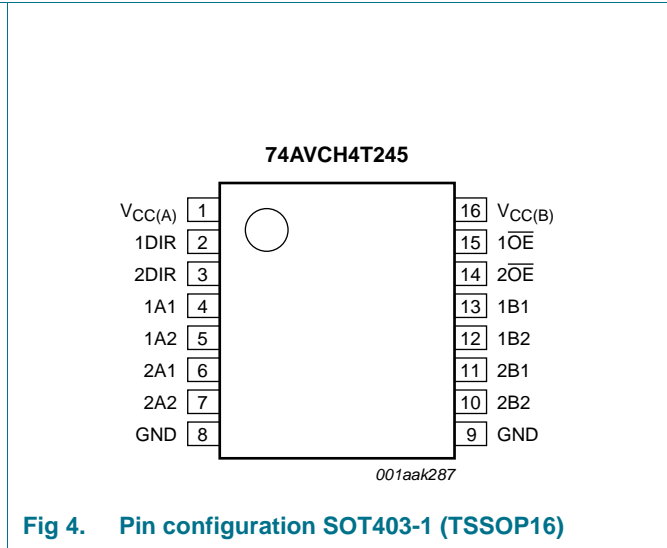


Fig 4. Pin configuration SOT403-1 (TSSOP16)

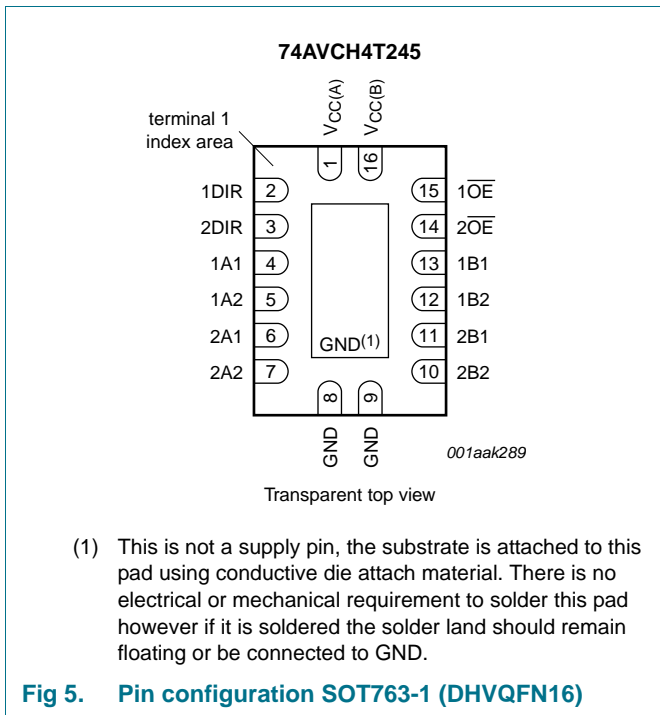


Fig 5. Pin configuration SOT763-1 (DHVQFN16)

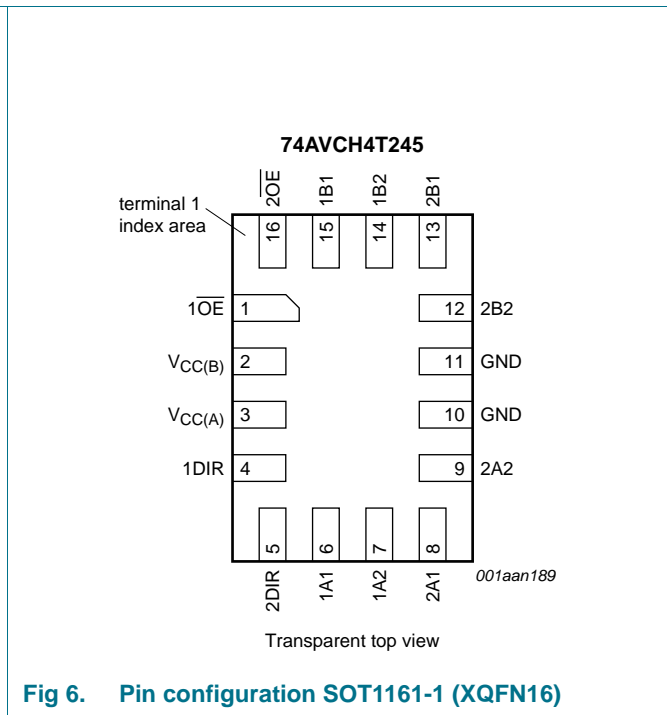


Fig 6. Pin configuration SOT1161-1 (XQFN16)

## 6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT109-1, SOT403-1 and SOT763-1	SOT1161-1	
$V_{CC(A)}$	1	3	supply voltage A ( $nA_n$ , $\overline{nOE}$ and $nDIR$ inputs are referenced to $V_{CC(A)}$ )
1DIR, 2DIR	2, 3	4, 5	direction control
1A1, 1A2	4, 5	6, 7	data input or output
2A1, 2A2	6, 7	8, 9	data input or output
GND <sup>[1]</sup>	8, 9	10, 11	ground (0 V)
2B2, 2B1	10, 11	12, 13	data input or output
1B2, 1B1	12, 13	14, 15	data input or output
$\overline{2OE}$ , $\overline{1OE}$	14, 15	16, 1	output enable input (active LOW)
$V_{CC(B)}$	16	2	supply voltage B ( $nB_n$ inputs are referenced to $V_{CC(B)}$ )

[1] All GND pins must be connected to ground (0 V).

## 7. Functional description

Table 4. Function table<sup>[1]</sup>

Supply voltage	Input		Input/output <sup>[3]</sup>	
	$\overline{nOE}$ <sup>[2]</sup>	$nDIR$ <sup>[2]</sup>	$nA_n$ <sup>[2]</sup>	$nB_n$ <sup>[2]</sup>
0.8 V to 3.6 V	L	L	$nA_n = nB_n$	input
0.8 V to 3.6 V	L	H	input	$nB_n = nA_n$
0.8 V to 3.6 V	H	X	Z	Z
GND <sup>[3]</sup>	X	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] The  $nA_n$ ,  $nDIR$  and  $\overline{nOE}$  input circuit is referenced to  $V_{CC(A)}$ ; The  $nB_n$  input circuit is referenced to  $V_{CC(B)}$ .

[3] If at least one of  $V_{CC(A)}$  or  $V_{CC(B)}$  is at GND level, the device goes into suspend mode.

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			-0.5	+4.6	V
$V_{CC(B)}$	supply voltage B			-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V		-50	-	mA
$V_I$	input voltage		[1]	-0.5	+4.6	V
$I_{OK}$	output clamping current	$V_O < 0$ V		-50	-	mA
$V_O$	output voltage	Active mode	[1][2][3]	-0.5	$V_{CCO} + 0.5$	V
		Suspend or 3-state mode	[1]	-0.5	+4.6	V
$I_O$	output current	$V_O = 0$ V to $V_{CCO}$	[2]	-	$\pm 50$	mA
$I_{CC}$	supply current	per $V_{CC(A)}$ or $V_{CC(B)}$ pin		-	100	mA
$I_{GND}$	ground current	per GND pin		-100	-	mA
$T_{stg}$	storage temperature			-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C				
		SO16, TSSOP16 and DHVQFN16	[4]	-	500	mW
		XQFN16	[5]	-	250	mW

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2]  $V_{CCO}$  is the supply voltage associated with the output port.

[3]  $V_{CCO} + 0.5$  V should not exceed 4.6 V.

[4] For SO16 package: above 70 °C the value of  $P_{tot}$  derates linearly at 8 mW/K.

For TSSOP16 package: above 60 °C the value of  $P_{tot}$  derates linearly at 5.5 mW/K.

For DHVQFN16 package: above 60 °C the value of  $P_{tot}$  derates linearly at 4.5 mW/K.

[5] For XQFN16 package: above 133 °C the value of  $P_{tot}$  derates linearly with 14.5 mW/K.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			0.8	3.6	V
$V_{CC(B)}$	supply voltage B			0.8	3.6	V
$V_I$	input voltage			0	3.6	V
$V_O$	output voltage	Active mode	[1]	0	$V_{CCO}$	V
		Suspend or 3-state mode		0	3.6	V
$T_{amb}$	ambient temperature			-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CCI} = 0.8$ V to 3.6 V	[2]	-	5	ns/V

[1]  $V_{CCO}$  is the supply voltage associated with the output port.

[2]  $V_{CCI}$  is the supply voltage associated with the input port.

## 10. Static characteristics

**Table 7. Typical static characteristics at  $T_{amb} = 25\text{ °C}$  [1][2]**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = -1.5 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V		-	0.69	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = 1.5 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V		-	0.07	-	V
I <sub>I</sub>	input leakage current	nDIR, nOE input; V <sub>I</sub> = 0 V or 3.6 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V		-	±0.025	±0.25	μA
I <sub>BHL</sub>	bus hold LOW current	A or B port; V <sub>I</sub> = 0.42 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.2 V	[3]	-	26	-	μA
I <sub>BHH</sub>	bus hold HIGH current	A or B port; V <sub>I</sub> = 0.78 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.2 V	[4]	-	-24	-	μA
I <sub>BHLO</sub>	bus hold LOW overdrive current	A or B port; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.2 V	[5]	-	27	-	μA
I <sub>BHHO</sub>	bus hold HIGH overdrive current	A or B port; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.2 V	[6]	-	-26	-	μA
I <sub>OZ</sub>	OFF-state output current	A or B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.6 V	[7]	-	±0.5	±2.5	μA
		suspend mode A port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	[7]	-	±0.5	±2.5	μA
		suspend mode B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	[7]	-	±0.5	±2.5	μA
I <sub>OFF</sub>	power-off leakage current	A port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V		-	±0.1	±1	μA
		B port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(B)</sub> = 0 V; V <sub>CC(A)</sub> = 0.8 V to 3.6 V		-	±0.1	±1	μA
C <sub>I</sub>	input capacitance	nDIR, nOE input; V <sub>I</sub> = 0 V or 3.3 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.3 V		-	1.0	-	pF
C <sub>I/O</sub>	input/output capacitance	A and B port; V <sub>O</sub> = 3.3 V or 0 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.3 V		-	4.0	-	pF

- [1] V<sub>CCO</sub> is the supply voltage associated with the output port.
- [2] V<sub>CCI</sub> is the supply voltage associated with the data input port.
- [3] The bus hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub> max. I<sub>BHL</sub> should be measured after lowering V<sub>I</sub> to GND and then raising it to V<sub>IL</sub> max.
- [4] The bus hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub> min. I<sub>BHH</sub> should be measured after raising V<sub>I</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub> min.
- [5] An external driver must source at least I<sub>BHLO</sub> to switch this node from LOW to HIGH.
- [6] An external driver must sink at least I<sub>BHHO</sub> to switch this node from HIGH to LOW.
- [7] For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.



**Table 8. Static characteristics** [1][2]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	data input					
		V <sub>CCI</sub> = 0.8 V	0.70V <sub>CCI</sub>	-	0.70V <sub>CCI</sub>	-	V
		V <sub>CCI</sub> = 1.1 V to 1.95 V	0.65V <sub>CCI</sub>	-	0.65V <sub>CCI</sub>	-	V
		V <sub>CCI</sub> = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		V <sub>CCI</sub> = 3.0 V to 3.6 V	2	-	2	-	V
		nDIR, n $\overline{\text{OE}}$ input					
		V <sub>CC(A)</sub> = 0.8 V	0.70V <sub>CC(A)</sub>	-	0.70V <sub>CC(A)</sub>	-	V
		V <sub>CC(A)</sub> = 1.1 V to 1.95 V	0.65V <sub>CC(A)</sub>	-	0.65V <sub>CC(A)</sub>	-	V
V <sub>IL</sub>	LOW-level input voltage	data input					
		V <sub>CCI</sub> = 0.8 V	-	0.30V <sub>CCI</sub>	-	0.30V <sub>CCI</sub>	V
		V <sub>CCI</sub> = 1.1 V to 1.95 V	-	0.35V <sub>CCI</sub>	-	0.35V <sub>CCI</sub>	V
		V <sub>CCI</sub> = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V <sub>CCI</sub> = 3.0 V to 3.6 V	-	0.8	-	0.8	V
		nDIR, n $\overline{\text{OE}}$ input					
		V <sub>CC(A)</sub> = 0.8 V	-	0.30V <sub>CC(A)</sub>	-	0.30V <sub>CC(A)</sub>	V
		V <sub>CC(A)</sub> = 1.1 V to 1.95 V	-	0.35V <sub>CC(A)</sub>	-	0.35V <sub>CC(A)</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = -100 $\mu$ A; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	V <sub>CCO</sub> - 0.1	-	V <sub>CCO</sub> - 0.1	-	V
		I <sub>O</sub> = -3 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.1 V	0.85	-	0.85	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	1.05	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	1.2	-	1.2	-	V
		I <sub>O</sub> = -9 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	1.75	-	1.75	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	2.3	-	2.3	-	V

**Table 8. Static characteristics ...continued** [1][2]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = 100 μA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	0.1	-	0.1	V
		I <sub>O</sub> = 3 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.1 V	-	0.25	-	0.25	V
		I <sub>O</sub> = 6 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	-	0.35	-	0.35	V
		I <sub>O</sub> = 8 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	-	0.45	-	0.45	V
		I <sub>O</sub> = 9 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	-	0.55	-	0.55	V
		I <sub>O</sub> = 12 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	-	0.7	-	0.7	V
I <sub>I</sub>	input leakage current	nDIR, nOE input; V <sub>I</sub> = 0 V or 3.6 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	±1	-	±5	μA
I <sub>BHL</sub>	bus hold LOW current	A or B port [3]					
		V <sub>I</sub> = 0.49 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	15	-	15	-	μA
		V <sub>I</sub> = 0.58 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	25	-	25	-	μA
		V <sub>I</sub> = 0.70 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	45	-	45	-	μA
		V <sub>I</sub> = 0.80 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	100	-	90	-	μA
I <sub>BHH</sub>	bus hold HIGH current	A or B port [4]					
		V <sub>I</sub> = 0.91 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	-15	-	-15	-	μA
		V <sub>I</sub> = 1.07 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	-25	-	-25	-	μA
		V <sub>I</sub> = 1.60 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	-45	-	-45	-	μA
		V <sub>I</sub> = 2.00 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	-100	-	-100	-	μA
I <sub>BHLO</sub>	bus hold LOW overdrive current	A or B port [5]					
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.6 V	125	-	125	-	μA
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.95 V	200	-	200	-	μA
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.7 V	300	-	300	-	μA
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.6 V	500	-	500	-	μA
I <sub>BHHO</sub>	bus hold HIGH overdrive current	A or B port [6]					
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.6 V	-125	-	-125	-	μA
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.95 V	-200	-	-200	-	μA
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.7 V	-300	-	-300	-	μA
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.6 V	-500	-	-500	-	μA

**Table 8. Static characteristics ...continued** [\[1\]](#)[\[2\]](#)

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I <sub>OZ</sub>	OFF-state output current	A or B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.6 V <a href="#">[1]</a>	-	±5	-	±30	μA
		suspend mode A port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V <a href="#">[1]</a>	-	±5	-	±30	μA
		suspend mode B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V <a href="#">[1]</a>	-	±5	-	±30	μA
I <sub>OFF</sub>	power-off leakage current	A port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	±5	-	±30	μA
		B port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(B)</sub> = 0 V; V <sub>CC(A)</sub> = 0.8 V to 3.6 V	-	±5	-	±30	μA

**Table 8. Static characteristics ...continued** [1][2]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I <sub>CC</sub>	supply current	A port; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A					
		V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	10	-	55	μA
		V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	8	-	50	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	8	-	50	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	-2	-	-12	-	μA
		B port; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A					
		V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	10	-	55	μA
		V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	8	-	50	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-2	-	-12	-	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	-	8	-	50	μA
		A plus B port (I <sub>CC(A)</sub> + I <sub>CC(B)</sub> ); I <sub>O</sub> = 0 A; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	20	-	70	μA
		A plus B port (I <sub>CC(A)</sub> + I <sub>CC(B)</sub> ); I <sub>O</sub> = 0 A; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	16	-	65	μA

- [1] V<sub>CCO</sub> is the supply voltage associated with the output port.
- [2] V<sub>CCI</sub> is the supply voltage associated with the data input port.
- [3] The bus hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub> max. I<sub>BHL</sub> should be measured after lowering V<sub>I</sub> to GND and then raising it to V<sub>IL</sub> max.
- [4] The bus hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub> min. I<sub>BHH</sub> should be measured after raising V<sub>I</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub> min.
- [5] An external driver must source at least I<sub>BHLO</sub> to switch this node from LOW to HIGH.
- [6] An external driver must sink at least I<sub>BHHO</sub> to switch this node from HIGH to LOW.
- [7] For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

**Table 9. Typical total supply current (I<sub>CC(A)</sub> + I<sub>CC(B)</sub>)**

V <sub>CC(A)</sub>	V <sub>CC(B)</sub>							Unit
	0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	0.1	0.1	0.1	0.1	0.1	0.1	μA
0.8 V	0.1	0.1	0.1	0.1	0.1	0.3	1.6	μA
1.2 V	0.1	0.1	0.1	0.1	0.1	0.1	0.8	μA
1.5 V	0.1	0.1	0.1	0.1	0.1	0.1	0.4	μA
1.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.2	μA
2.5 V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	μA
3.3 V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	μA

## 11. Dynamic characteristics

**Table 10. Typical power dissipation capacitance at  $V_{CC(A)} = V_{CC(B)}$  and  $T_{amb} = 25\text{ °C}$  [1][2]**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$V_{CC(A)} = V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$C_{PD}$	power dissipation capacitance	A port: (direction nAn to nBn); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction nAn to nBn); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction nBn to nAn); output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		A port: (direction nBn to nAn); output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction nAn to nBn); output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		B port: (direction nAn to nBn); output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction nBn to nAn); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		B port: (direction nBn to nAn); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

[2]  $f_i = 10\text{ MHz}$ ;  $V_i = \text{GND to } V_{CC}$ ;  $t_r = t_f = 1\text{ ns}$ ;  $C_L = 0\text{ pF}$ ;  $R_L = \infty\ \Omega$ .

**Table 11. Typical dynamic characteristics at  $V_{CC(A)} = 0.8\text{ V}$  and  $T_{amb} = 25\text{ °C}$**

*Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 9](#); for wave forms see [Figure 7](#) and [Figure 8](#)*

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$t_{pd}$	propagation delay	nAn to nBn	14.5	7.3	6.5	6.2	5.9	6.0	ns
		nBn to nAn	14.5	12.7	12.4	12.3	12.1	12.0	ns
$t_{dis}$	disable time	$\overline{nOE}$ to nAn	14.3	14.3	14.3	14.3	14.3	14.3	ns
		$\overline{nOE}$ to nBn	17.0	9.9	9.0	9.4	9.0	9.7	ns
$t_{en}$	enable time	$\overline{nOE}$ to nAn	18.2	18.2	18.2	18.2	18.2	18.2	ns
		$\overline{nOE}$ to nBn	19.2	10.7	9.8	9.6	9.7	10.2	ns

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

**Table 12. Typical dynamic characteristics at  $V_{CC(B)} = 0.8\text{ V}$  and  $T_{amb} = 25\text{ °C}$**

*Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 9](#); for wave forms see [Figure 7](#) and [Figure 8](#)*

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$t_{pd}$	propagation delay	nAn to nBn	14.5	12.7	12.4	12.3	12.1	12.0	ns
		nBn to nAn	14.5	7.3	6.5	6.2	5.9	6.0	ns
$t_{dis}$	disable time	$\overline{nOE}$ to nAn	14.3	5.5	4.1	4.0	3.0	3.5	ns
		$\overline{nOE}$ to nBn	17.0	13.8	13.4	13.1	12.9	12.7	ns
$t_{en}$	enable time	$\overline{nOE}$ to nAn	18.2	5.6	4.0	3.2	2.4	2.2	ns
		$\overline{nOE}$ to nBn	19.2	14.6	14.1	13.9	13.7	13.6	ns

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

**Table 13. Dynamic characteristics for temperature range –40 °C to +85 °C [1]**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 9](#); for wave forms see [Figure 7](#) and [Figure 8](#).

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
<b>V<sub>CC(A)</sub> = 1.1 V to 1.3 V</b>													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	9.4	0.5	7.1	0.5	6.2	0.5	5.2	0.5	5.1	ns
		nBn to nAn	0.5	9.4	0.5	8.9	0.5	8.7	0.5	8.4	0.5	8.2	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.8	10.9	1.8	10.9	1.8	10.9	1.8	10.9	1.8	10.9	ns
		n $\overline{\text{OE}}$ to nBn	1.9	12.4	1.9	9.6	1.9	9.5	1.4	8.1	1.2	9.1	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.4	12.8	1.4	12.8	1.4	12.8	1.4	12.8	1.4	12.8	ns
		n $\overline{\text{OE}}$ to nBn	1.1	13.3	1.1	10.0	1.1	8.9	1.0	7.9	1.0	7.7	ns
<b>V<sub>CC(A)</sub> = 1.4 V to 1.6 V</b>													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.3	8.9	0.3	6.3	0.3	5.2	0.3	4.2	0.3	4.2	ns
		nBn to nAn	0.7	7.1	0.7	6.3	0.5	6.0	0.4	5.7	0.3	5.6	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.8	10.2	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	ns
		n $\overline{\text{OE}}$ to nBn	1.9	11.3	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.1	9.4	1.4	9.4	1.1	9.4	0.7	9.4	0.4	9.4	ns
		n $\overline{\text{OE}}$ to nBn	1.4	12.1	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	ns
<b>V<sub>CC(A)</sub> = 1.65 V to 1.95 V</b>													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.1	8.7	0.1	6.0	0.1	4.9	0.1	3.9	0.3	3.9	ns
		nBn to nAn	0.6	6.2	0.6	5.3	0.5	4.9	0.3	4.6	0.3	4.5	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.8	8.6	1.6	8.6	1.8	8.6	1.3	8.6	1.6	8.6	ns
		n $\overline{\text{OE}}$ to nBn	1.7	10.9	1.7	9.9	1.6	8.7	1.2	6.9	1.0	6.9	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.0	7.2	1.0	7.2	1.0	7.2	0.6	7.2	0.4	7.2	ns
		n $\overline{\text{OE}}$ to nBn	1.2	11.7	1.2	9.2	1.0	7.4	0.8	5.3	0.8	4.6	ns
<b>V<sub>CC(A)</sub> = 2.3 V to 2.7 V</b>													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.1	8.4	0.1	5.7	0.1	4.6	0.2	3.5	0.1	3.6	ns
		nBn to nAn	0.6	5.2	0.6	4.2	0.4	3.9	0.2	3.4	0.2	3.3	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.0	6.2	1.0	6.2	1.0	6.2	1.0	6.2	1.0	6.2	ns
		n $\overline{\text{OE}}$ to nBn	1.5	10.4	1.5	8.8	1.3	8.2	1.1	6.2	0.9	5.2	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	0.7	4.8	0.7	4.8	0.7	4.8	0.6	4.8	0.4	4.8	ns
		n $\overline{\text{OE}}$ to nBn	0.9	11.3	0.9	8.8	0.8	7.0	0.6	4.8	0.6	4.0	ns
<b>V<sub>CC(A)</sub> = 3.0 V to 3.6 V</b>													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.1	8.2	0.1	5.6	0.1	4.5	0.1	3.3	0.1	2.9	ns
		nBn to nAn	0.6	5.1	0.6	4.2	0.4	3.4	0.2	3.0	0.1	2.8	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	0.7	5.6	0.7	5.6	0.7	5.6	0.7	5.6	0.7	5.6	ns
		n $\overline{\text{OE}}$ to nBn	1.4	10.2	1.4	9.3	1.2	8.1	1.0	6.4	0.8	6.2	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	0.6	3.8	0.6	3.8	0.6	3.8	0.6	3.8	0.4	3.8	ns
		n $\overline{\text{OE}}$ to nBn	0.8	11.3	0.8	8.7	0.6	6.8	0.5	4.7	0.5	3.8	ns

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

**Table 14. Dynamic characteristics for temperature range –40 °C to +125 °C [1]**

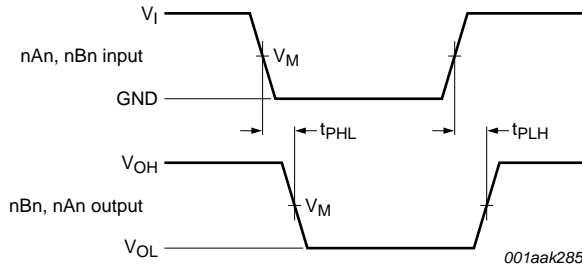
Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 9](#); for wave forms see [Figure 7](#) and [Figure 8](#)

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
<b>V<sub>CC(A)</sub> = 1.1 V to 1.3 V</b>													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	10.4	0.5	7.9	0.5	6.9	0.5	5.8	0.5	5.7	ns
		nBn to nAn	0.5	10.4	0.5	9.8	0.5	9.6	0.5	9.3	0.5	9.1	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.8	12.0	1.8	12.0	1.8	12.0	1.8	12.0	1.8	12.0	ns
		n $\overline{\text{OE}}$ to nBn	1.9	13.7	1.9	10.6	1.9	10.5	1.4	9.0	1.2	10.1	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.4	14.1	1.4	14.1	1.4	14.1	1.4	14.1	1.4	14.1	ns
		n $\overline{\text{OE}}$ to nBn	1.1	14.7	1.1	11.0	1.1	9.8	1.0	8.7	1.0	8.5	ns
<b>V<sub>CC(A)</sub> = 1.4 V to 1.6 V</b>													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.3	9.8	0.3	7.0	0.3	5.8	0.3	4.7	0.3	4.7	ns
		nBn to nAn	0.7	7.9	0.7	7.0	0.5	6.6	0.4	6.3	0.3	6.2	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.8	11.3	1.8	11.3	1.5	11.3	1.3	11.3	1.6	11.3	ns
		n $\overline{\text{OE}}$ to nBn	1.9	12.5	1.9	11.4	1.9	10.1	1.4	8.2	1.2	8.4	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.1	10.4	1.4	10.4	1.1	10.4	0.7	10.4	0.4	10.4	ns
		n $\overline{\text{OE}}$ to nBn	1.4	13.3	1.4	10.6	1.1	8.5	0.9	6.4	0.9	6.2	ns
<b>V<sub>CC(A)</sub> = 1.65 V to 1.95 V</b>													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.1	9.6	0.1	6.6	0.1	5.4	0.1	4.3	0.3	4.3	ns
		nBn to nAn	0.6	6.9	0.6	5.9	0.5	5.4	0.3	5.1	0.3	5.0	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.8	9.5	1.6	9.5	1.8	9.5	1.3	9.5	1.6	9.5	ns
		n $\overline{\text{OE}}$ to nBn	1.7	12.0	1.7	10.9	1.6	9.6	1.2	7.6	1.0	7.6	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.0	8.0	1.0	8.0	1.0	8.0	0.6	8.0	0.4	8.0	ns
		n $\overline{\text{OE}}$ to nBn	1.2	12.9	1.2	10.2	1.0	8.2	0.8	5.9	0.8	5.1	ns
<b>V<sub>CC(A)</sub> = 2.3 V to 2.7 V</b>													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.1	9.3	0.1	6.3	0.1	5.1	0.2	4.0	0.1	4.0	ns
		nBn to nAn	0.6	5.8	0.6	4.7	0.4	4.3	0.2	3.9	0.2	3.8	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.0	6.9	1.0	6.9	1.0	6.9	1.0	6.9	1.0	6.9	ns
		n $\overline{\text{OE}}$ to nBn	1.5	11.5	1.5	10.4	1.3	9.1	1.1	6.9	0.9	5.8	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	0.7	5.3	0.7	5.3	0.7	5.3	0.6	5.3	0.4	5.3	ns
		n $\overline{\text{OE}}$ to nBn	0.9	12.4	0.9	9.7	0.8	7.7	0.6	5.3	0.6	4.4	ns
<b>V<sub>CC(A)</sub> = 3.0 V to 3.6 V</b>													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.1	9.1	0.1	6.2	0.1	5.0	0.1	3.8	0.1	3.3	ns
		nBn to nAn	0.6	5.7	0.6	4.7	0.4	3.9	0.2	3.4	0.1	3.3	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	0.7	6.2	0.7	6.2	0.7	6.2	0.7	6.2	0.7	6.2	ns
		n $\overline{\text{OE}}$ to nBn	1.4	11.3	1.4	10.3	1.2	9.0	1.0	7.1	0.8	6.9	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	0.6	4.2	0.6	4.2	0.6	4.2	0.6	4.2	0.4	4.2	ns
		n $\overline{\text{OE}}$ to nBn	0.8	12.4	0.8	9.6	0.6	7.5	0.5	5.2	0.5	4.2	ns

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

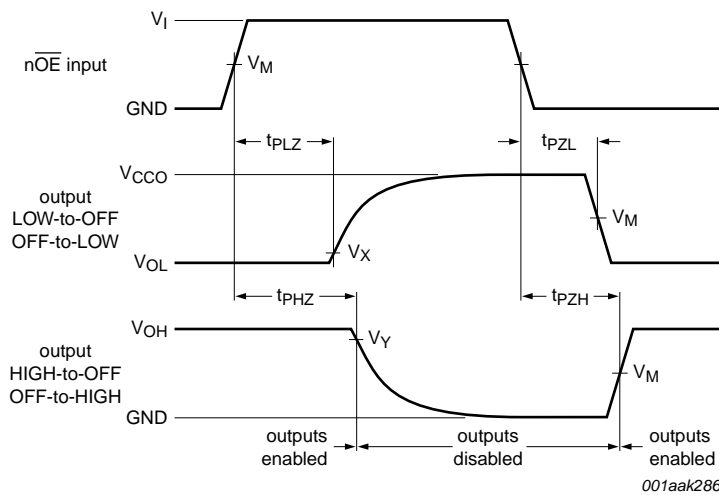


12. Waveforms



Measurement points are given in [Table 15](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 7. The data input (nAn, nBn) to output (nBn, nAn) propagation delay times**



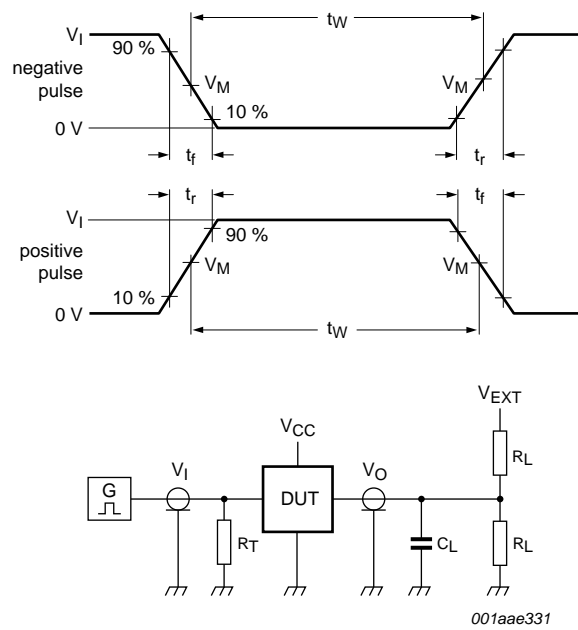
Measurement points are given in [Table 15](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 8. Enable and disable times**

**Table 15. Measurement points**

Supply voltage	Input <sup>[1]</sup>	Output <sup>[2]</sup>		
$V_{CC(A)}, V_{CC(B)}$	$V_M$	$V_M$	$V_X$	$V_Y$
0.8 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1 V$	$V_{OH} - 0.1 V$
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
3.0 V to 3.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

[1]  $V_{CCI}$  is the supply voltage associated with the data input port.  
 [2]  $V_{CCO}$  is the supply voltage associated with the output port.



Test data is given in [Table 16](#).  
 $R_L$  = Load resistance.  
 $C_L$  = Load capacitance including jig and probe capacitance.  
 $R_T$  = Termination resistance.  
 $V_{EXT}$  = External voltage for measuring switching times.

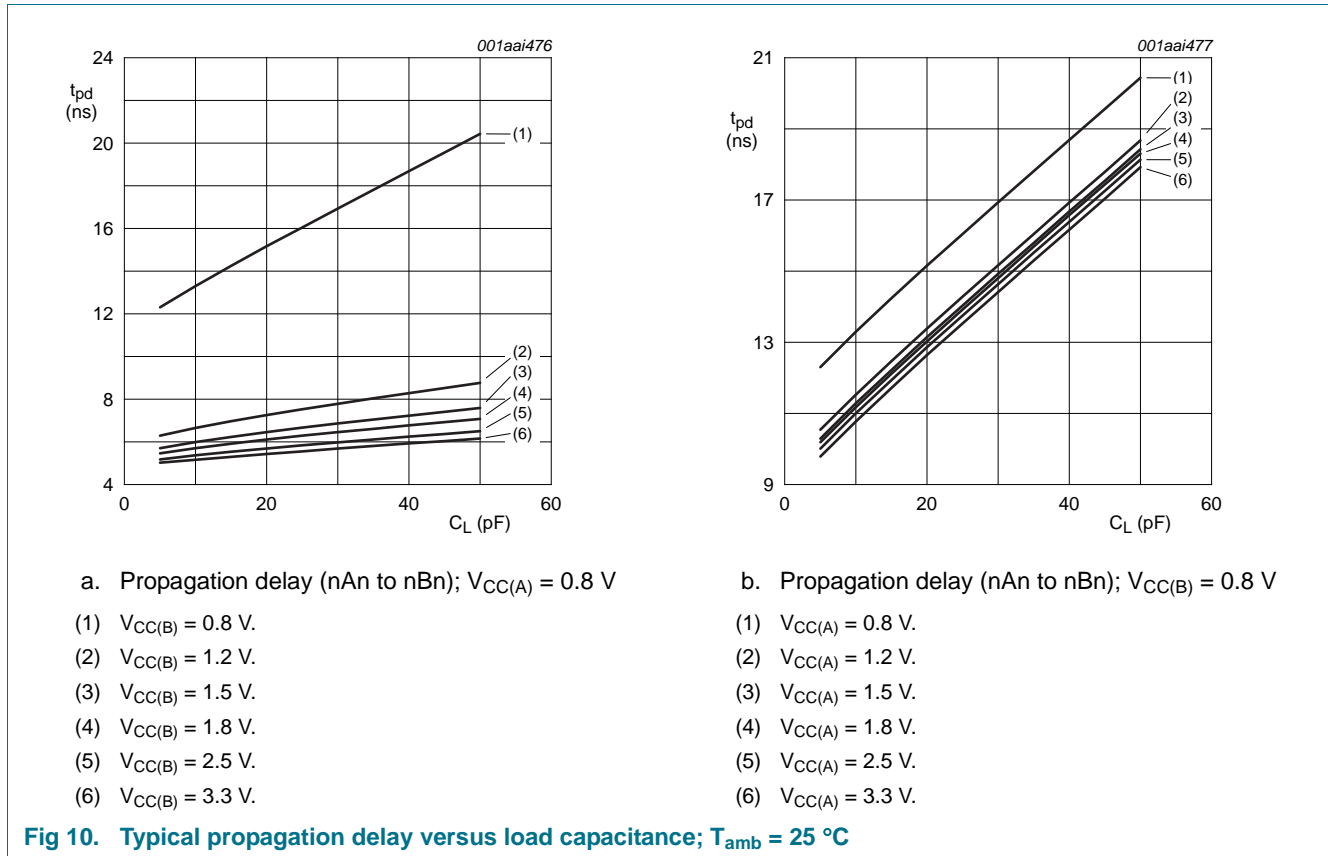
**Fig 9. Test circuit for measuring switching times**

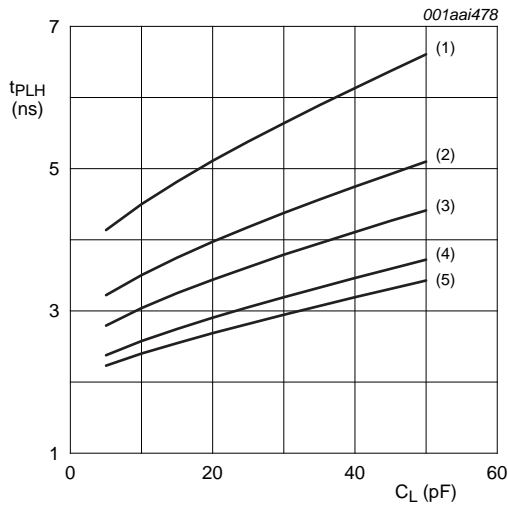
**Table 16. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_{CC(A)}$ , $V_{CC(B)}$	$V_I$ <sup>[1]</sup>	$\Delta t/\Delta V$ <sup>[2]</sup>	$C_L$	$R_L$	$t_{PLH}$ , $t_{PHL}$	$t_{PZH}$ , $t_{PHZ}$
0.8 V to 1.6 V	$V_{CCI}$	$\leq 1.0$ ns/V	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$
1.65 V to 2.7 V	$V_{CCI}$	$\leq 1.0$ ns/V	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$
3.0 V to 3.6 V	$V_{CCI}$	$\leq 1.0$ ns/V	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$

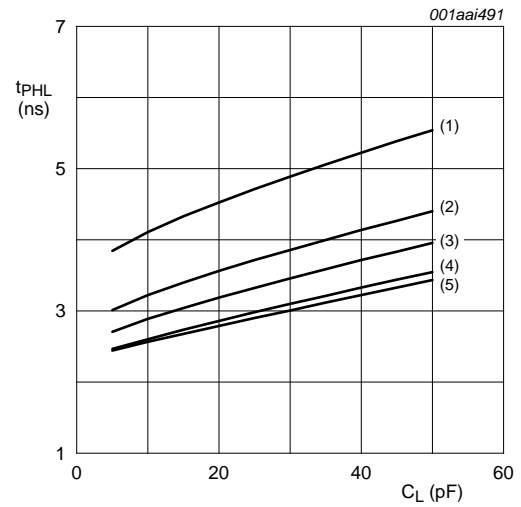
- [1]  $V_{CCI}$  is the supply voltage associated with the data input port.
- [2]  $dV/dt \geq 1.0$  V/ns
- [3]  $V_{CCO}$  is the supply voltage associated with the output port.

### 13. Typical propagation delay characteristics

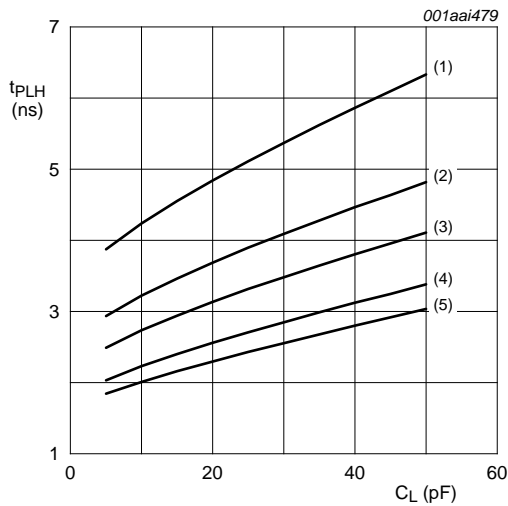




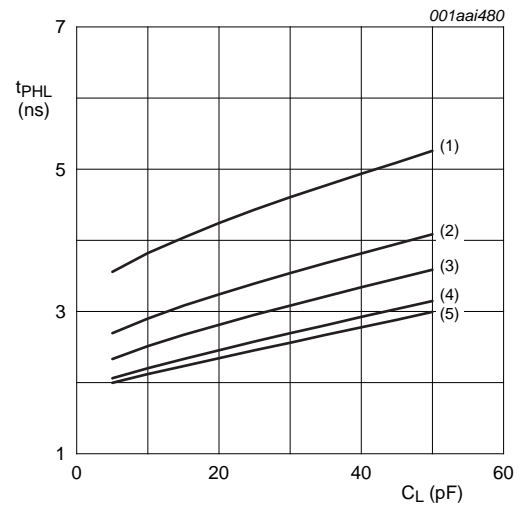
a. LOW to HIGH propagation delay (nAn to nBn);  
 $V_{CC(A)} = 1.2\text{ V}$



b. HIGH to LOW propagation delay (nAn to nBn);  
 $V_{CC(A)} = 1.2\text{ V}$



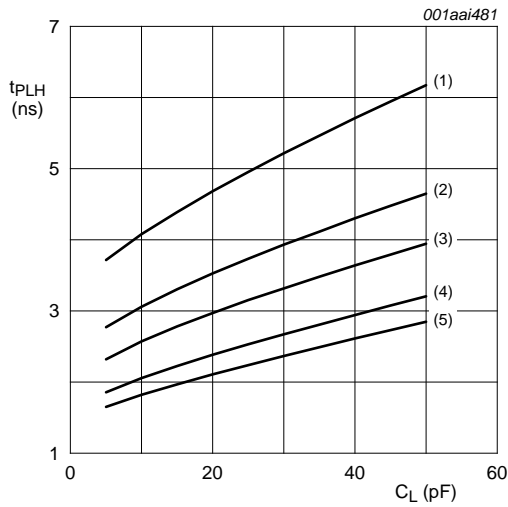
c. LOW to HIGH propagation delay (nAn to nBn);  
 $V_{CC(A)} = 1.5\text{ V}$



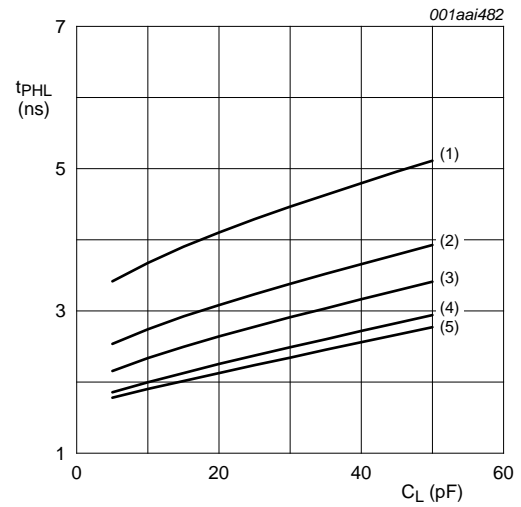
d. HIGH to LOW propagation delay (nAn to nBn);  
 $V_{CC(A)} = 1.5\text{ V}$

- (1)  $V_{CC(B)} = 1.2\text{ V}$ .
- (2)  $V_{CC(B)} = 1.5\text{ V}$ .
- (3)  $V_{CC(B)} = 1.8\text{ V}$ .
- (4)  $V_{CC(B)} = 2.5\text{ V}$ .
- (5)  $V_{CC(B)} = 3.3\text{ V}$ .

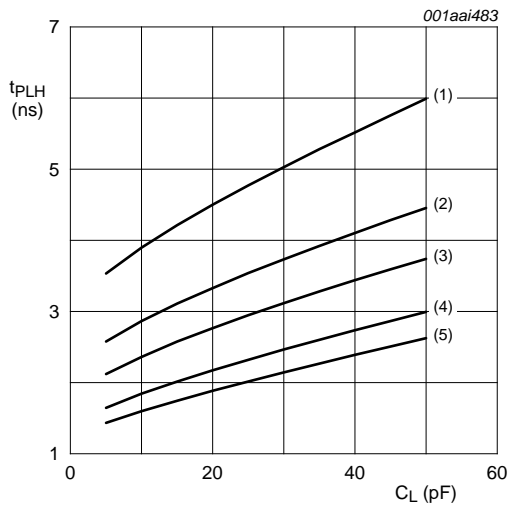
Fig 11. Typical propagation delay versus load capacitance;  $T_{amb} = 25\text{ }^\circ\text{C}$



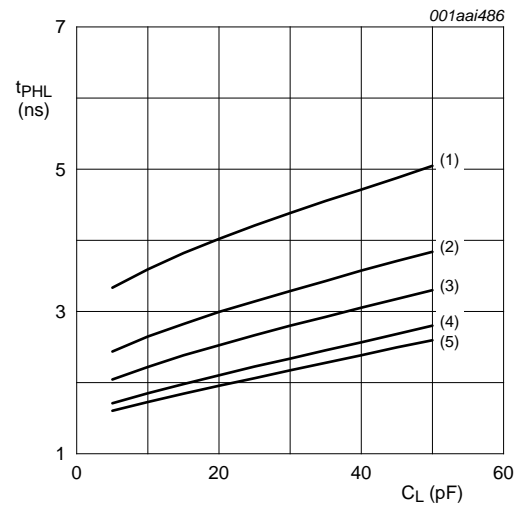
a. LOW to HIGH propagation delay (nAn to nBn);  
V<sub>CC(A)</sub> = 1.8 V



b. HIGH to LOW propagation delay (nAn to nBn);  
V<sub>CC(A)</sub> = 1.8 V



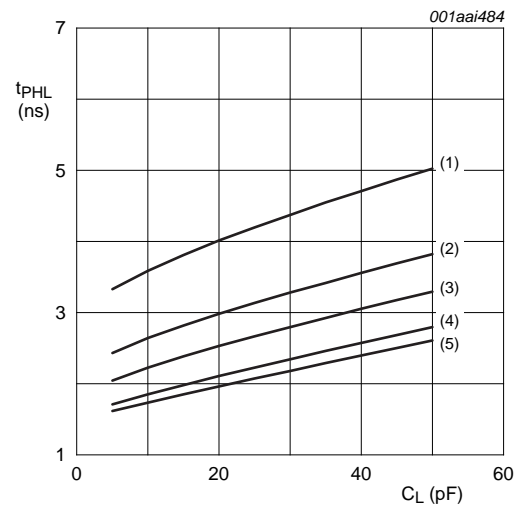
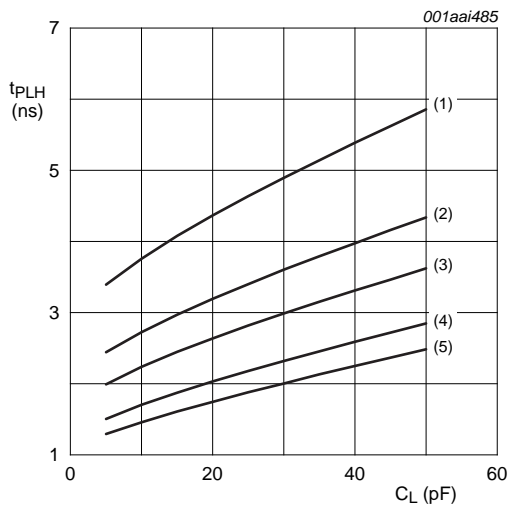
c. LOW to HIGH propagation delay (nAn to nBn);  
V<sub>CC(A)</sub> = 2.5 V



d. HIGH to LOW propagation delay (nAn to nBn);  
V<sub>CC(A)</sub> = 2.5 V

- (1) V<sub>CC(B)</sub> = 1.2 V.
- (2) V<sub>CC(B)</sub> = 1.5 V.
- (3) V<sub>CC(B)</sub> = 1.8 V.
- (4) V<sub>CC(B)</sub> = 2.5 V.
- (5) V<sub>CC(B)</sub> = 3.3 V.

Fig 12. Typical propagation delay versus load capacitance; T<sub>amb</sub> = 25 °C



a. LOW to HIGH propagation delay (nAn to nBn);  
 $V_{CC(A)} = 3.3 \text{ V}$

- (1)  $V_{CC(B)} = 1.2 \text{ V}$ .
- (2)  $V_{CC(B)} = 1.5 \text{ V}$ .
- (3)  $V_{CC(B)} = 1.8 \text{ V}$ .
- (4)  $V_{CC(B)} = 2.5 \text{ V}$ .
- (5)  $V_{CC(B)} = 3.3 \text{ V}$ .

b. HIGH to LOW propagation delay (nAn to nBn);  
 $V_{CC(A)} = 3.3 \text{ V}$

Fig 13. Typical propagation delay versus load capacitance;  $T_{amb} = 25 \text{ }^\circ\text{C}$

14. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

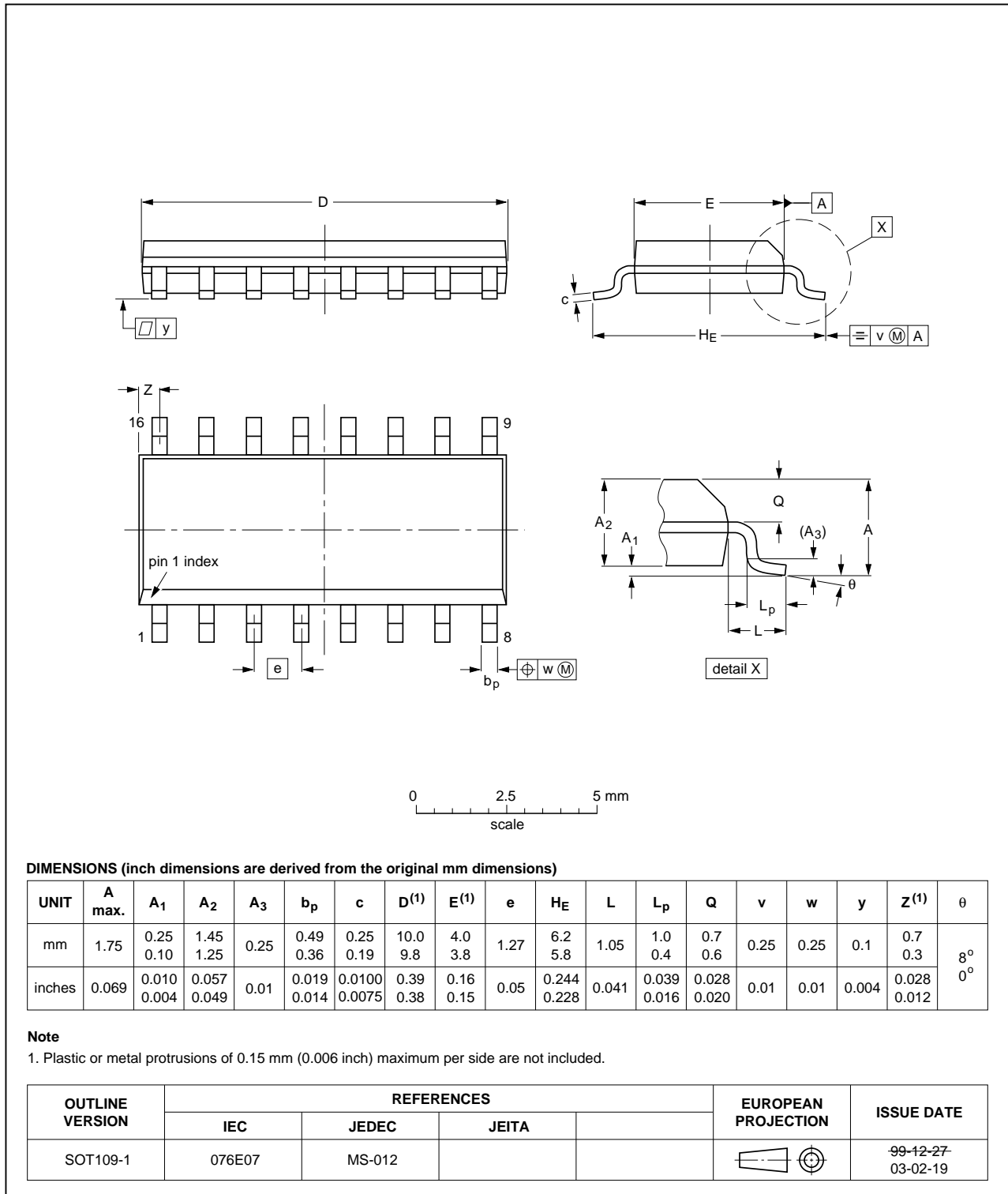


Fig 14. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

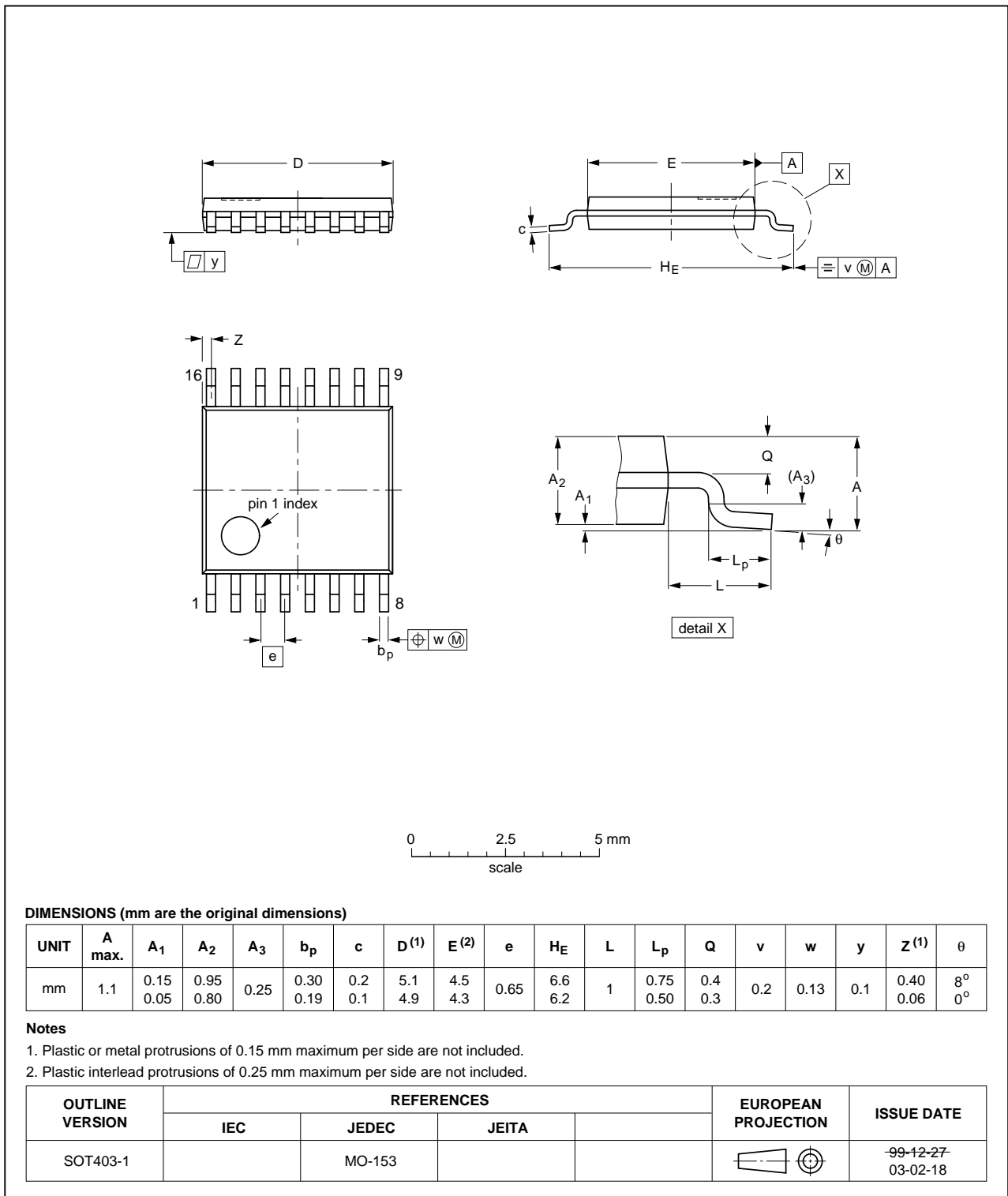


Fig 15. Package outline SOT403-1 (TSSOP16)



DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

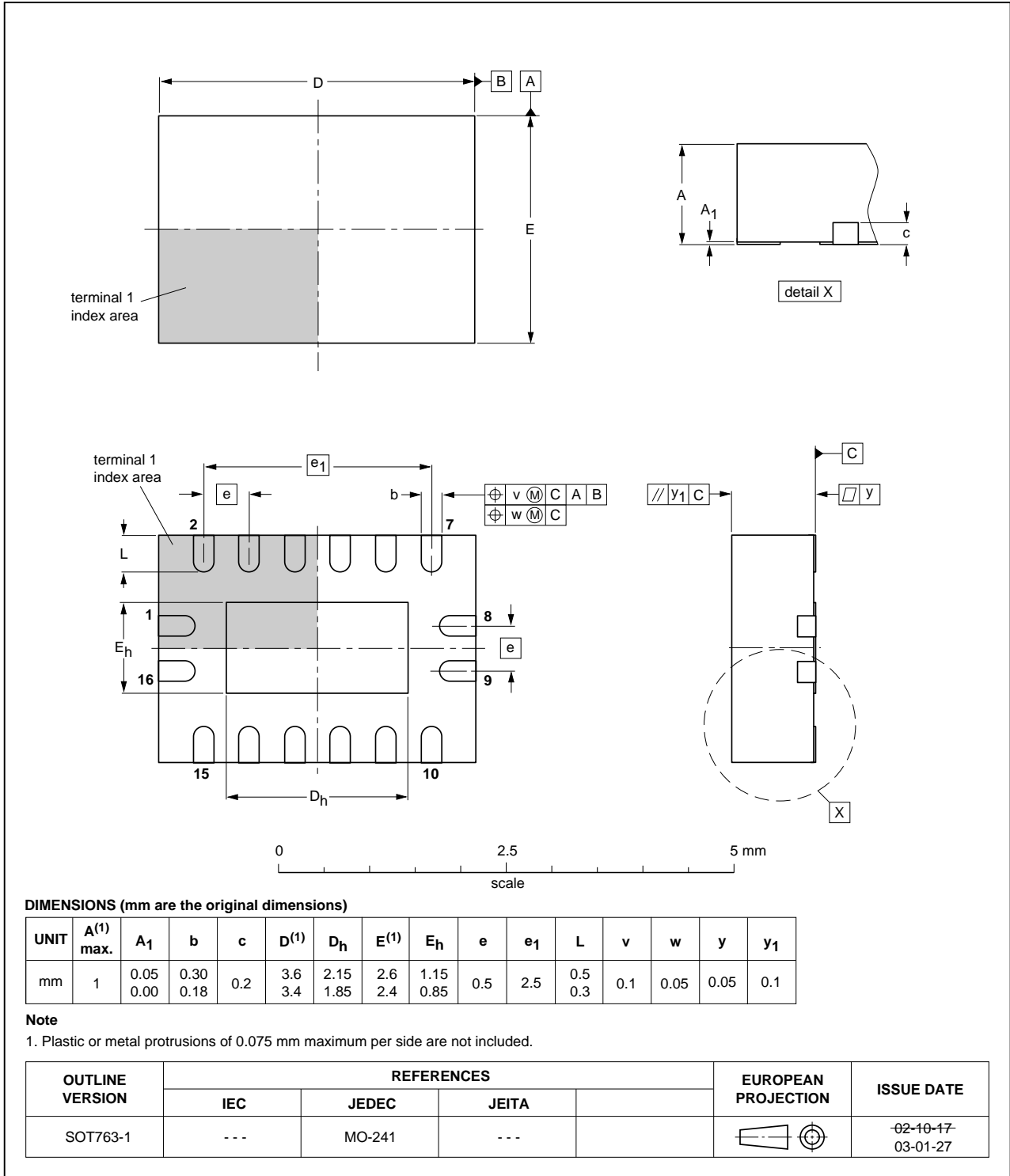


Fig 16. Package outline SOT763-1 (DHVQFN16)

XQFN16: plastic, extremely thin quad flat package; no leads; 16 terminals; body 1.80 x 2.60 x 0.50 mm

SOT1161-1

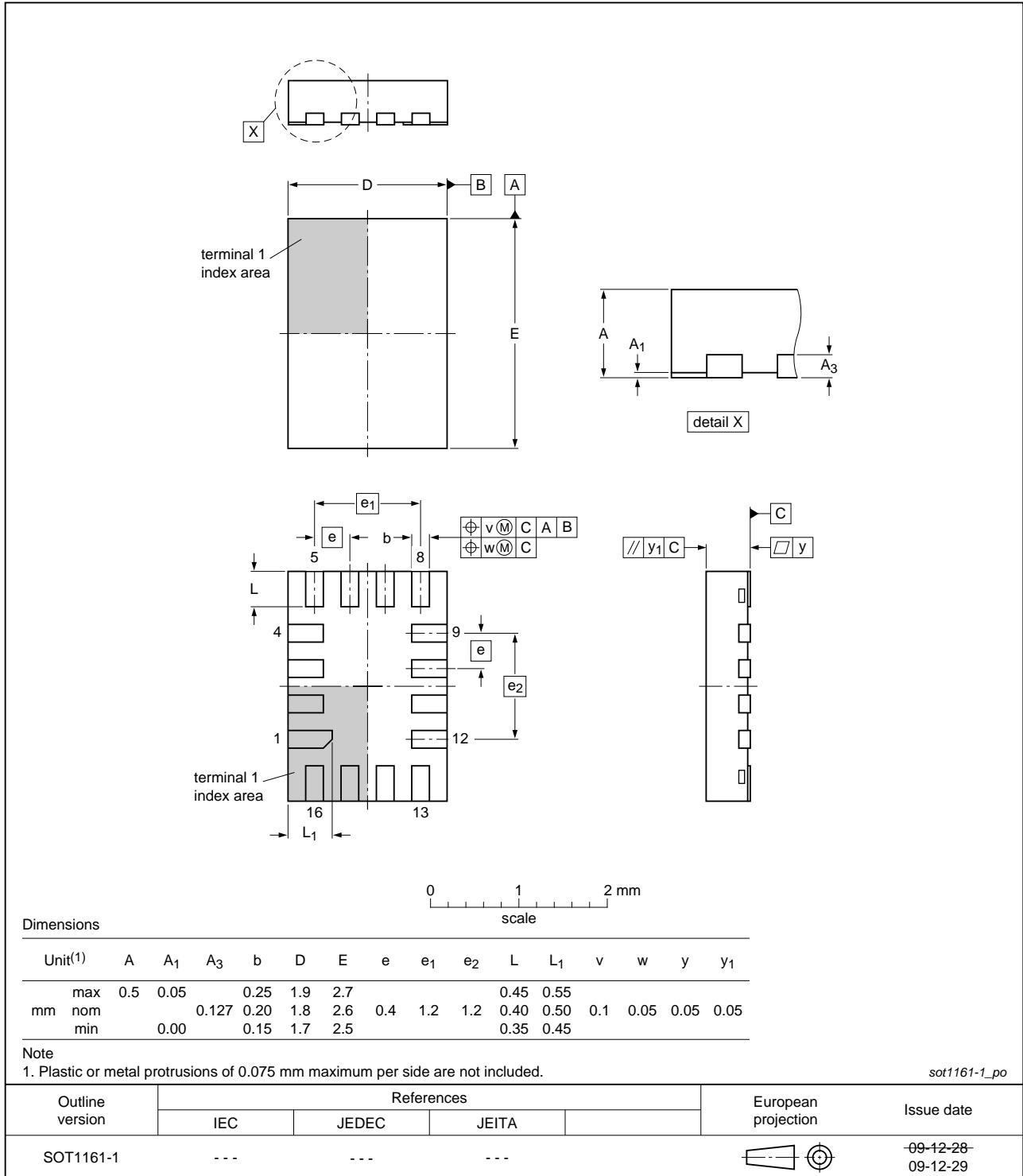


Fig 17. Package outline SOT1161-1 (XQFN16)

## 15. Abbreviations

Table 17. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 16. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVCH4T245 v.5	20151217	Product data sheet	-	74AVCH4T245 v.4
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Table 5</a>: conditions I<sub>CC</sub> and I<sub>GND</sub> changed (errata).</li> </ul>			
74AVCH4T245 v.4	20111214	Product data sheet	-	74AVCH4T245 v.3
Modifications:	<ul style="list-style-type: none"> <li>• Legal pages updated.</li> </ul>			
74AVCH4T245 v.3	20110927	Product data sheet	-	74AVCH4T245 v.2
74AVCH4T245 v.2	20101203	Product data sheet	-	74AVCH4T245 v.1
74AVCH4T245 v.1	20090806	Product data sheet	-	-

## 17. Legal information

### 17.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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19. Contents

1 General description ..... 1

2 Features and benefits ..... 1

3 Ordering information ..... 2

4 Marking ..... 2

5 Functional diagram ..... 3

6 Pinning information ..... 4

6.1 Pinning ..... 4

6.2 Pin description ..... 5

7 Functional description ..... 5

8 Limiting values ..... 6

9 Recommended operating conditions ..... 6

10 Static characteristics ..... 7

11 Dynamic characteristics ..... 12

12 Waveforms ..... 16

13 Typical propagation delay characteristics .. 18

14 Package outline ..... 22

15 Abbreviations ..... 26

16 Revision history ..... 26

17 Legal information ..... 27

17.1 Data sheet status ..... 27

17.2 Definitions ..... 27

17.3 Disclaimers ..... 27

17.4 Trademarks ..... 28

18 Contact information ..... 28

19 Contents ..... 29

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Date of release: 17 December 2015  
 Document identifier: 74AVCH4T245