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## 74LVT16374 • 74LVTH16374

### Low Voltage 16-Bit D-Type Flip-Flop with 3-STATE Outputs

#### General Description

The LVT16374 and LVTH16374 contain sixteen non-inverting D-type flip-flops with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable ( $\overline{OE}$ ) are common to each byte and can be shorted together for full 16-bit operation.

The LVTH16374 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These flip-flops are designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16374 and LVTH16374 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

#### Features

- Input and output interface capability to systems at 5V  $V_{CC}$
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH16374), also available without bushold feature (74LVT16374)
- Live insertion/extraction permitted
- Power Up/Power Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Functionally compatible with the 74 series 16374
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human-body model > 2000V
  - Machine model > 200V
  - Charged-device model > 1000V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

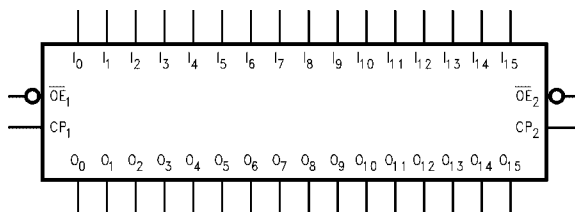
#### Ordering Code:

Order Number	Package Number	Package Description
74LVT16374G (Note 1)(Note 2)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LVT16374MEA (Note 2)	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LVT16374MTD (Note 2)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
74LVTH16374G (Note 1)(Note 2)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LVTH16374MEA (Note 2)	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LVTH16374MTD (Note 2)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

**Note 1:** Ordering code "G" indicates Trays.

**Note 2:** Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

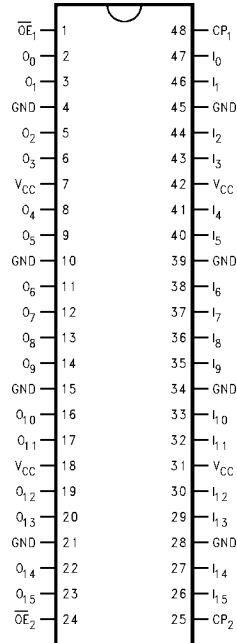
#### Logic Symbol



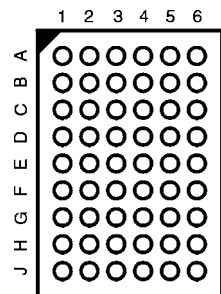
74LVT16374 • 74LVTH16374 Low Voltage 16-Bit D-Type Flip-Flop with 3-STATE Outputs

## Connection Diagrams

Pin Assignment for SSOP and TSSOP



Pin Assignment for FBGA



(Top Thru View)

## Functional Description

The LVT16374 and LVTH16374 consist of sixteen edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte.

## Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$CP_n$	Clock Pulse Input
$I_0-I_{15}$	Inputs
$O_0-O_{15}$	3-STATE Outputs
NC	No Connect

## FBGA Pin Assignments

	1	2	3	4	5	6
<b>A</b>	$O_0$	NC	$\overline{OE}_1$	$CP_1$	NC	$I_0$
<b>B</b>	$O_2$	$O_1$	NC	NC	$I_1$	$I_2$
<b>C</b>	$O_4$	$O_3$	$V_{CC}$	$V_{CC}$	$I_3$	$I_4$
<b>D</b>	$O_6$	$O_5$	GND	GND	$I_5$	$I_6$
<b>E</b>	$O_8$	$O_7$	GND	GND	$I_7$	$I_8$
<b>F</b>	$O_{10}$	$O_9$	GND	GND	$I_9$	$I_{10}$
<b>G</b>	$O_{12}$	$O_{11}$	$V_{CC}$	$V_{CC}$	$I_{11}$	$I_{12}$
<b>H</b>	$O_{14}$	$O_{13}$	NC	NC	$I_{13}$	$I_{14}$
<b>J</b>	$O_{15}$	NC	$\overline{OE}_2$	$CP_2$	NC	$I_{15}$

## Truth Tables

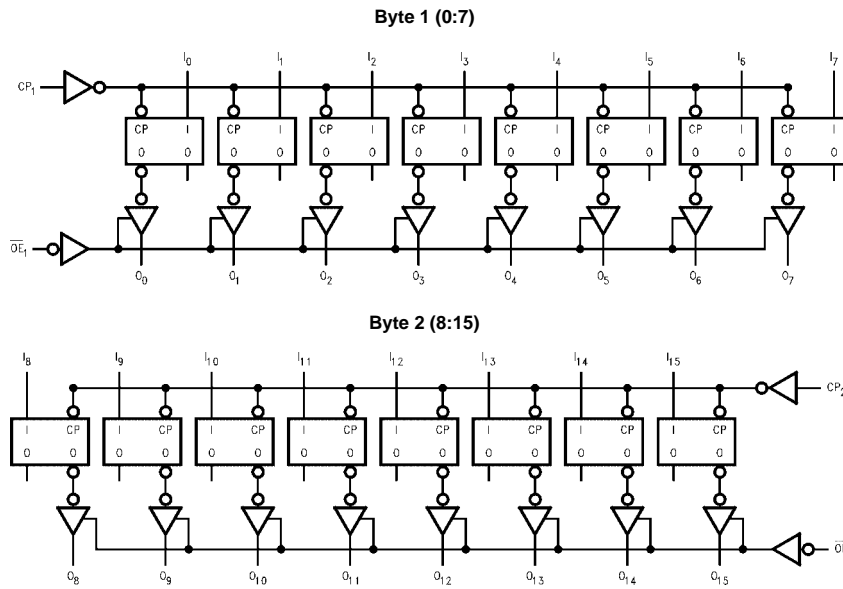
Inputs			Outputs
$CP_1$	$\overline{OE}_1$	$I_0-I_7$	$O_0-O_7$
↗	L	H	H
↗	L	L	L
L	L	X	$O_0$
X	H	X	Z

Inputs			Outputs
$CP_2$	$\overline{OE}_2$	$I_8-I_{15}$	$O_8-O_{15}$
↗	L	H	H
↗	L	L	L
L	L	X	$O_0$
X	H	X	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = HIGH Impedance  
 $O_0$  = Previous  $O_0$  before HIGH to LOW of CP

Each flip-flop will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock ( $CP_n$ ) transition. With the Output Enable ( $\overline{OE}_n$ ) LOW, the contents of the flip-flops are available at the outputs. When  $\overline{OE}_n$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}_n$  input does not affect the state of the flip-flops.

**Logic Diagrams**



Please note that these diagrams are provided for the understanding of logic operation and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 3)

Symbol	Parameter	Value	Conditions	Units
$V_{CC}$	Supply Voltage	-0.5 to +4.6		V
$V_I$	DC Input Voltage	-0.5 to +7.0		V
$V_O$	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE	V
		-0.5 to +7.0	Output in High or Low State (Note 4)	
$I_{IK}$	DC Input Diode Current	-50	$V_I < \text{GND}$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < \text{GND}$	mA
$I_O$	DC Output Current	64	$V_O > V_{CC}$ Output at High State	mA
		128	$V_O > V_{CC}$ Output at Low State	
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 64$		mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 128$		mA
$T_{STG}$	Storage Temperature	-65 to +150		$^{\circ}\text{C}$

**Recommended Operating Conditions**

Symbol	Parameter	Min	Max	Units
$V_{CC}$	Supply Voltage	2.7	3.6	V
$V_I$	Input Voltage	0	5.5	V
$I_{OH}$	High-Level Output Current		-32	mA
$I_{OL}$	Low-Level Output Current		64	mA
$T_A$	Free-Air Operating Temperature	-40	85	$^{\circ}\text{C}$
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8\text{V}-2.0\text{V}$ , $V_{CC} = 3.0\text{V}$	0	10	ns/V

**Note 3:** Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

**Note 4:**  $I_O$  Absolute Maximum Rating must be observed.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		Units	Conditions	
			Min	Max			
$V_{IK}$	Input Clamp Diode Voltage	2.7		-1.2	V	$I_I = -18\text{ mA}$	
$V_{IH}$	Input HIGH Voltage	2.7-3.6	2.0		V	$V_O \leq 0.1\text{V}$ or $V_O \geq V_{CC} - 0.1\text{V}$	
$V_{IL}$	Input LOW Voltage	2.7-3.6		0.8			
$V_{OH}$	Output HIGH Voltage	2.7-3.6	$V_{CC} - 0.2$		V	$I_{OH} = -100\ \mu\text{A}$	
		2.7	2.4			$I_{OH} = -8\text{ mA}$	
		3.0	2.0			$I_{OH} = -32\text{ mA}$	
$V_{OL}$	Output LOW Voltage	2.7		0.2	V	$I_{OL} = 100\ \mu\text{A}$	
		2.7		0.5		$I_{OL} = 24\text{ mA}$	
		3.0		0.4		$I_{OL} = 16\text{ mA}$	
		3.0		0.5		$I_{OL} = 32\text{ mA}$	
		3.0		0.55		$I_{OL} = 64\text{ mA}$	
$I_{I(\text{HOLD})}$ (Note 5)	Bushold Input Minimum Drive	3.0	75		$\mu\text{A}$	$V_I = 0.8\text{V}$	
			-75			$V_I = 2.0\text{V}$	
$I_{I(\text{OD})}$ (Note 5)	Bushold Input Over-Drive Current to Change State	3.0	500		$\mu\text{A}$	(Note 6)	
			-500			(Note 7)	
$I_I$	Input Current	3.6		10	$\mu\text{A}$	$V_I = 5.5\text{V}$	
		Control Pins	3.6			$\pm 1$	$V_I = 0\text{V}$ or $V_{CC}$
			Data Pins	3.6			-5
				1		$V_I = V_{CC}$	
$I_{OFF}$	Power Off Leakage Current	0		$\pm 100$	$\mu\text{A}$	$0\text{V} \leq V_I$ or $V_O \leq 5.5\text{V}$	
$I_{PU/PD}$	Power Up/Down 3-STATE Output Current	0-1.5V		$\pm 100$	$\mu\text{A}$	$V_O = 0.5\text{V}$ to $3.0\text{V}$ $V_I = \text{GND}$ or $V_{CC}$	
$I_{OZL}$	3-STATE Output Leakage Current	3.6		-5	$\mu\text{A}$	$V_O = 0.5\text{V}$	
$I_{OZH}$	3-STATE Output Leakage Current	3.6		5	$\mu\text{A}$	$V_O = 3.0\text{V}$	
$I_{OZH+}$	3-STATE Output Leakage Current	3.6		10	$\mu\text{A}$	$V_{CC} < V_O \leq 5.5\text{V}$	

**DC Electrical Characteristics** (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Min	Max		
I <sub>CCH</sub>	Power Supply Current	3.6		0.19	mA	Outputs HIGH
I <sub>CCL</sub>	Power Supply Current	3.6		5	mA	Outputs LOW
I <sub>CCZ</sub>	Power Supply Current	3.6		0.19	mA	Outputs Disabled
I <sub>CCZ+</sub>	Power Supply Current	3.6		0.19	mA	V <sub>CC</sub> ≤ V <sub>O</sub> ≤ 5.5V, Outputs Disabled
ΔI <sub>CC</sub>	Increase in Power Supply Current (Note 8)	3.6		0.2	mA	One Input at V <sub>CC</sub> - 0.6V Other Inputs at V <sub>CC</sub> or GND

**Note 5:** Applies to bushold versions only (74LVTH16374).

**Note 6:** An external driver must source at least the specified current to switch from LOW-to-HIGH.

**Note 7:** An external driver must sink at least the specified current to switch from HIGH-to-LOW.

**Note 8:** This is the increase in supply current for each input that is at the specified voltage level rather than V<sub>CC</sub> or GND.

**Dynamic Switching Characteristics** (Note 9)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			Units	Conditions C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω
			Min	Typ	Max		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3		0.8		V	(Note 10)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3		-0.8		V	(Note 10)

**Note 9:** Characterized in SSOP package. Guaranteed parameter, but not tested.

**Note 10:** Max number of outputs defined as (n), n-1 data inputs are driven 0V to 3V. Output under test held LOW.

**AC Electrical Characteristics**

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω				Units
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		
		Min	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	160		160		MHz
t <sub>PHL</sub>	Propagation Delay	1.9	4.3	1.9	4.6	ns
t <sub>PLH</sub>	CP to O <sub>n</sub>	1.6	4.5	1.6	5.2	ns
t <sub>PZL</sub>	Output Enable Time	1.3	4.4	1.3	5.0	ns
t <sub>PZH</sub>		1.0	4.5	1.0	5.4	ns
t <sub>PLZ</sub>	Output Disable Time	1.5	4.6	1.5	4.8	ns
t <sub>PHZ</sub>		2.0	5.0	2.0	5.4	ns
t <sub>S</sub>	Setup Time	1.8		2.0		ns
t <sub>H</sub>	Hold Time	0.8		0.1		ns
t <sub>W</sub>	Pulse Width	3.0		3.0		ns
t <sub>OSSL</sub>	Output to Output Skew (Note 11)		1.0		1.0	ns
t <sub>OSLH</sub>			1.0		1.0	ns

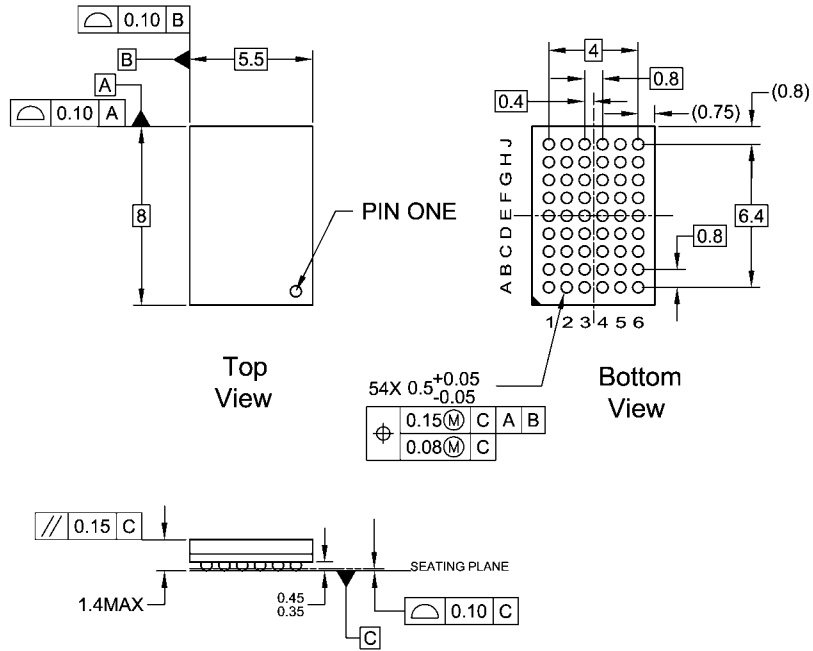
**Note 11:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSSL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

**Capacitance** (Note 12)

Symbol	Parameter	Conditions	Typical	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = Open, V <sub>I</sub> = 0V or V <sub>CC</sub>	4	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 3.0V, V <sub>O</sub> = 0V or V <sub>CC</sub>	8	pF

**Note 12:** Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

**Physical Dimensions** inches (millimeters) unless otherwise noted



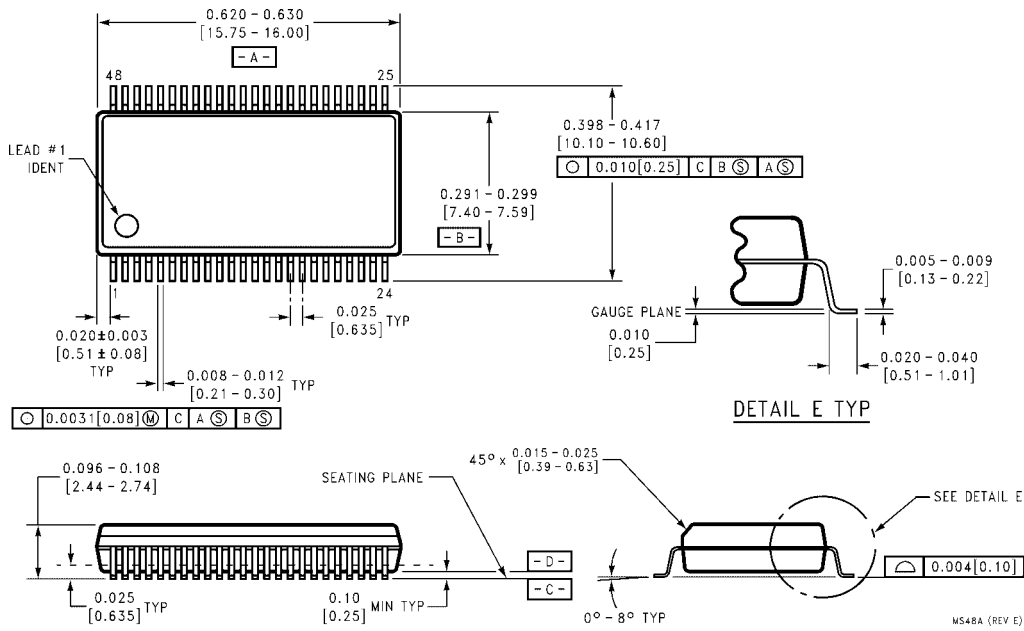
**NOTES:**

- A. THIS PACKAGE CONFORMS TO JEDEC MO-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)  
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide  
Package Number BGA54A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide  
Package Number MS48A**

MS48A (REV E)



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



MTD48REV C

**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48**

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