# Buffered 2:1 TMDS Switch with Equalization

Data Sheet

# AD8194

## FEATURES

- 2 inputs, 1 output HDMI/DVI high speed signal switch
- Pin-to-pin compatible with the AD8193
- Enables HDMI 1.3-compliant receiver
  - 4 TMDS channels per input/output
    - Supports 250 Mbps to 2.25 Gbps data rates
    - Supports 25 MHz to 225 MHz pixel clocks
    - Fully buffered unidirectional inputs/outputs
    - Equalized inputs for operation with long HDMI cables (20 m at 2.25 Gbps)
    - Matched 50 Ω input and output on-chip terminations
    - Low added jitter
    - Single-supply operation (3.3 V)
- Standards compliant: HDMI receiver, DVI
- 32-lead, 5 mm × 5 mm, RoHS-compliant LFCSP

## APPLICATIONS

- Advanced television (HDTV) sets
- Multiple input displays
- Projectors
- A/V receivers
- Set-top boxes

## FUNCTIONAL BLOCK DIAGRAM

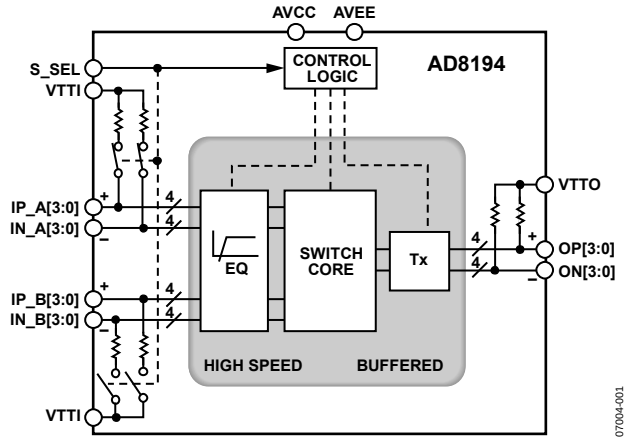



*Figure 1.*

## TYPICAL APPLICATION

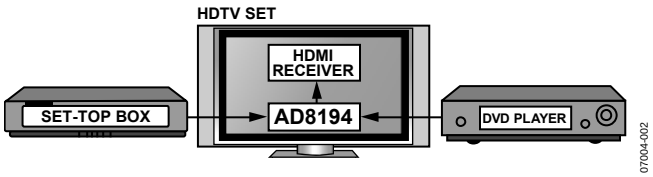



*Figure 2. Typical AD8194 Application for HDTV Sets*

## GENERAL DESCRIPTION

The AD8194 is a low cost quad 2:1 TMDS® switch for high speed HDMI™/DVI video applications. The AD8194 features equalized inputs, ideal for systems with long cable runs. Its primary function is to switch the high speed signals from one of two single-link (HDMI or DVI) sources to the single-link output. The AD8194 is a fully buffered switch solution with 50 Ω input and output terminations, providing full-swing output signal recovery and minimizing reflections for improved system signal integrity.

The AD8194 is provided in a space-saving, 32-lead, LFCSP, surface-mount, RoHS-compliant, plastic package and is specified to operate over the −40°C to +85°C temperature range.

## PRODUCT HIGHLIGHTS

1. Data supports rates up to 2.25 Gbps, enabling greater than 1080p deep color (12-bit color) HDMI formats and greater than UXGA (1600 × 2300) DVI resolutions.
2. Fully buffered inputs and outputs.
3. Input cable equalizer enables use of long cables at the input. For a typical 24 AWG cable, the AD8194 compensates for more than 20 m at data rates up to 2.25 Gbps.
4. Matched 50 Ω on-chip input and output terminations improve system signal integrity.
5. Single-pin source select bit.
6. Low added jitter.

Rev. A
Document Feedback


One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 
Technical Support www.analog.com

# AD8194* PRODUCT PAGE QUICK LINKS

Last Content Update: 10/20/2017

## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- AD8194 Evaluation Board

## DOCUMENTATION

**Data Sheet**

- AD8194: Buffered 2:1 TMDS Switch with Equalization Data Sheet

## REFERENCE MATERIALS

**Informational**

- Advantiv™ Advanced TV Solutions

**Technical Articles**

- Analysis of Common Failures of HDMI CT

## DESIGN RESOURCES

- AD8194 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all AD8194 EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK

Submit feedback for this data sheet.

# TABLE OF CONTENTS



## REVISION HISTORY

**10/2017—Rev. 0 to Rev. A**

Changed CP-32-8 to CP-32-21 ... Throughout
Changes to Figure 3 ... 5
Updated Outline Dimensions ... 16
Changes to Ordering Guide ... 16

**11/2007—Revision 0: Initial Version**

# SPECIFICATIONS

$T_A$ = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, AVEE = 0 V, differential input swing = 1000 mV, pattern = PRBS $2^7 - 1$, data rate = 2.25 Gbps, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

**Table 1.**

| Parameter | Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| Maximum Data Rate (DR) per Channel | NRZ | 2.25 | | | Gbps |
| Bit Error Rate (BER) | | | | $10^{-9}$ | |
| Added Deterministic Jitter | | | 10 | | ps (p-p) |
| Added Random Jitter | | | 1 | | ps (rms) |
| Differential Intrapair Skew | At output | | 1 | | ps |
| Differential Interpair Skew[1] | At output | | 30 | | ps |
| EQUALIZATION PERFORMANCE | | | | | |
| Receiver | Boost frequency = 1.125 GHz | | 12 | | dB |
| INPUT CHARACTERISTICS | | | | | |
| Input Voltage Swing | Differential | 150 | | 1200 | mV |
| Input Common-Mode Voltage ($V_{ICM}$) | | AVCC − 800 | | AVCC | mV |
| OUTPUT CHARACTERISTICS | | | | | |
| High Voltage Level | Single-ended high speed channel | | AVCC | | mV |
| Low Voltage Level | Single-ended high speed channel | AVCC − 600 | | AVCC − 400 | mV |
| Rise/Fall Time (20% to 80%) | | 75 | | 178 | ps |
| TERMINATION | | | | | |
| Input Resistance | Single-ended | | 50 | | Ω |
| Output Resistance | Single-ended | | 50 | | Ω |
| POWER SUPPLY | | | | | |
| AVCC | Operating range | 3 | 3.3 | 3.6 | V |
| QUIESCENT CURRENT[2] | | | | | |
| AVCC | | | 50 | 70 | mA |
| VTTI | | | 40 | 54 | mA |
| VTTO | | | 40 | 65 | mA |
| POWER DISSIPATION[3] | | | 429 | | mW |
| SOURCE SELECT INTERFACE | | | | | |
| Input High Voltage ($V_{IH}$) | S_SEL | 2 | | | V |
| Input Low Voltage ($V_{IL}$) | S_SEL | | | 0.8 | V |

[1] Differential interpair skew is measured between the TMDS pairs of a single link.
[2] Typical value assumes only the selected HDMI/DVI link is active with nominal signal swings and that the unselected HDMI/DVI link is deactivated. Minimum and maximum limits are measured at the respective extremes of input termination resistance and input voltage swing.
[3] The total power dissipation excludes power dissipated in the 50 Ω off-chip loads.

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| AVCC to AVEE | 3.7 V |
| VTTI | AVCC + 0.6 V |
| VTTO | AVCC + 0.6 V |
| Internal Power Dissipation | 1.2 W |
| High Speed Input Voltage | AVCC − 1.4 V < $V_{IN}$ < AVCC + 0.6 V |
| High Speed Differential Input Voltage | 2.0 V |
| Source Select (S_SEL) | AVEE − 0.3 V < $V_{IN}$ < AVCC + 0.6 V |
| Storage Temperature Range | −65°C to +125°C |
| Operating Temperature Range | −40°C to +85°C |
| Junction Temperature | 150°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions: a device soldered in a 4-layer JEDEC circuit board for surface-mount packages. $\theta_{JC}$ is specified for the exposed pad soldered to the circuit board with no airflow.

**Table 3. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 32-Lead LFCSP | 47 | 6.8 | °C/W |

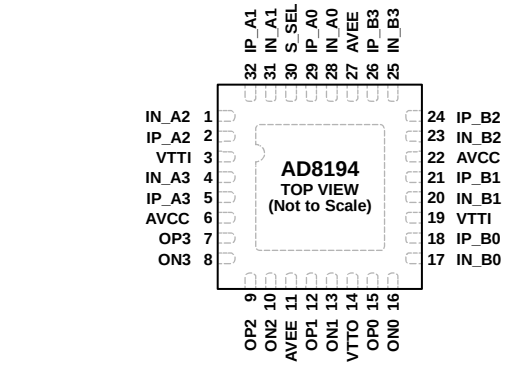
## MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8194 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure. To ensure proper operation, it is necessary to observe the maximum power derating as determined by the coefficients in Table 3.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS




NOTES
1. THE AD8194 LFCSP HAS AN EXPOSED PADDLE (ePAD) ON THE UNDERSIDE OF THE PACKAGE, WHICH AIDS IN HEAT DISSIPATION. THE ePAD MUST BE ELECTRICALLY CONNECTED TO THE AVEE SUPPLY PLANE TO MEET THERMAL SPECIFICATIONS.

07004-003

*Figure 3. Pin Configuration*

**Table 4. Pin Function Descriptions**

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 1 | IN_A2 | HS I | High Speed Input Complement. |
| 2 | IP_A2 | HS I | High Speed Input. |
| 3, 19 | VTTI | Power | Input Termination Supply. Nominally connected to AVCC. |
| 4 | IN_A3 | HS I | High Speed Input Complement. |
| 5 | IP_A3 | HS I | High Speed Input. |
| 6, 22 | AVCC | Power | Positive Power Supply. 3.3 V nominal. |
| 7 | OP3 | HS O | High Speed Output. |
| 8 | ON3 | HS O | High Speed Output Complement. |
| 9 | OP2 | HS O | High Speed Output. |
| 10 | ON2 | HS O | High Speed Output Complement. |
| 11, 27, ePAD | AVEE | Power | Negative Power Supply. 0 V nominal. |
| 12 | OP1 | HS O | High Speed Output. |
| 13 | ON1 | HS O | High Speed Output Complement. |
| 14 | VTTO | Power | Output Termination Supply. Nominally connected to AVCC. |
| 15 | OP0 | HS O | High Speed Output. |
| 16 | ON0 | HS O | High Speed Output Complement. |
| 17 | IN_B0 | HS I | High Speed Input Complement. |
| 18 | IP_B0 | HS I | High Speed Input. |
| 20 | IN_B1 | HS I | High Speed Input Complement. |
| 21 | IP_B1 | HS I | High Speed Input. |
| 23 | IN_B2 | HS I | High Speed Input Complement. |
| 24 | IP_B2 | HS I | High Speed Input. |
| 25 | IN_B3 | HS I | High Speed Input Complement. |
| 26 | IP_B3 | HS I | High Speed Input. |
| 28 | IN_A0 | HS I | High Speed Input Complement. |
| 29 | IP_A0 | HS I | High Speed Input. |
| 30 | S_SEL | Control | Source Selector Pin. |
| 31 | IN_A1 | HS I | High Speed Input Complement. |
| 32 | IP_A1 | HS I | High Speed Input. |

[1] HS = high speed, I = input, O = output.

# TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, AVEE = 0 V, differential input swing = 1000 mV, pattern = PRBS $2^7 - 1$, data rate = 2.25 Gbps, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

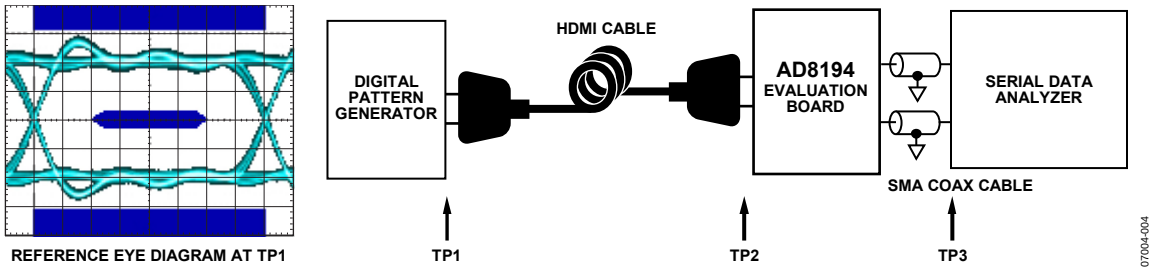



*Figure 4. Test Circuit Diagram for Rx Eye Diagrams*

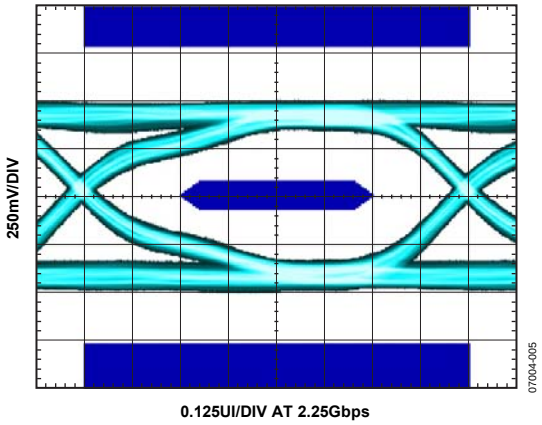



*Figure 5. Rx Eye Diagram at TP2 (Cable = 2 m, 30 AWG)*

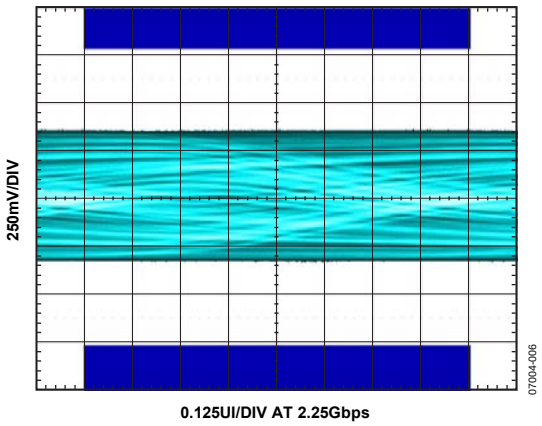



*Figure 6. Rx Eye Diagram at TP2 (Cable = 20 m, 24 AWG)*

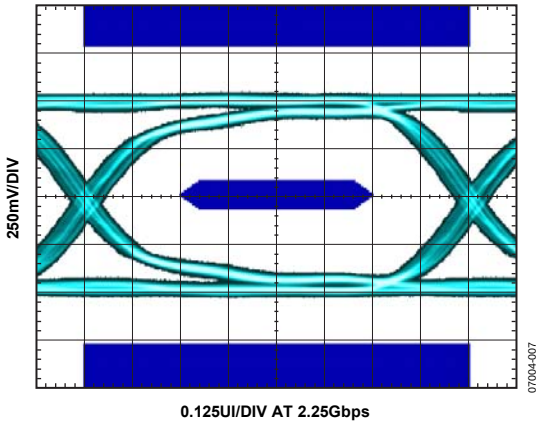



*Figure 7. Rx Eye Diagram at TP3, EQ = 12 dB (Cable = 2 m, 30 AWG)*

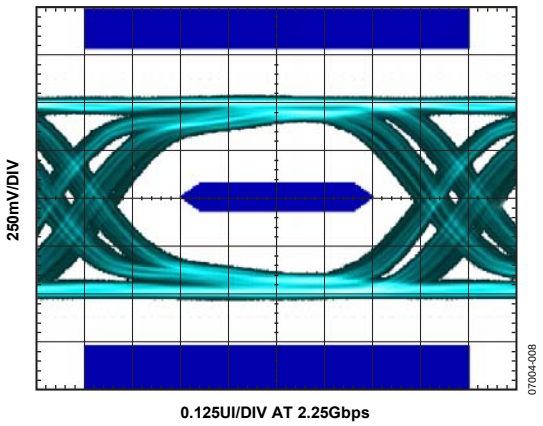



*Figure 8. Rx Eye Diagram at TP3, EQ = 12 dB (Cable = 20 m, 24 AWG)*

$T_A$ = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, AVEE = 0 V, differential input swing = 1000 mV, pattern = PRBS $2^7 - 1$, data rate = 2.25 Gbps, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

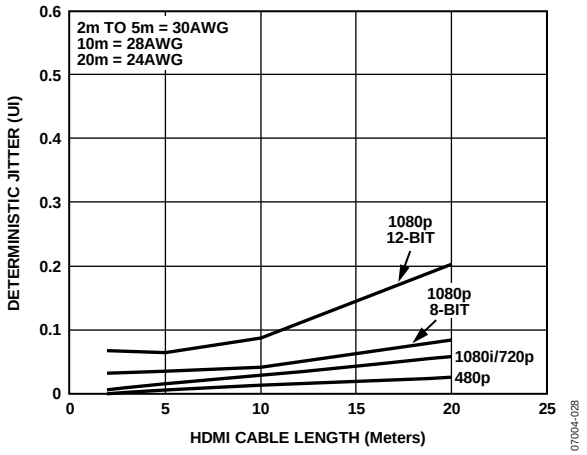



Figure 9. Jitter vs. Input Cable Length (See Figure 4 for Test Setup)

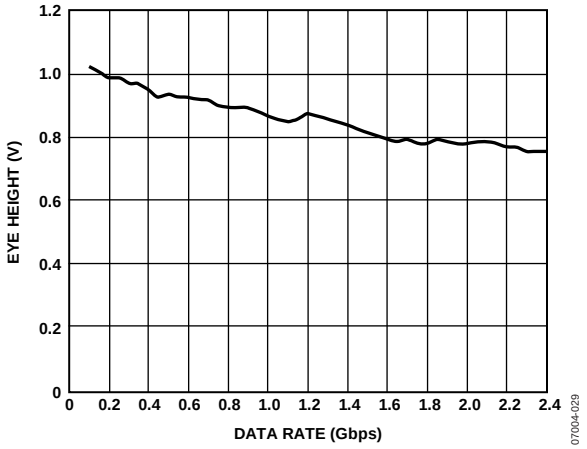



Figure 10. Eye Height vs. Data Rate

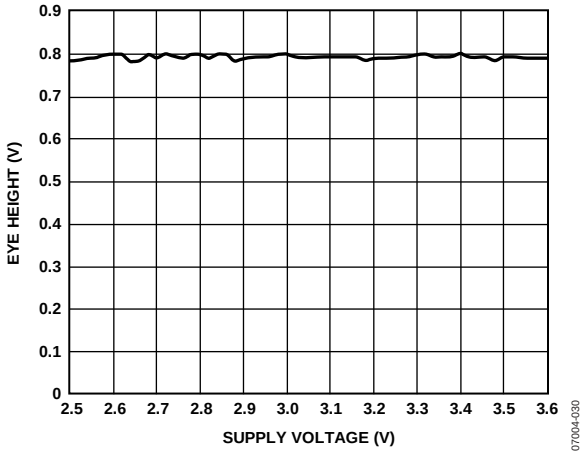



Figure 11. Eye Height vs. Supply Voltage

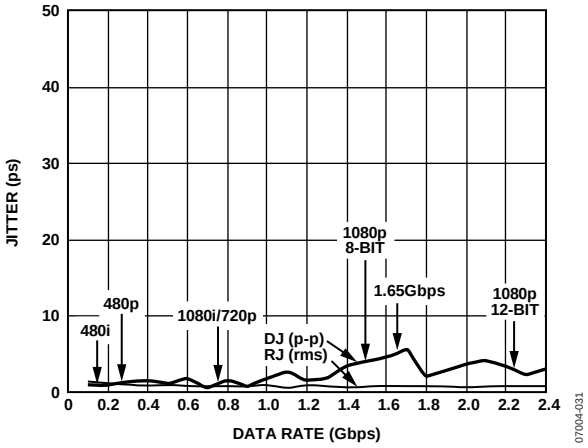



Figure 12. Jitter vs. Data Rate

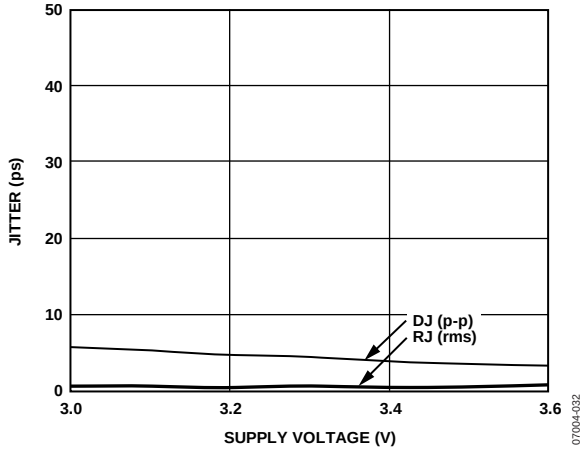



Figure 13. Jitter vs. Supply Voltage

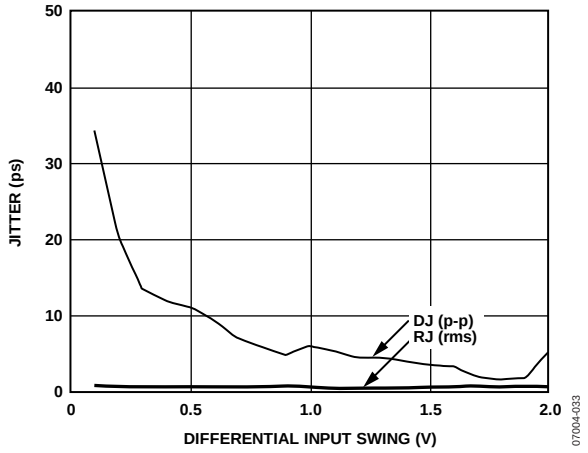



Figure 14. Jitter vs. Differential Input Swing

$T_A$ = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, AVEE = 0 V, differential input swing = 1000 mV, pattern = PRBS $2^7 - 1$, data rate = 2.25 Gbps, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

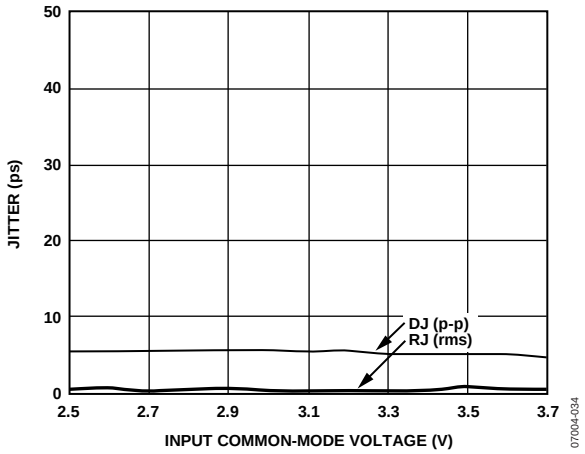



Figure 15. Jitter vs. Input Common-Mode Voltage

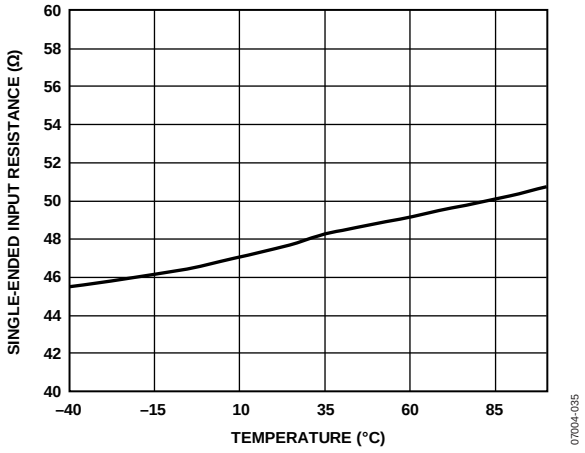



Figure 16. Single-Ended Input Resistance vs. Temperature

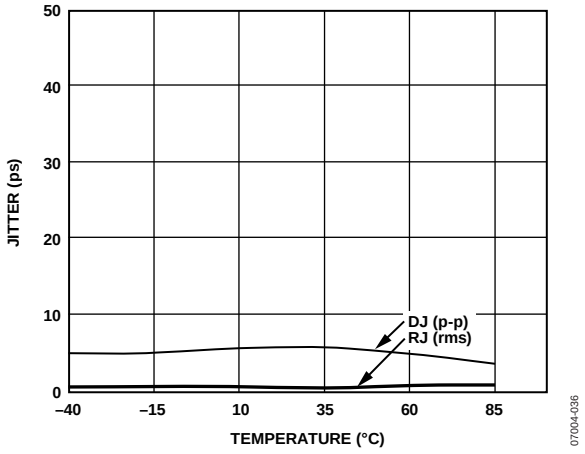



Figure 17. Jitter vs. Temperature

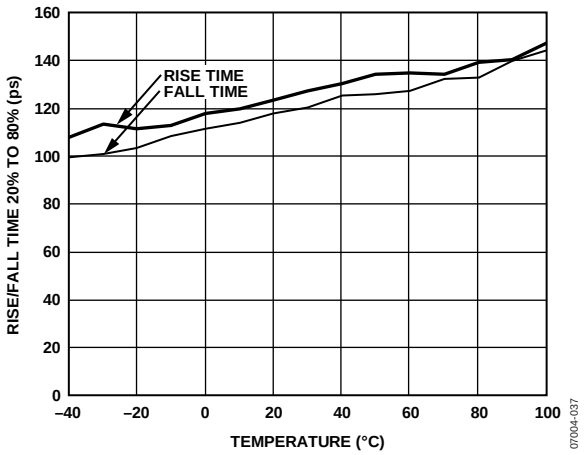



Figure 18. Rise and Fall Time vs. Temperature

# THEORY OF OPERATION

## INTRODUCTION

The primary function of the AD8194 is to switch the high speed signals from one of two (HDMI or DVI) single-link sources to one output. Each source group consists of four differential, high speed channels. The four high speed channels include a data-word clock and three Transition Minimized Differential Signaling (TMDS) data channels running at 10× the data-word clock frequency for data rates up to 2.25 Gbps. All four high speed channels of the AD8194 are identical; that is, the pixel clock can be run on any of the four TMDS channels. The AD8194 does not provide switching of the low speed DDC and CEC signals.

The AD8194 is an equalized, buffered TMDS switch with low added jitter. The output pins are electrically isolated from the inputs and the input equalizer recovers and transmits an open, full-swing data eye at the output, even for heavily attenuated input signals.

Because the AD8194 is a TMDS-only switch, a complete HDMI switch solution requires another component to switch the low speed DDC channels. Several low cost CMOS switches can be used along with the AD8194 to make an HDMI 1.3-compliant 2:1 link switch. The requirements for such a switch are as follows:

- Low input capacitance. The HDMI 1.3 specification limits the total DDC link capacitance for an HDMI sink to less than 50 pF. This 50 pF limit includes the HDMI connector, the PCB, the capacitance of the CMOS switch, and whatever capacitance is seen at the input of the HDMI receiver.
- Low channel on resistance ($R_{ON}$). Switches with high on resistance degrade the quality of the DDC signals.
- An appropriate form factor to switch the DDC and HPD signals as necessary.

A reference design that incorporates the AD8194 and a low cost CMOS switch is described in more detail in the Evaluation Board section.

In addition to the AD8194, Analog Devices, Inc., offers several HDMI switches with integrated DDC, in a variety of form factors.

## INPUT CHANNELS

Each high speed input differential pair terminates to the 3.3 V VTTI power supply through a pair of single-ended 50 Ω on-chip resistors, as shown in Figure 19. These matched on-chip terminations absorb reflections on the input TMDS channels, properly terminating the inputs and improving overall system signal integrity.

The input termination resistors all have series switches, as shown in Figure 19. The state of these switches is determined by the S_SEL signal, which also controls the input selection. The termination switches for the selected input channel are closed (terminations present), whereas the termination switches for the unselected input are open (high-Z inputs).

The input equalizer of the AD8194 provides 12 dB of high frequency boost. No specific cable length is suggested for use with the AD8194 because cable performance varies widely between manufacturers; however, in general, the equalization of the AD8194 does not degrade the system signal integrity, even for short input cables. For a 24 AWG reference cable, the AD8194 can equalize more than 20 m at data rates up to 2.25 Gbps.

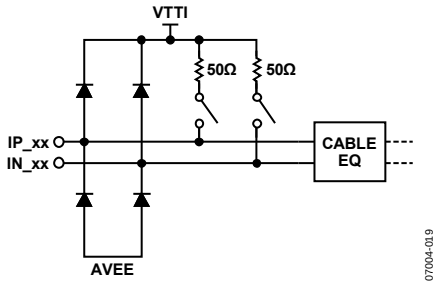



*Figure 19. High Speed Input Simplified Schematic*

## OUTPUT CHANNELS

Each high speed output differential pair is terminated to the 3.3 V VTTO power supply through two single-ended 50 Ω on-chip resistors, as shown in Figure 20. These matched on-chip back terminations absorb reflections on the output TMDS channels and improve the overall system signal integrity. These termination resistors are always present in the outputs and they cannot be switched out.

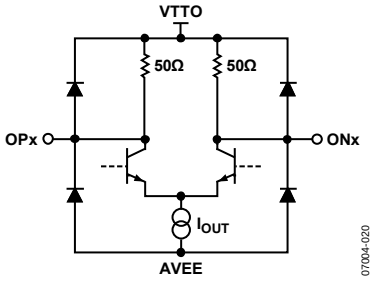



*Figure 20. High Speed Output Simplified Schematic*

In a typical application, the AD8194 output is connected to the input of an HDMI/DVI receiver, which provides a second set of matched terminations in accordance with the HDMI 1.3 specification. If no receiver is connected, each of the AD8194 output pins should be tied to 3.3 V through a 50 Ω on-board termination resistor.

## SWITCHING MODE

The source selector pin, S_SEL, is used to select which of the two input groups is routed to the output. Source A is selected when S_SEL is pulled up to logic high, and Source B is selected when S_SEL is pulled down to logic low. Logic levels for this pin are set in accordance with the specifications listed in Table 5. The AD8194 can be used as a single-link TMDS buffer by setting S_SEL to one fixed logic value.

S_SEL also controls the switch status of the input termination resistors. The termination resistors for the selected input are always connected, whereas the termination resistors for the unselected input are always switched out (high-Z inputs).

**Table 5. S_SEL Description**

| S_SEL | Selected Input | Input Termination Status |
|---|---|---|
| 0 | Input B | Input B terminations enabled, Input A terminations disabled |
| 1 | Input A | Input A terminations enabled, Input B terminations disabled |

# APPLICATION NOTES

## SWITCHING HIGH SPEED SIGNALS

The AD8194 is a quad 2:1 TMDS switch that is used to switch the high speed signals of two input HDMI links to a single HDMI output.

## SWITCHING LOW SPEED SIGNALS

Because the AD8194 is a TMDS-only switch, a complete HDMI switch solution requires another component to switch the low speed DDC channels.

The HDMI 1.3 specification places a number of restrictions on the low speed signal path that limit the selection of a suitable low cost DDC switch. The first requirement is that the switch must be bidirectional to convey the I²C® protocol signals that pass through it. A CMOS device is the simplest switch with this capability.

The second HDMI requirement for the DDC signals is that the total DDC signal path capacitance be less than 50 pF. The total capacitance comprises the HDMI connector, the PC board traces, the DDC switch, and the input capacitance of the HDMI receiver. As a practical design consideration, a suitable DDC switch has a total channel capacitance of less than 10 pF.

Finally, the channel on-resistance ($R_{ON}$) of the DDC switch must not be too high; otherwise, the voltage drop across it violates the maximum $V_{OL}$ of the I²C signals. Any switch with an on resistance of approximately 100 Ω is sufficient in a typical application, assuming that the end application includes an I²C-compliant receiver device. Switches with lower channel on resistance have improved $V_{OL}$ performance.

For the AD8194 evaluation board, the MC74LVX4053 was chosen to switch the low speed signals. This part has a maximum $R_{ON}$ of 108 Ω and a maximum parasitic capacitance of 10 pF. Refer to the Evaluation Board section for details on how to use the MC74LVX4053 with the AD8194 in an application.

## PCB LAYOUT GUIDELINES

The AD8194 is used to switch HDMI/DVI video signals, which are differential, unidirectional, and high speed (up to 2.25 Gbps). The channels that carry the video data must be controlled impedance, terminated at the receiver, and capable of operating up to at least 2.25 Gbps. It is especially important to note that the differential traces that carry the TMDS signals should be designed with a controlled differential impedance of 100 Ω. The AD8194 provides single-ended 50 Ω terminations on chip for both its inputs and outputs. Transmitter termination is not fully specified by the HDMI standard, but the inclusion of the 50 Ω output terminations improves the overall system signal integrity.

### *TMDS Signals*

The audiovisual (AV) data carried on these high speed channels is encoded by a technique called Transition Minimized Differential Signaling (TMDS) and, in the case of HDMI, is also encrypted according to the high bandwidth digital content protection (HDCP) standard.

In the HDMI/DVI standard, four differential pairs carry the TMDS signals. For DVI, three of these pairs are dedicated to carrying RGB video and sync data. For HDMI, audio data is also interleaved with the video data; the DVI standard does not incorporate audio information. The fourth high speed differential pair is used for the AV data-word clock and runs at one-tenth the speed of the TMDS data channels.

The four high speed channels of the AD8194 are identical. No concession was made to lower the bandwidth of the fourth channel for the pixel clock, so any channel can be used for any TMDS signal. The user chooses which signal is routed over which channel. Additionally, the TMDS channels are symmetrical; therefore, the p and n of a given differential pair are interchangeable, provided the inversion is consistent across all inputs and outputs of the AD8194. However, the routing between inputs and outputs through the AD8194 is fixed. For example, Output Channel 0 always switches between Input A0 and Input B0, and so forth.

The AD8194 buffers the TMDS signals, and the input traces can be considered electrically independent of the output traces. In most applications, the quality of the signal on the input TMDS traces is more sensitive to the PCB layout. Regardless of the data being carried on a specific TMDS channel, or whether the TMDS line is at the input or the output of the AD8194, all four high speed signals should be routed on a PCB in accordance with the same RF layout guidelines.

### *Layout for the TMDS Signals*

The TMDS differential pairs can be either microstrip traces, routed on the outer layer of a board, or stripline traces, routed on an internal layer of the board. If microstrip traces are used, there should be a continuous reference plane on the PCB layer directly below the traces. If stripline traces are used, they must be sandwiched between two continuous reference planes in the PCB stackup. Additionally, the p and n of each differential pair must have a controlled differential impedance of 100 Ω. The characteristic impedance of a differential pair is a function of several variables, including the trace width, the distance separating the two traces, the spacing between the traces and the reference plane, and the dielectric constant of the PC board binder material. Interlayer vias introduce impedance discontinuities that can cause reflections and jitter on the signal path; therefore, it is preferable to route the TMDS lines exclusively on one layer of the board, particularly for the input traces. Additionally, to prevent unwanted signal coupling and interference, route the TMDS signals away from other signals and noise sources on the PCB.

Both traces of a given differential pair must be equal in length to minimize intrapair skew. Maintaining the physical symmetry of a differential pair is integral to ensuring its signal integrity; excessive intrapair skew can introduce jitter through duty cycle distortion (DCD). The p and n of a given differential pair should always be routed together to establish the required 100 Ω differential impedance. Enough space should be left between the differential pairs of a given group so that the n of one pair does not couple to the p of another pair. For example, one technique is to make the interpair distance 4 to 10 times wider than the intrapair spacing.

Any group of four TMDS channels (Input A, Input B, or the output) should have closely matched trace lengths to minimize interpair skew. Severe interpair skew can cause the data on the four different channels of a group to arrive out of alignment with one another. A good practice is to match the trace lengths for a given group of four channels to within 0.05 inches on FR4 material.

The length of the TMDS traces should be minimized to reduce overall signal degradation. Commonly used PC board material such as FR4 is lossy at high frequencies; therefore, long traces on the circuit board increase signal attenuation, resulting in decreased signal swing and increased jitter through intersymbol interference (ISI).

### Controlling the Characteristic Impedance of a TMDS Differential Pair

The characteristic impedance of a differential pair depends on a number of variables, including the trace width, the distance between the two traces, the height of the dielectric material between the trace and the reference plane below it, and the dielectric constant of the PCB binder material. To a lesser extent, the characteristic impedance also depends upon the trace thickness and the presence of solder mask.

There are many combinations that can produce the correct characteristic impedance. It is generally required to work with the PC board fabricator to obtain a set of parameters to produce the desired results.

To guarantee a differential pair with a differential impedance of 100 Ω over the entire length of the trace, change the width of the traces in a differential pair based on how closely one trace is coupled to the other. When the two traces of a differential pair are close and strongly coupled, they should have a width that produces a 100 Ω differential impedance. When the traces split apart to go into a connector, for example, and are no longer so strongly coupled, the width of the traces should be increased to yield a differential impedance of 100 Ω in the new configuration.

### Ground Current Return

In some applications, it may be necessary to invert the output pin order of the AD8194. This requires routing the TMDS traces on multiple layers of the PCB. When routing differential pairs on multiple layers, it is also necessary to reroute the corresponding reference plane to provide one continuous ground current return path for the differential signals. Standard plated through-hole vias are acceptable for both the TMDS traces and the reference plane. An example of this is illustrated in Figure 21.

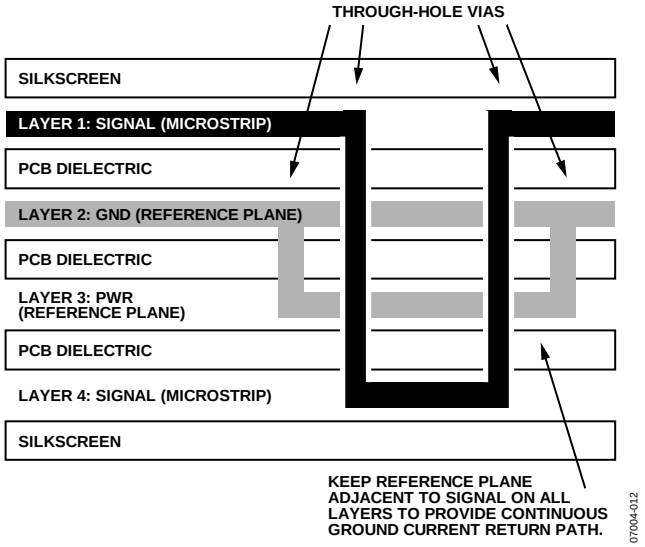



*Figure 21. Example Routing of Reference Plane*

### TMDS Terminations

The AD8194 provides internal 50 Ω single-ended terminations for all of its high speed inputs and outputs. The termination resistors back-terminate the output TMDS transmission lines. These back-terminations act to absorb reflections from impedance discontinuities on the output traces, improving the signal integrity of the output traces and adding flexibility to how the output traces can be routed. For example, interlayer vias can be used to route the AD8194 TMDS outputs on multiple layers of the PCB without severely degrading the quality of the output signal.

In a typical application, the AD8194 output is connected to an HDMI/DVI receiver or to another device with a 50 Ω single-ended input termination. It is recommended that the outputs be terminated with external 50 Ω on-board resistors when the AD8194 is not connected to another device.

### Auxiliary Control Signals

There are four single-ended control signals associated with each source or sink in an HDMI/DVI application. These are hot plug detect (HPD), consumer electronics control (CEC), and two display data channel (DDC) lines. The two signals on the DDC bus are SDA and SCL (serial data and serial clock, respectively). The AD8194, which is a low cost part, does not have any additional capability to switch these signals; other means are required to switch these signals if required.

In general, it is sufficient to route each auxiliary signal as a single-ended trace. These signals are not sensitive to impedance discontinuities, do not require a reference plane, and can be routed on multiple layers of the PCB. However, it is best to follow strict layout practices whenever possible to prevent the PCB design from affecting the overall application. The specific routing of the HPD, CEC, and DDC lines depends upon the application in which the AD8194 is being used.

For example, the maximum speed of signals present on the auxiliary lines is 100 kHz $I^2C$ data on the DDC lines; therefore, any layout that enables 100 kHz $I^2C$ to be passed over the DDC bus should suffice. The HDMI 1.3 specification, however, places a strict 50 pF limit on the amount of capacitance that can be measured on either SDA or SCL at the HDMI input connector. This 50 pF limit includes the HDMI connector, the PCB, the capacitance of the CMOS switch, and whatever capacitance is seen at the input of the HDMI receiver. There is a similar limit of 100 pF of input capacitance for the CEC line.

The parasitic capacitance of traces on a PCB increases with trace length. To help ensure that a design satisfies the HDMI specification, the length of the CEC and DDC lines on the PCB should be made as short as possible. Additionally, if there is a reference plane in the layer adjacent to the auxiliary traces in the PCB stackup, relieving or clearing out this reference plane immediately under the auxiliary traces significantly decreases the amount of parasitic trace capacitance. An example of the board stackup is shown in Figure 22.

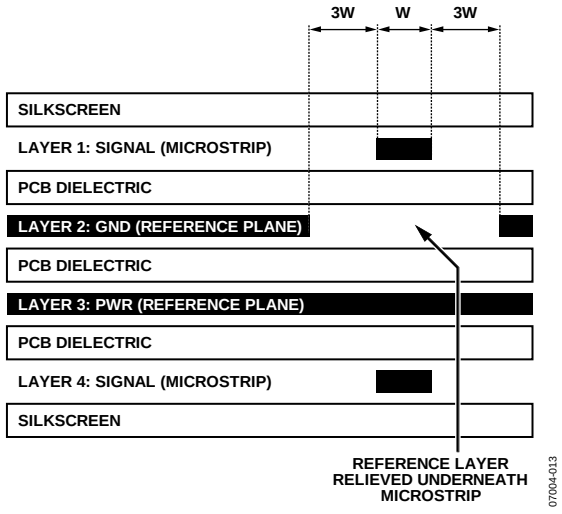



*Figure 22. Example Board Stackup*

HPD is a dc signal presented by a sink to a source to indicate that the source EDID is available for reading. The placement of this signal is not critical, but it should be routed as directly as possible.

### Power Supplies

The AD8194 has three separate power supplies referenced to a single ground. The supply/ground pairs are

- AVCC/AVEE
- VTTI/AVEE
- VTTO/AVEE

The AVCC/AVEE (3.3 V) supply powers the core of the AD8194. The VTTI/AVEE supply (3.3 V) powers the input termination (see Figure 19). Similarly, the VTTO/AVEE supply (3.3 V) powers the output termination (see Figure 20).

In a typical application, all pins labeled AVEE should be connected directly to ground. All pins labeled AVCC, VTTI, or VTTO should be connected to 3.3 V. The supplies can also be powered individually, but care must be taken to ensure that each stage of the AD8194 is powered correctly.

### Power Supply Bypassing

The AD8194 requires minimal supply bypassing. When powering the supplies individually, place a 0.01 µF capacitor between each 3.3 V supply pin (AVCC, VTTI, and VTTO) and ground to filter out supply noise. Generally, bypass capacitors should be placed near the power pins and should connect directly to the relevant supplies (without long intervening traces). For example, to minimize the parasitic inductance of the power supply decoupling capacitors, minimize the trace length between capacitor landing pads and the vias as shown in Figure 23.

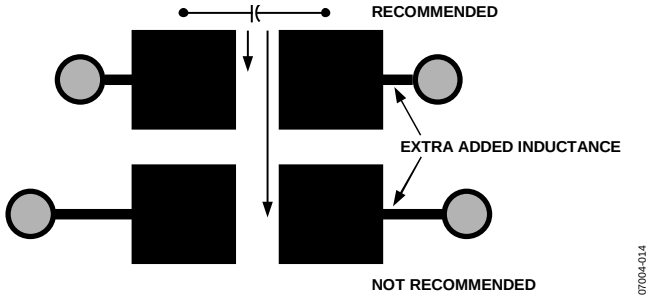



*Figure 23. Recommended Pad Outline for Bypass Capacitors*

In applications where the AD8194 is powered by a single 3.3 V supply, it is recommended to use two reference supply planes and bypass the 3.3 V reference plane to the ground reference plane with one 220 pF, one 1000 pF, two 0.01 µF, and one 4.7 µF capacitors. The capacitors should via down directly to the supply planes and be placed within a few centimeters of the AD8194.

### *Evaluation Board*

The AD8194 evaluation board illustrates one way to implement a 2:1 HDMI link switch with an AD8194 and a CMOS switch. The AD8194 evaluation board deviates from a typical application in that it uses an HDMI connector for the output as well as for the inputs. This setup makes it easy to connect equipment to the AD8194 evaluation board with standard HDMI cables. However, this arrangement requires crossing over the TMDS signals on the output side (see Figure 24).

In a typical application, the output of the AD8194 is routed directly into an HDMI receiver. Because a receiver is generally designed to interface directly to an HDMI input connector, it is not necessary to cross over the TMDS signals in a typical application (see Figure 25).

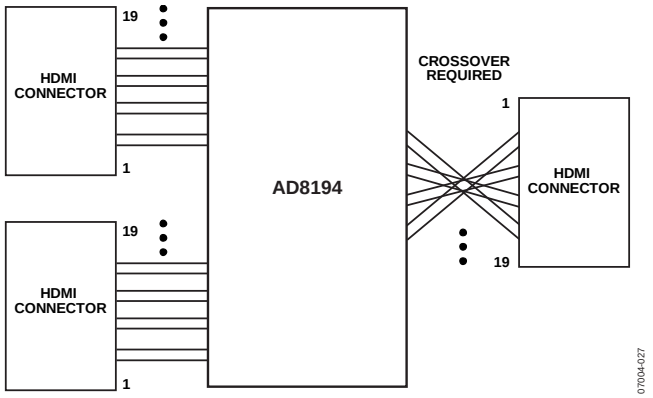



*Figure 24. Block Diagram of AD8194 Evaluation Board Showing Output Crossover*

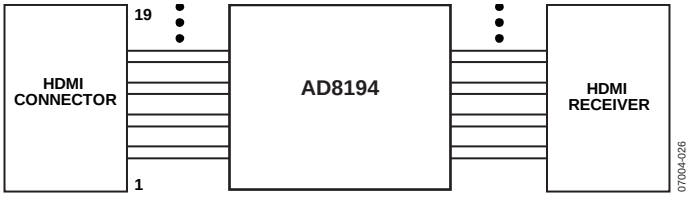



*Figure 25. HDMI Signals to HDMI Receiver, No Crossover Required*

Figure 26 shows the layout of the TMDS traces. These are 100 Ω differential, controlled-impedance traces. Serpentine traces are used for some of the paths to match the lengths within a group of four. The gray traces are routed on the top layer and the black traces on the bottom layer.

The low speed switching is performed by an MC74LVX4053. This part contributes a maximum on resistance of 108 Ω and a maximum capacitive load of 10 pF. The same select signal (S_SEL) controls both the AD8194 and the MC74LVX4053.

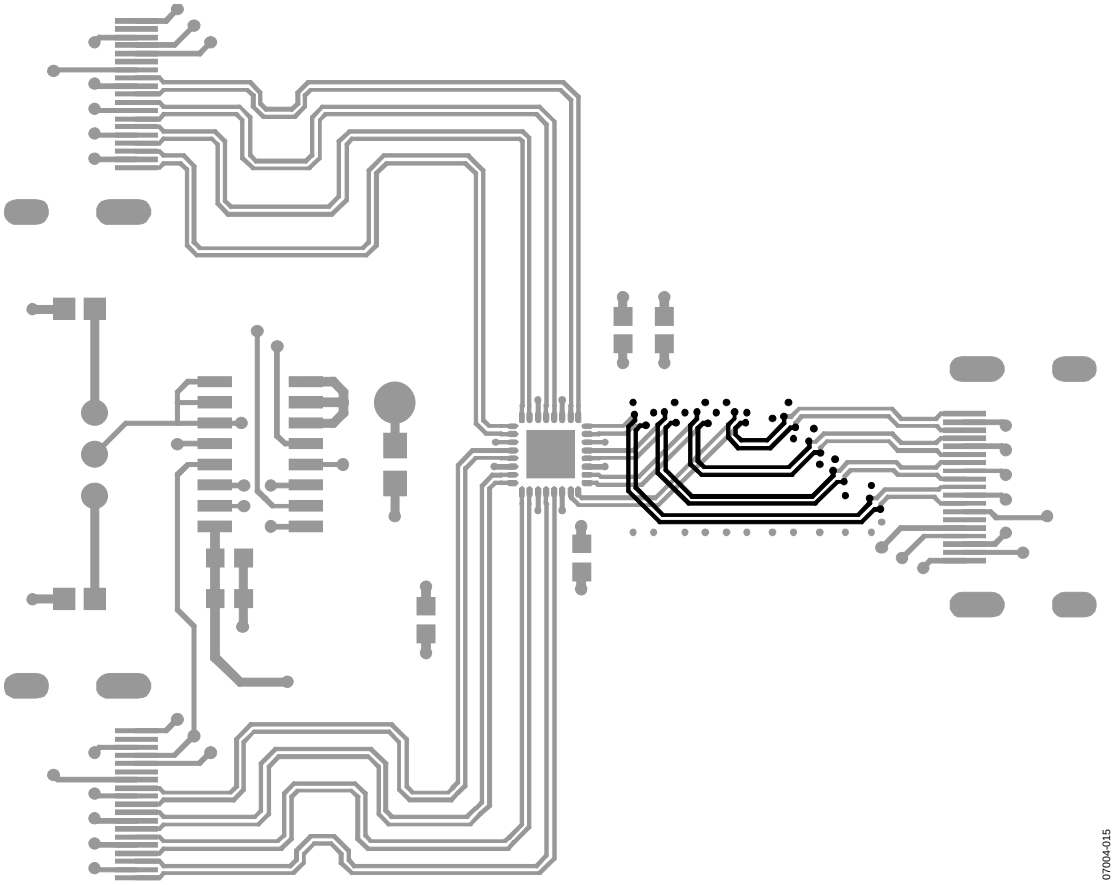
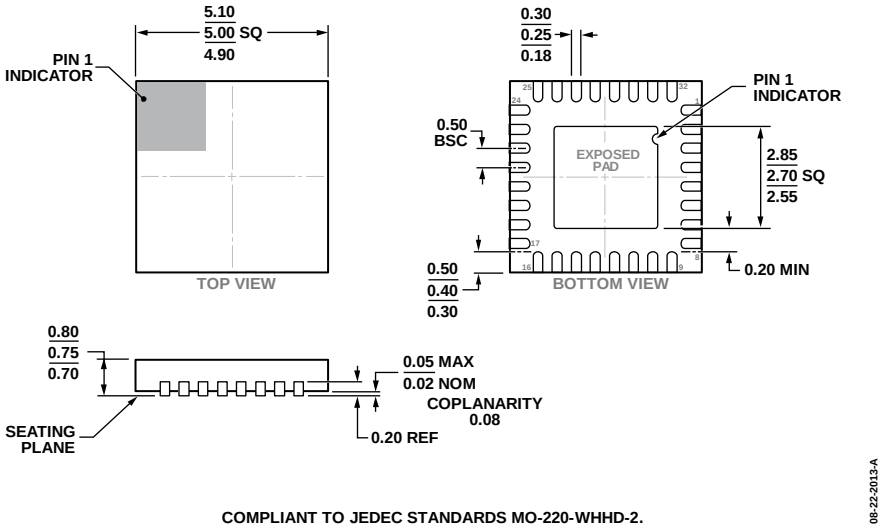



*Figure 26. Layout of TMDS Traces*

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-2.

*Figure 27. 32-Lead Lead Frame Chip Scale Package [LFCSP]*
*5 mm × 5 mm Body and 0.75 mm Package Height*
*(CP-32-21)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option | Ordering Quantity |
|---|---|---|---|---|
| AD8194ACPZ | −40°C to +85°C | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-21 | |
| AD8194ACPZ-R7 | −40°C to +85°C | 32-Lead Lead Frame Chip Scale Package [LFCSP], Reel | CP-32-21 | 1,500 |
| AD8194-EVALZ | | Evaluation Board | | |

[1] Z = RoHS Compliant Part.