

**General Description**

The AO4618 uses advanced trench technology to provide excellent  $R_{DS(ON)}$  and low gate charge. This complementary N and P channel MOSFET configuration is ideal for low Input Voltage inverter applications.

**Product Summary**
**N-Channel**

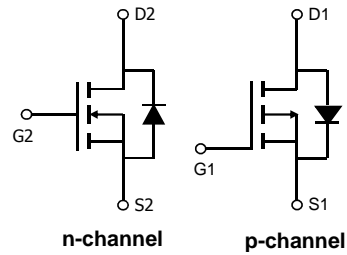
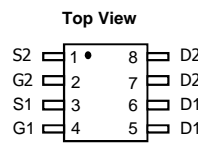
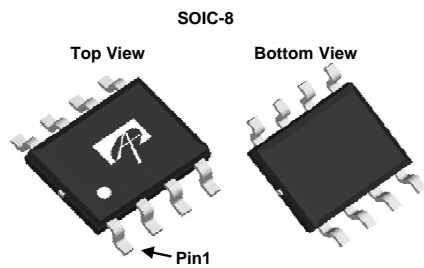
$V_{DS} = 40V$   
 $I_D = 8A$  ( $V_{GS} = 10V$ )  
 $R_{DS(ON)} < 19m\Omega$  ( $V_{GS} = 10V$ )  
 $< 27m\Omega$  ( $V_{GS} = 4.5V$ )

100% UIS Tested  
 100%  $R_g$  Tested

**P-Channel**

$-40V$   
 $-7A$  ( $V_{GS} = -10V$ )  
 $R_{DS(ON)} < 23m\Omega$  ( $V_{GS} = -10V$ )  
 $< 30m\Omega$  ( $V_{GS} = -4.5V$ )

100% UIS Tested  
 100%  $R_g$  Tested


**Absolute Maximum Ratings  $T_A = 25^\circ C$  unless otherwise noted**

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	$V_{DS}$	40	-40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_A = 25^\circ C$	8	A
		$T_A = 70^\circ C$	6	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	40	-35	A
Avalanche Current <sup>C</sup>	$I_{AS}$	15	-35	A
Avalanche energy $L = 0.1mH$ <sup>C</sup>	$E_{AS}$	11	61	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_A = 25^\circ C$	2	W
		$T_A = 70^\circ C$	1.3	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150		$^\circ C$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	48	62.5	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A,D</sup>		Steady-State	74	90
Maximum Junction-to-Lead	$R_{\theta JL}$	32	40	$^\circ C/W$

**N-Channel Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	40			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.4	1.9	2.4	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =8A T <sub>J</sub> =125°C		15.4	19	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =4A		21	27	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =8A		33		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.75	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				2.5	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =20V, f=1MHz		415		pF
C <sub>oss</sub>	Output Capacitance			112		pF
C <sub>riss</sub>	Reverse Transfer Capacitance			11		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	1	2.2	3.5	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, I <sub>D</sub> =8A		6.5	12	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge			3	6	nC
Q <sub>gs</sub>	Gate Source Charge			1.2		nC
Q <sub>gd</sub>	Gate Drain Charge			1.1		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, R <sub>L</sub> =2.5Ω, R <sub>GEN</sub> =3Ω		4		ns
t <sub>r</sub>	Turn-On Rise Time			3		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			15		ns
t <sub>f</sub>	Turn-Off Fall Time			2		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =8A, dI/dt=100A/μs		12.5		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =8A, dI/dt=100A/μs		3.5		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25° C.

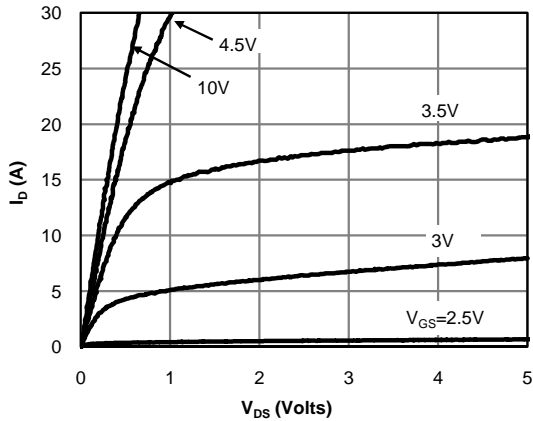
D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

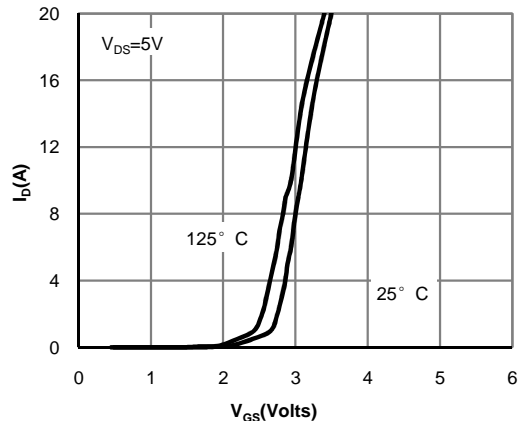
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.

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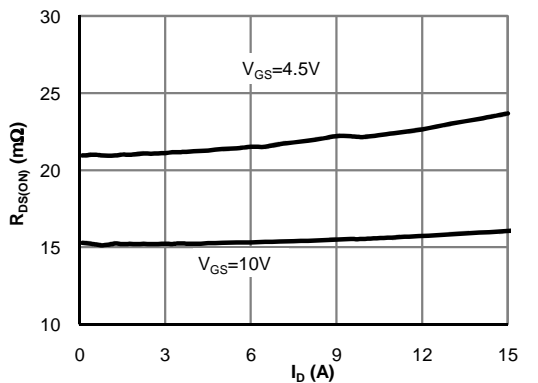
**N-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



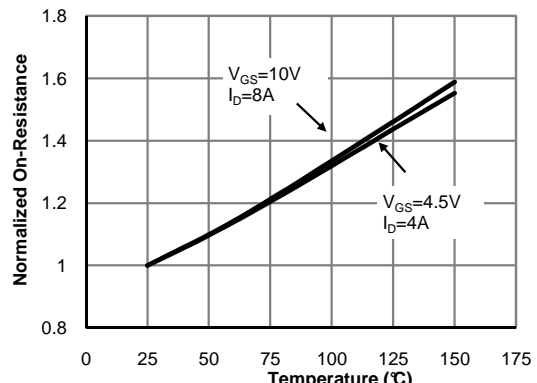
**Fig 1: On-Region Characteristics (Note E)**



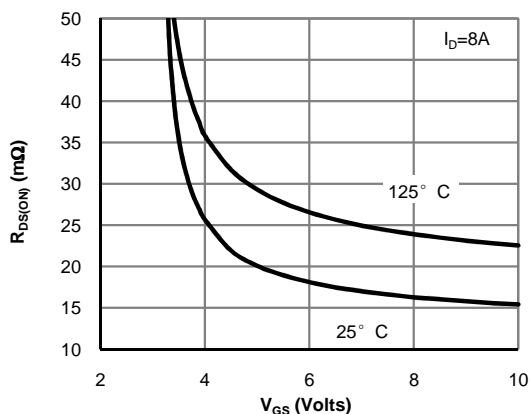
**Figure 2: Transfer Characteristics (Note E)**



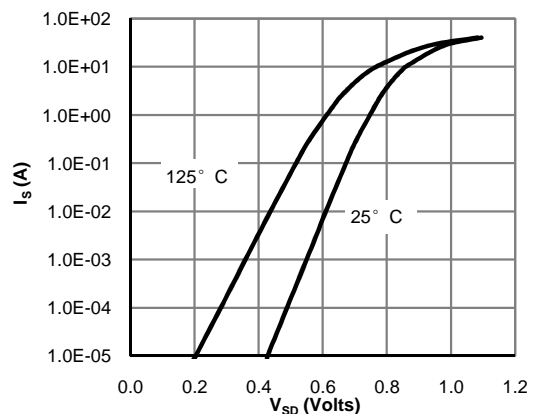
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

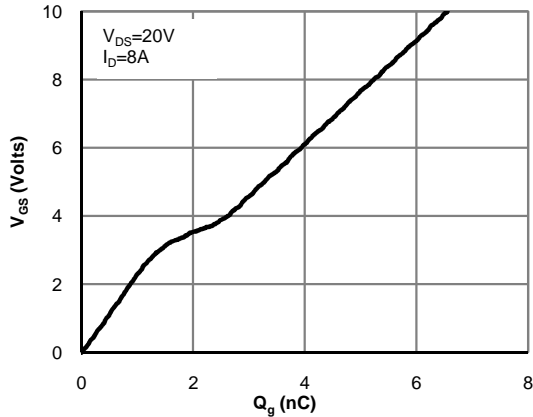


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

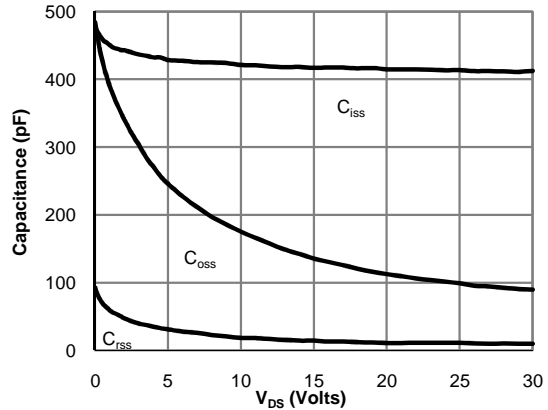


**Figure 6: Body-Diode Characteristics (Note E)**

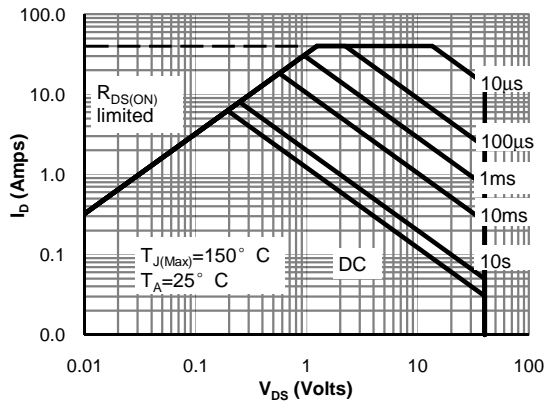
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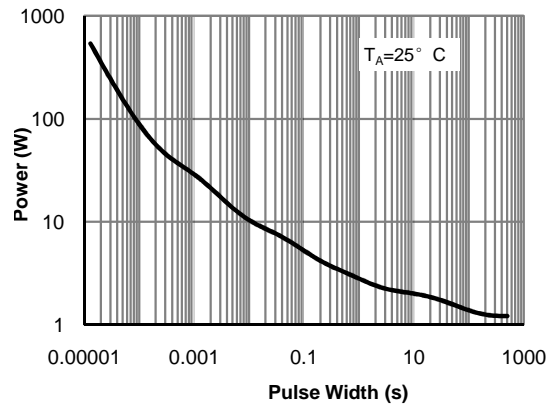
**Figure 7: Gate-Charge Characteristics**



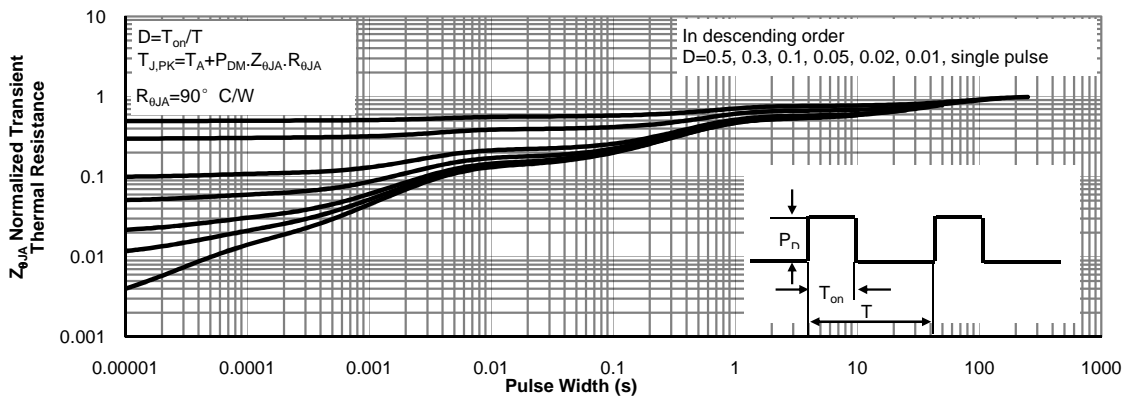
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

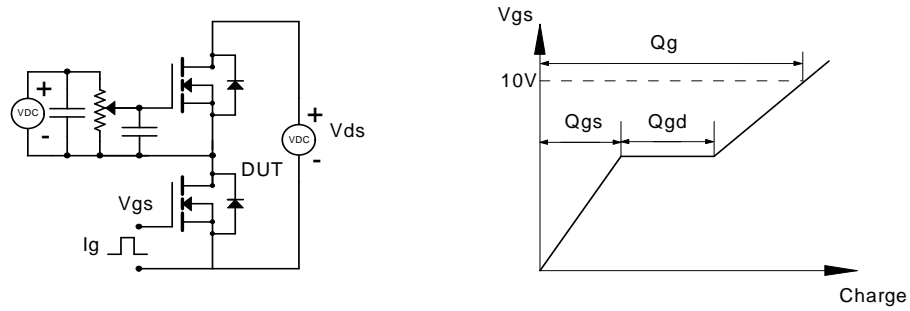


**Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)**

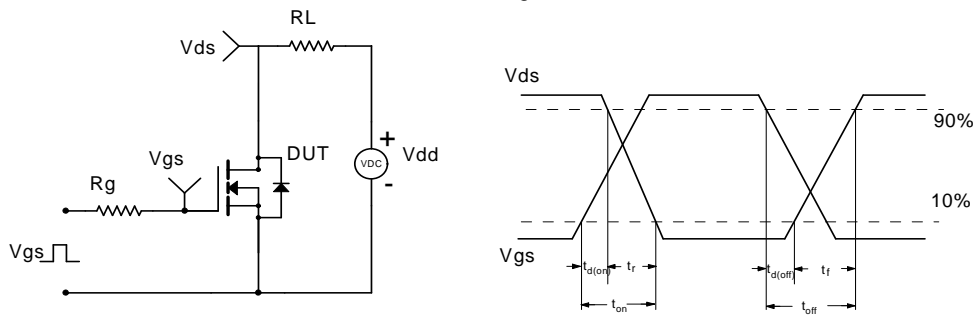


**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

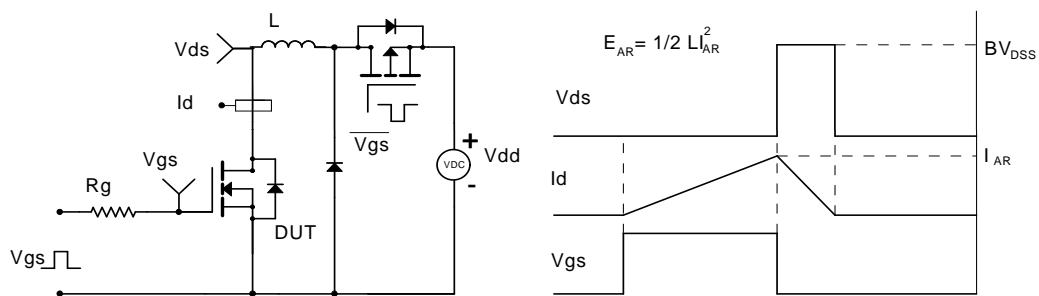
**Gate Charge Test Circuit & Waveform**



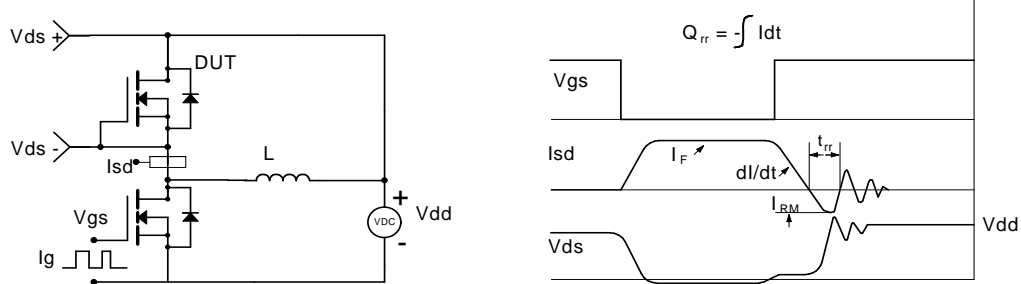
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**P-Channel Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0V	-40			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-40V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-1 -5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.7	-1.9	-3	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-7A T <sub>J</sub> =125°C		19	23	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4A		28.5	35	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-7A		26		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.74	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				-2.5	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-20V, f=1MHz		1870		pF
C <sub>oss</sub>	Output Capacitance			185		pF
C <sub>riss</sub>	Reverse Transfer Capacitance			155		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		4.5	9	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =-20V, I <sub>D</sub> =-7A		32	45	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge			8	12	nC
Q <sub>gs</sub>	Gate Source Charge			7.6		nC
Q <sub>gd</sub>	Gate Drain Charge			6.2		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =-20V, R <sub>L</sub> =2.8Ω, R <sub>GEN</sub> =3Ω		10		ns
t <sub>r</sub>	Turn-On Rise Time			18		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			38		ns
t <sub>f</sub>	Turn-Off Fall Time			24		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =-7A, dI/dt=500A/μs		13		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =-7A, dI/dt=500A/μs		33		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using ≤ 10s junction-to-ambient thermal resistance.

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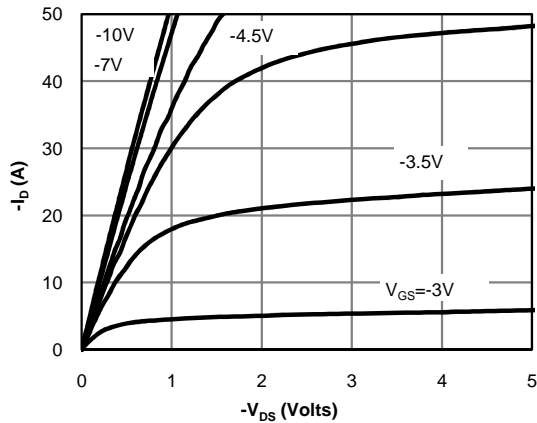
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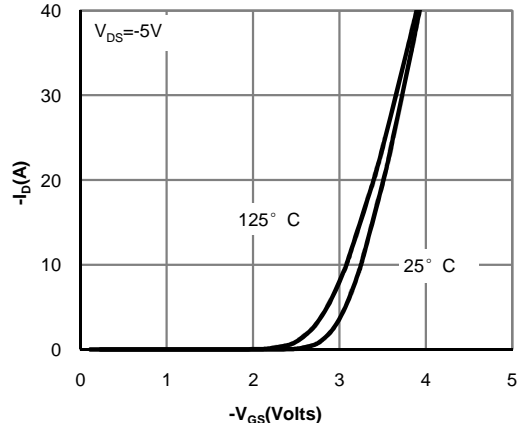
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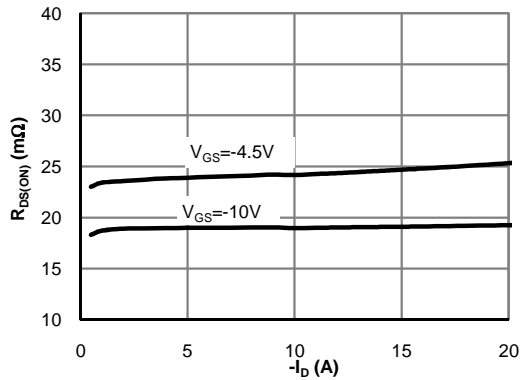
**P-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



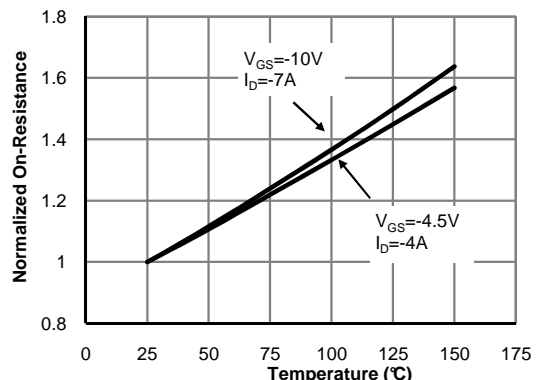
**Fig 1: On-Region Characteristics (Note E)**



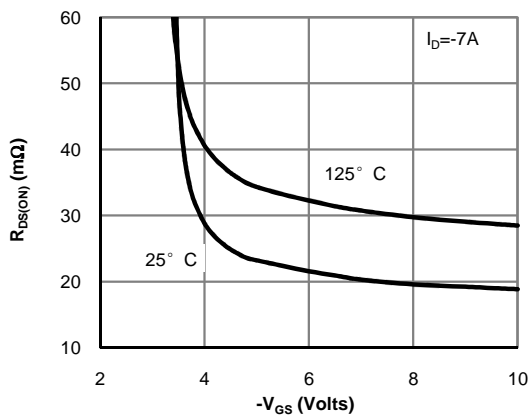
**Figure 2: Transfer Characteristics (Note E)**



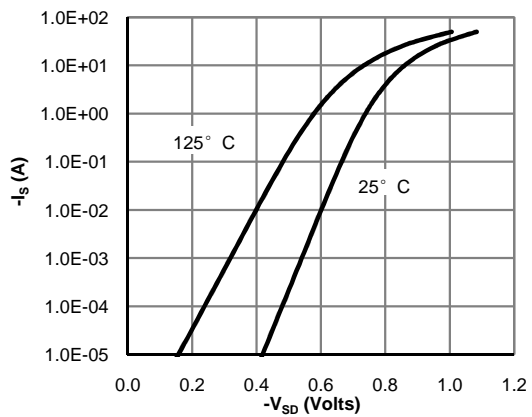
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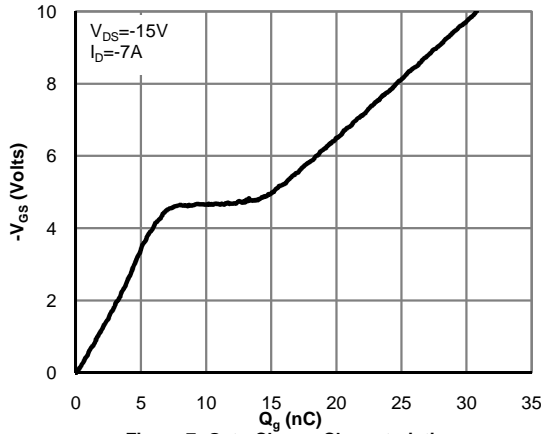


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

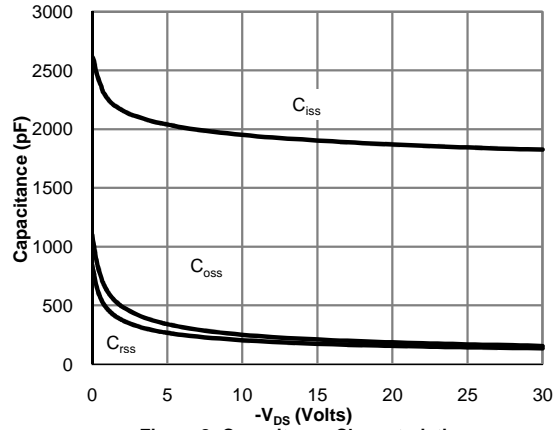


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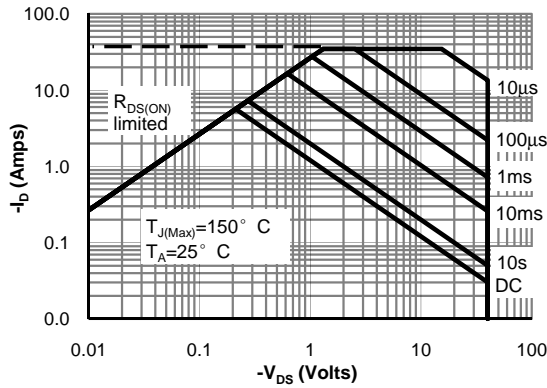
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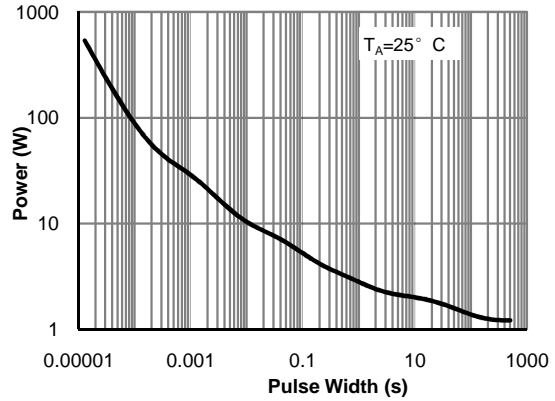
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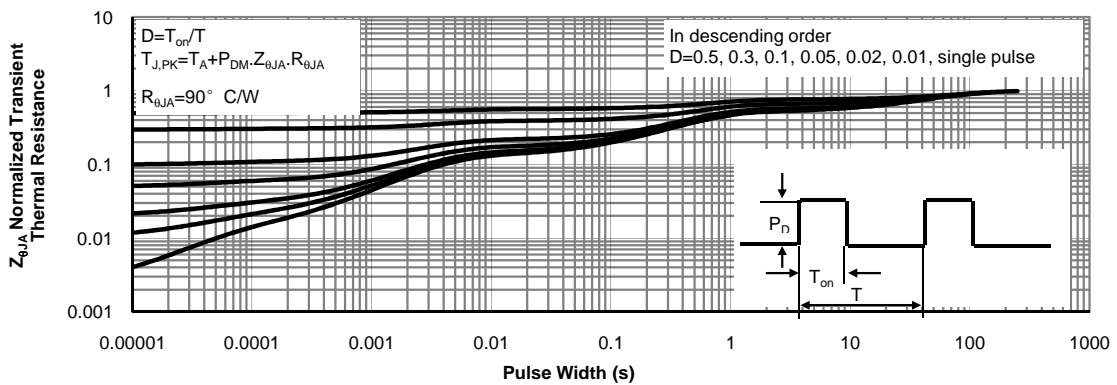
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



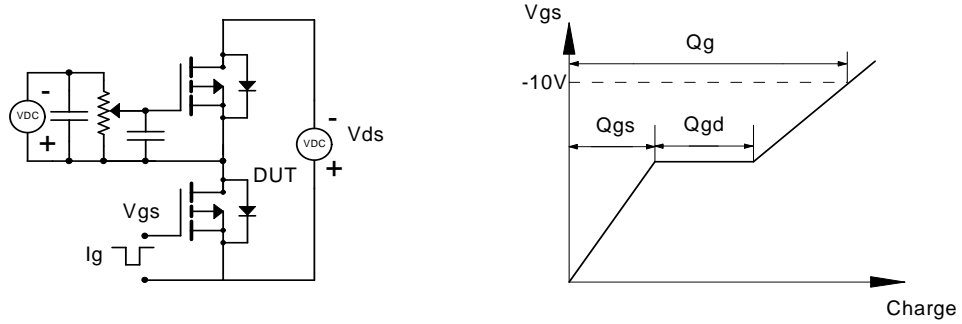
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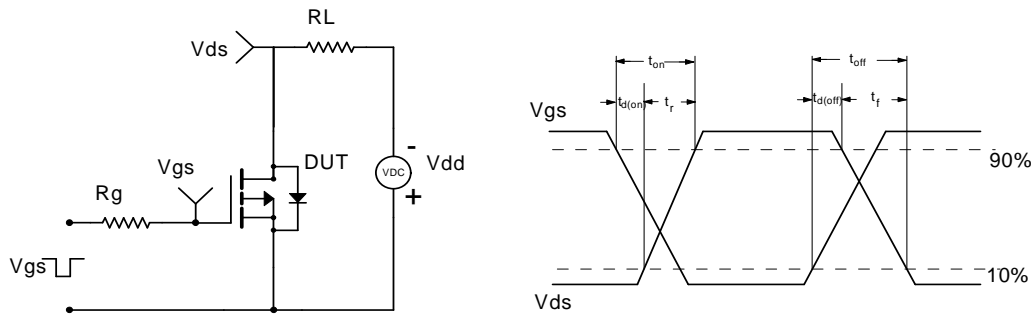
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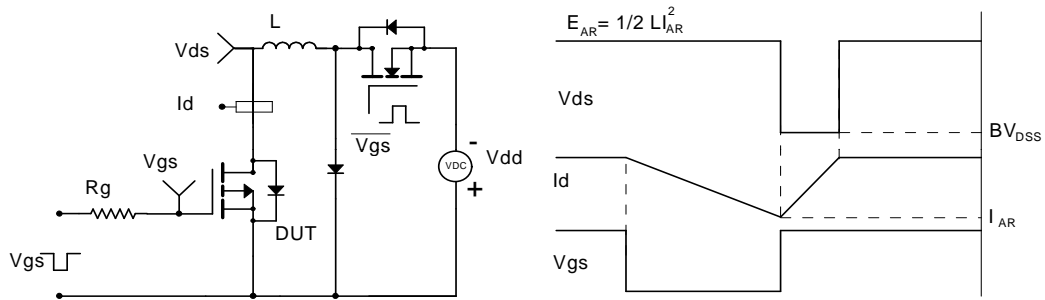
**Gate Charge Test Circuit & Waveform**



**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**

