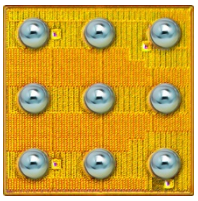
EPC2039 – Enhancement Mode Power Transistor
Preliminary Specification Sheet

Status: Engineering

Features:

- V_{DS}, 80V
- Maximum $R_{DS(on)}$, 22 mΩ
- I_D, 6.8 A
- Pulsed I_D, 50 A
- Pb-Free (RoHS Compliant), Halogen Free



EPC2039 eGaN® FETs are supplied only in passivated die form with solder balls

Die Size: 1.35 mm x 1.35 mm

Applications:

- High Frequency DC-DC Conversion
- Wireless Power Transfer
- LiDAR/Pulsed Power Applications

MAXIMUM RATINGS

Parameter	Value
Maximum Drain – Source Voltage	80 V
Gate – Source Maximum Voltage Range	-4 V < V_{GS} < 6 V
Continuous Drain Current, (T_A = 25 °C, $R_{\theta JA}$ = 70 °C/W)	6.8 A
Maximum Pulsed Drain Current, 25 °C, T_{pulse} = 300 µs	50 A
Optimum Temperature Range	-40 °C < T_J < 150 °C

STATIC CHARACTERISTICS

Parameter	Conditions	Value
Maximum Drain – Source Leakage	V_{DS} = 64 V, V_{GS} = 0 V	0.25 mA
Maximum $R_{DS(on)}$	V_{GS} = 5 V, I_D = 6 A	22 mΩ
Typical $R_{DS(on)}$	V_{GS} = 5 V, I_D = 6 A	17 mΩ
Gate – Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 2 mA	0.8 V < $V_{GS(TH)}$ < 2.5 V
Gate – Source Maximum Positive Leakage	V_{GS} = 5 V	2 mA
Gate – Source Maximum Negative Leakage	V_{GS} = -4 V	-0.25 mA

T_J = 25 °C unless otherwise stated
Specifications are with Substrate shorted to Source

DYNAMIC CHARACTERISTICS

Parameter	Conditions	Typical Value
C_{ISS} (Input Capacitance)	V_{DS} = 40 V, V_{GS} = 0 V	210 pF
C_{OSS} (Output Capacitance)		115 pF
C_{RSS} (Reverse Transfer Capacitance)		3 pF
Q_G (Total Gate Charge)	V_{DS} = 40 V, I_D = 6 A, V_{GS} = 5 V	2 nC
Q_{GS} (Gate to Source Charge)	V_{DS} = 40 V, I_D = 6 A	0.63 nC
Q_{GD} (Gate to Drain Charge)		0.42 nC
$Q_{G(TH)}$ (Gate Charge at Threshold)		0.45 nC
Q_{OSS} (Output Charge)	V_{DS} = 40 V, V_{GS} = 0 V	7.6 nC
Q_{RR} (Source-Drain Recovery Charge)		0

T_J = 25 °C unless otherwise stated
Specifications are with Substrate shorted to Source

THERMAL CHARACTERISTICS

		TYP	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	28	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	80	°C/W

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details

Figure 1: Typical Output Characteristics at 25°C

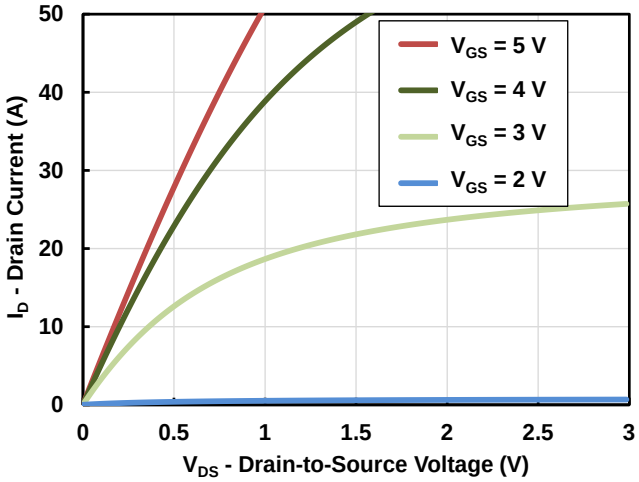


Figure 2: Transfer Characteristics

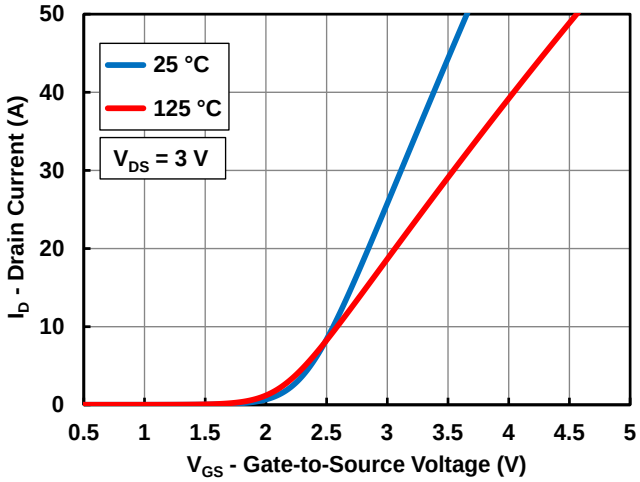


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

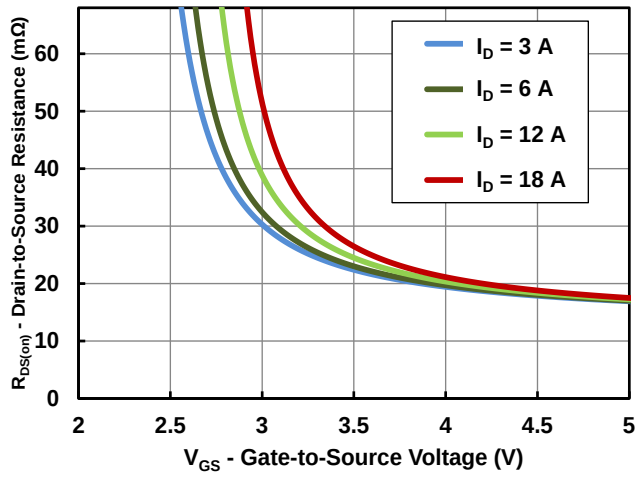


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Drain Temperatures

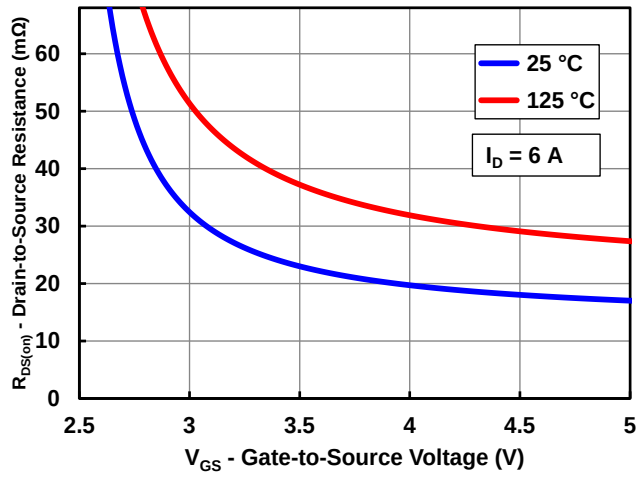


Figure 5a: Capacitance (Linear Scale)

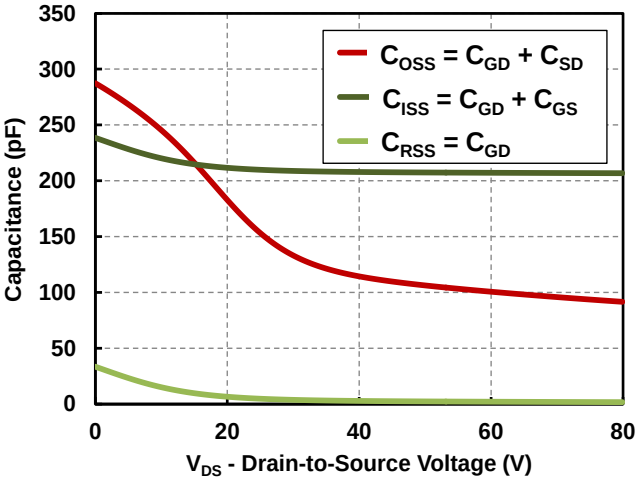


Figure 5b: Capacitance (Log Scale)

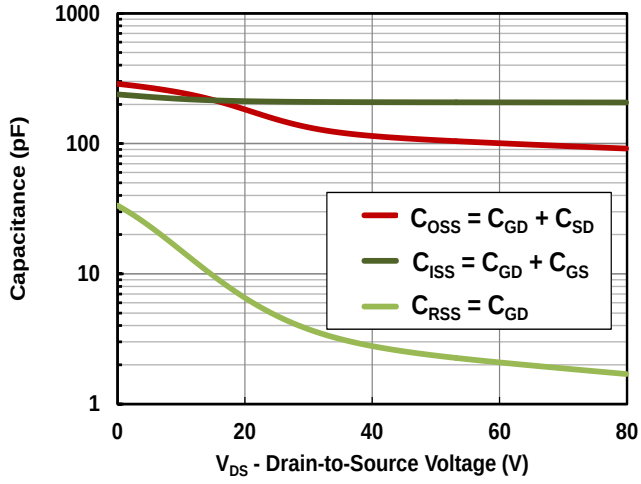


Figure 6: Gate Charge

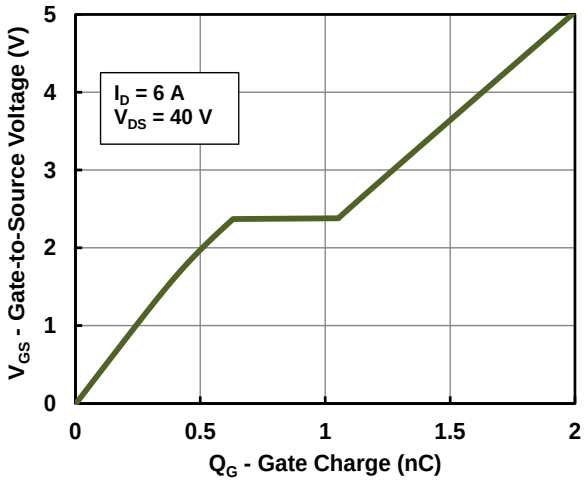


Figure 7: Reverse Drain-Source Characteristics

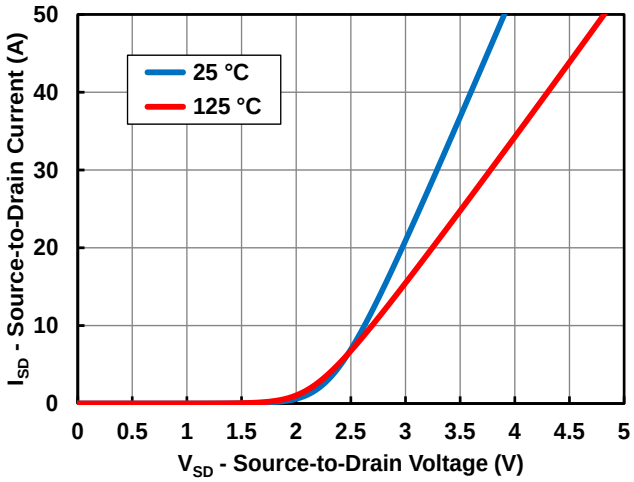


Figure 8: Normalized On Resistance vs. Temperature

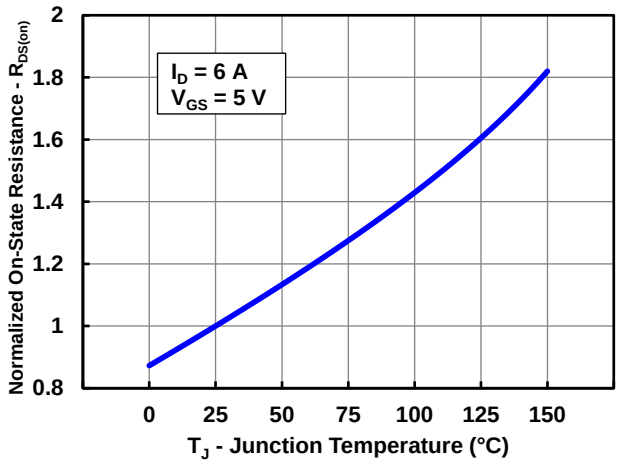


Figure 9: Normalized Threshold Voltage vs. Temperature

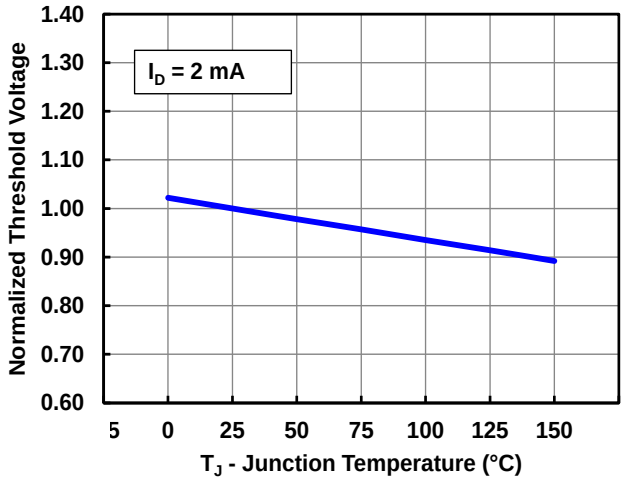
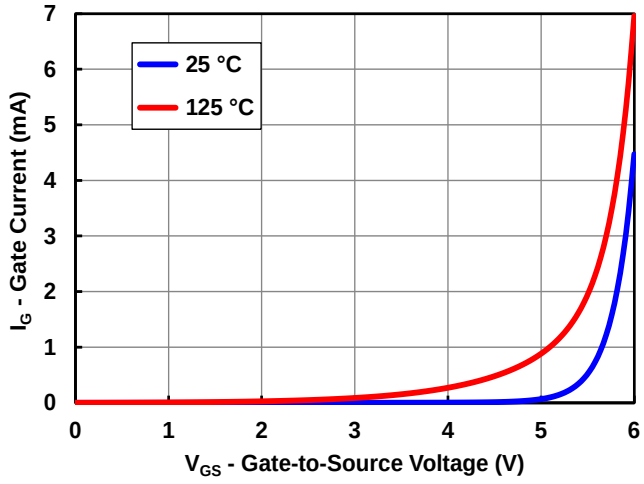
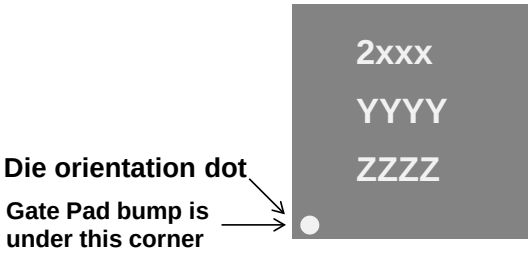


Figure 10: Gate-Source Characteristics



All measurements were done with substrate shorted to source

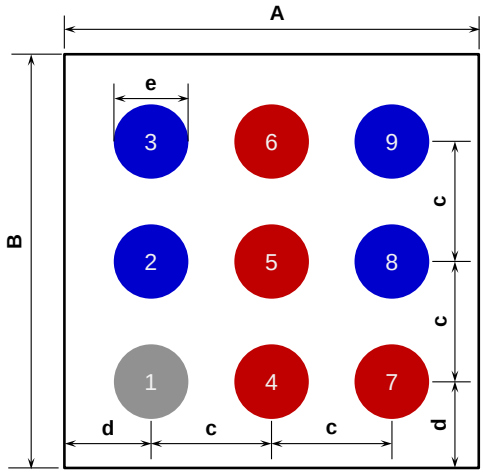
DIE MARKINGS



Part Number	Laser Marking		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2039ENGR	2XXX	YYYY	ZZZZ

DIE OUTLINE

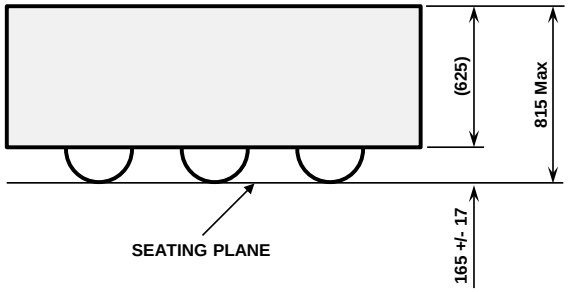
Solder Bar View



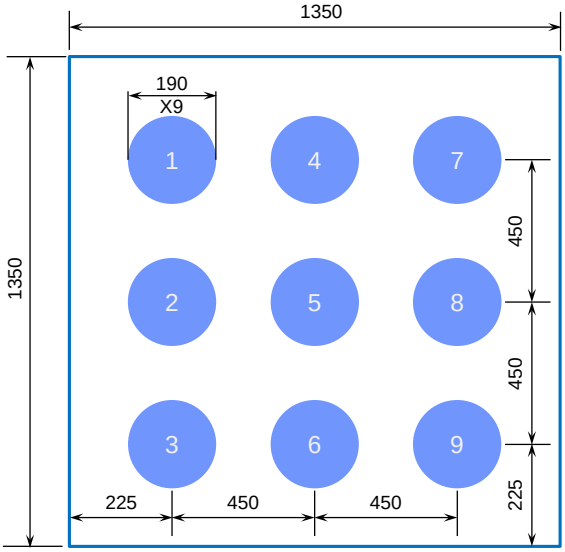
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	1320	1350	1380
B	1320	1350	1380
c	450	450	450
d	210	225	240
e	187	208	229

Pad 1 is Gate;
Pads 4, 5, 6, 7 are Drain;
Pads 2, 3, 8, 9 are Source

Side View

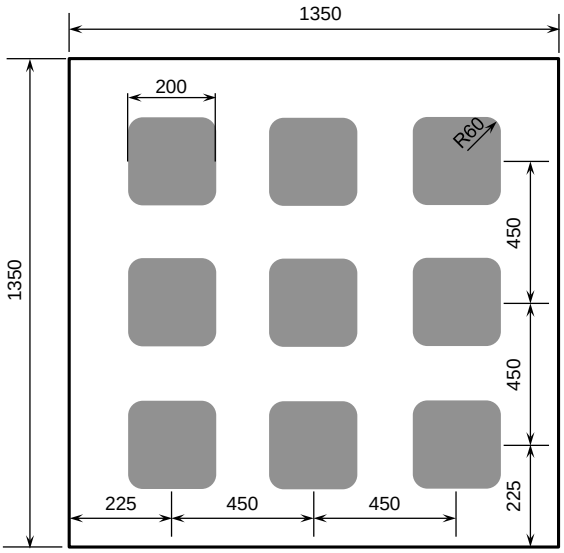


RECOMMENDED LAND PATTERN
(Units in µm)



Pad 1 is Gate;
Pads 4, 5, 6, 7 are Drain;
Pads 2, 3, 8, 9 are Source

RECOMMENDED STENCIL DESIGN
(Units in µm)



Recommended stencil should be 4mil (100µm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content

Additional assembly resources available at http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

Revised December, 2015