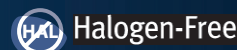
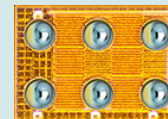


## EPC2040 – Enhancement Mode Power Transistor

 $V_{DSS}$ , 15 V $R_{DS(on)}$ , 30 mΩ $I_D$ , 3.4 A

Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 60 years. GaN's exceptionally high electron mobility and low temperature coefficient allows very low  $R_{DS(on)}$ , while its lateral device structure and majority carrier diode provide exceptionally low  $Q_G$  and zero  $Q_{RR}$ . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.



EPC2040 eGaN® FETs are supplied only in passivated die form with solder bumps  
Die Size: 0.85 mm x 1.25 mm

**Applications**

- High Speed DC-DC conversion
- LiDAR/Pulsed Power Applications
- LiDAR for Augmented Reality Applications

**Benefits**

- Ultra High Efficiency
- Ultra Low  $R_{DS(on)}$
- Ultra low  $Q_G$
- Ultra small footprint

[www.epc-co.com/epc/Products/eGaNfets/EPC2040.aspx](http://www.epc-co.com/epc/Products/eGaNfets/EPC2040.aspx)

**Maximum Ratings**

Maximum Ratings			
$V_{DS}$	Drain-to-Source Voltage (Continuous)	15	V
	Drain-to-Source Voltage (up to 10,000 5ms pulses at 150°C)	18	
$I_D$	Continuous ( $T_A = 25^\circ\text{C}$ , $R_{\theta JA} = 220^\circ\text{C/W}$ )	3.4	A
	Pulsed ( $25^\circ\text{C}$ , $T_{PULSE} = 300 \mu\text{s}$ )	28	
$V_{GS}$	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
$T_J$	Operating Temperature	-40 to 150	°C
$T_{STG}$	Storage Temperature	-40 to 150	

**Static Characteristics ( $T_J = 25^\circ\text{C}$  unless otherwise stated)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}$ , $I_D = 300 \mu\text{A}$	15			V
$I_{DSS}$	Drain Source Leakage	$V_{DS} = 12\text{ V}$ , $V_{GS} = 0\text{ V}$		10	250	$\mu\text{A}$
$I_{GSS}$	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$		0.1	1.2	mA
	Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}$		10	250	$\mu\text{A}$
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 1\text{ mA}$	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}$ , $I_D = 1.5\text{ A}$		24	30	mΩ
$V_{SD}$	Source-Drain Forward Voltage	$I_S = 0.5\text{ A}$ , $V_{GS} = 0\text{ V}$		2.2		V

All measurements were done with substrate shorted to source.

**Thermal Characteristics**

		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	5.7	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	19	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	97	°C/W

Note 1:  $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.  
See [http://epc-co.com/epc/documents/product-training/Appnote\\_Thermal\\_Performance\\_of\\_eGaN\\_FETs.pdf](http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf) for details.

Dynamic Characteristics (T<sub>J</sub> = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> = 6 V, V <sub>GS</sub> = 0 V		86	105	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			20		
C <sub>OSS</sub>	Output Capacitance			67	100	
C <sub>OSS(ER)</sub>	Effective Output Capacitance, Energy Related (Note 2)	V <sub>DS</sub> = 0 to 6 V, V <sub>GS</sub> = 0 V		106		
C <sub>OSS(TR)</sub>	Effective Output Capacitance, Time Related (Note 3)			87		
R <sub>G</sub>	Gate Resistance			0.5		Ω
Q <sub>G</sub>	Total Gate Charge	V <sub>DS</sub> = 6 V, V <sub>GS</sub> = 5 V, I <sub>D</sub> = 1.5 A		745	925	pC
Q <sub>GS</sub>	Gate to Source Charge	V <sub>DS</sub> = 6 V, I <sub>D</sub> = 1.5 A		230		
Q <sub>GD</sub>	Gate to Drain Charge			140		
Q <sub>G(TH)</sub>	Gate Charge at Threshold			165		
Q <sub>OSS</sub>	Output Charge	V <sub>DS</sub> = 6 V, V <sub>GS</sub> = 0 V		420	630	
Q <sub>RR</sub>	Source-Drain Recovery Charge			0		

Note 2: C<sub>OSS(ER)</sub> is a fixed capacitance that gives the same stored energy as C<sub>OSS</sub> while V<sub>DS</sub> is rising from 0 to 40% BV<sub>DSS</sub>.  
 Note 3: C<sub>OSS(TR)</sub> is a fixed capacitance that gives the same charging time as C<sub>OSS</sub> while V<sub>DS</sub> is rising from 0 to 40% BV<sub>DSS</sub>.

Figure 1: Typical Output Characteristics at 25°C

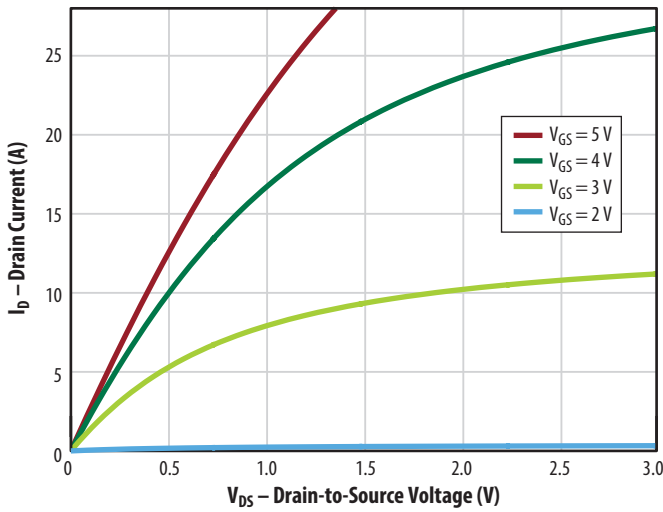


Figure 2: Transfer Characteristics

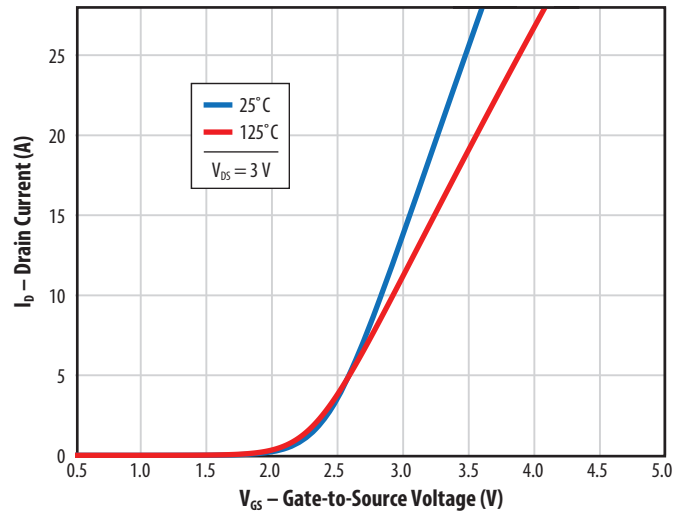


Figure 3: R<sub>DS(on)</sub> vs. V<sub>GS</sub> for Various Drain Currents

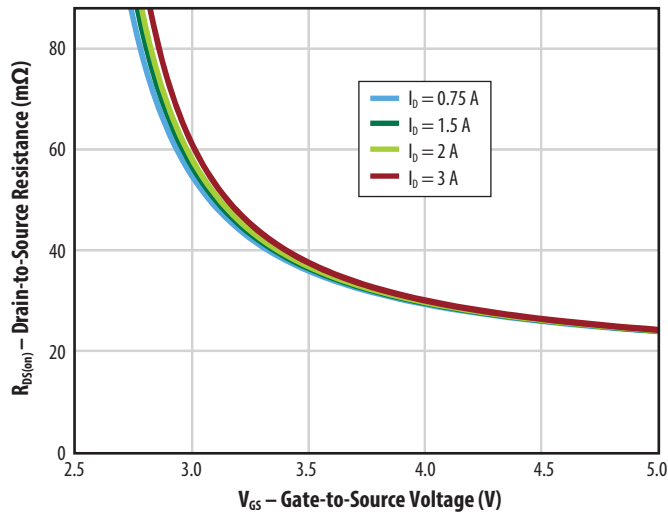


Figure 4: R<sub>DS(on)</sub> vs. V<sub>GS</sub> for Various Temperatures

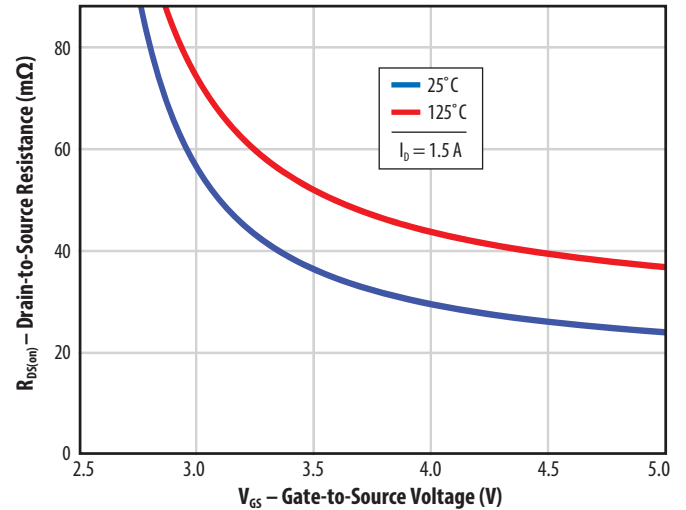


Figure 5a: Capacitance (Linear Scale)

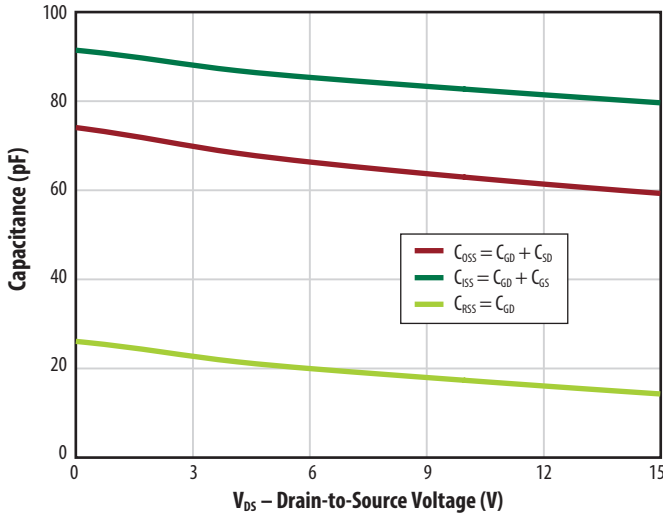


Figure 5b: Capacitance (Log Scale)

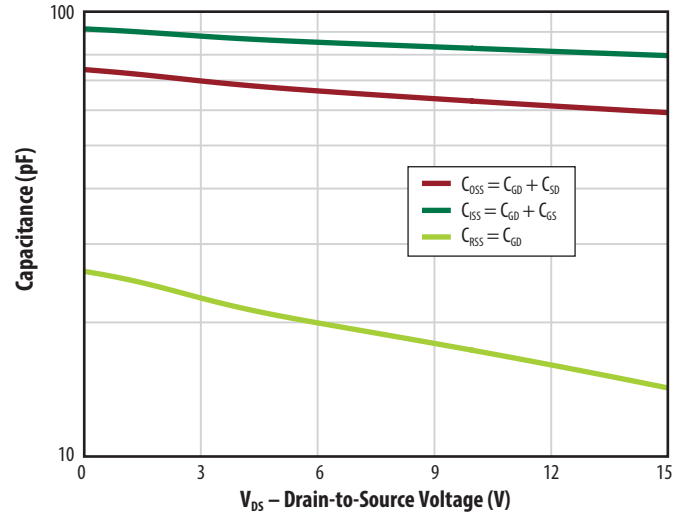


Figure 6: Gate Charge

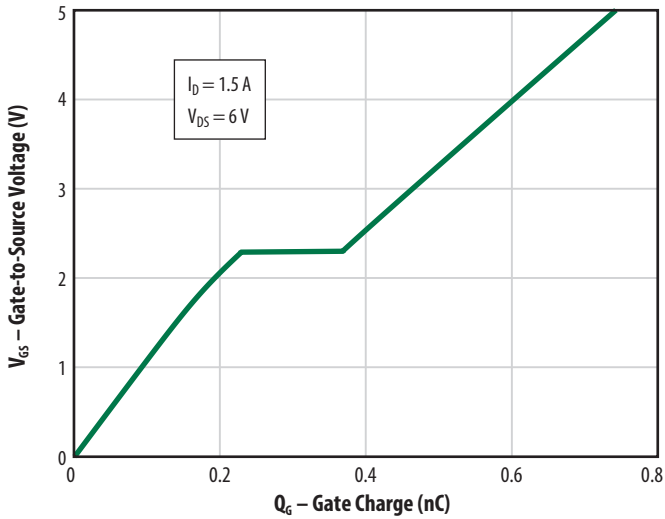


Figure 7: Reverse Drain-Source Characteristics

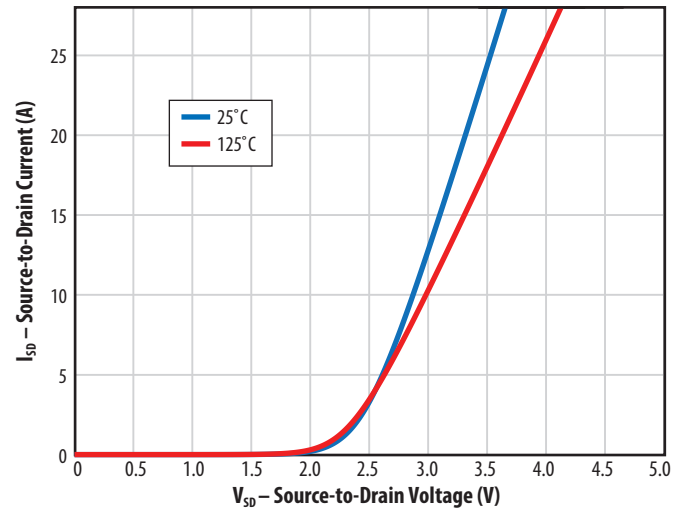


Figure 8: Normalized On-State Resistance vs. Temperature

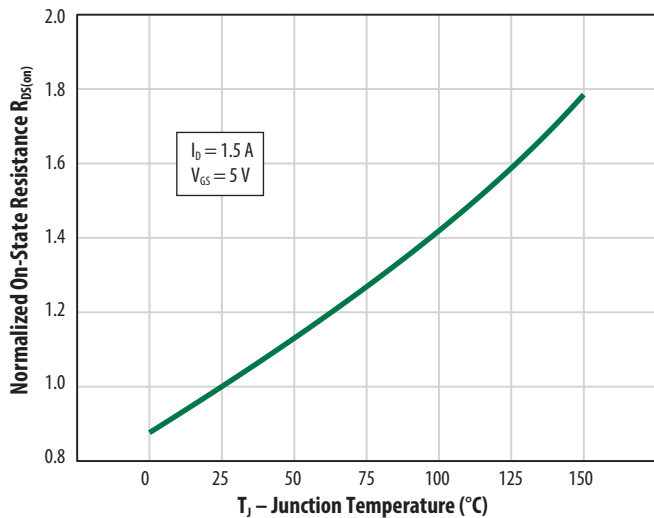
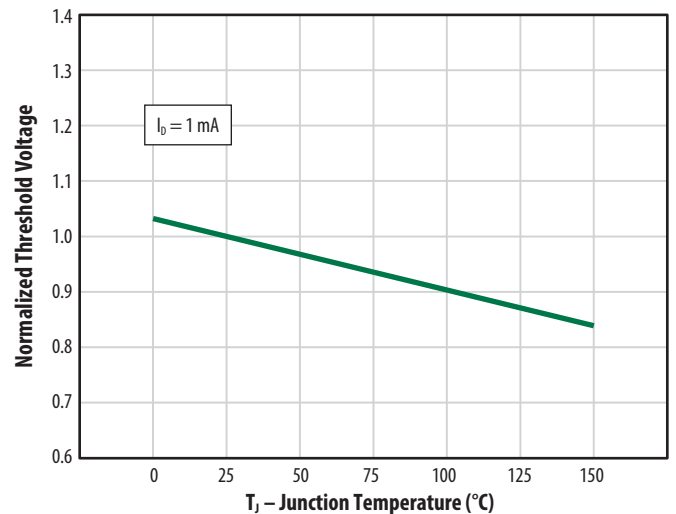


Figure 9: Normalized Threshold Voltage vs. Temperature



All measurements were done with substrate shorted to source.

Figure 10: Safe Operating Area

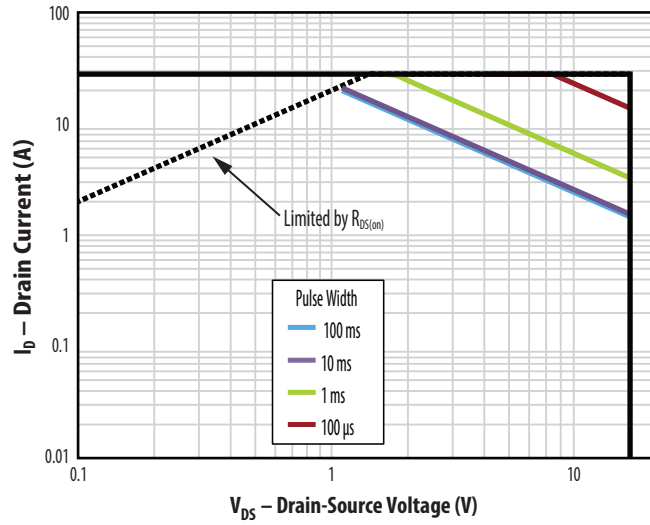
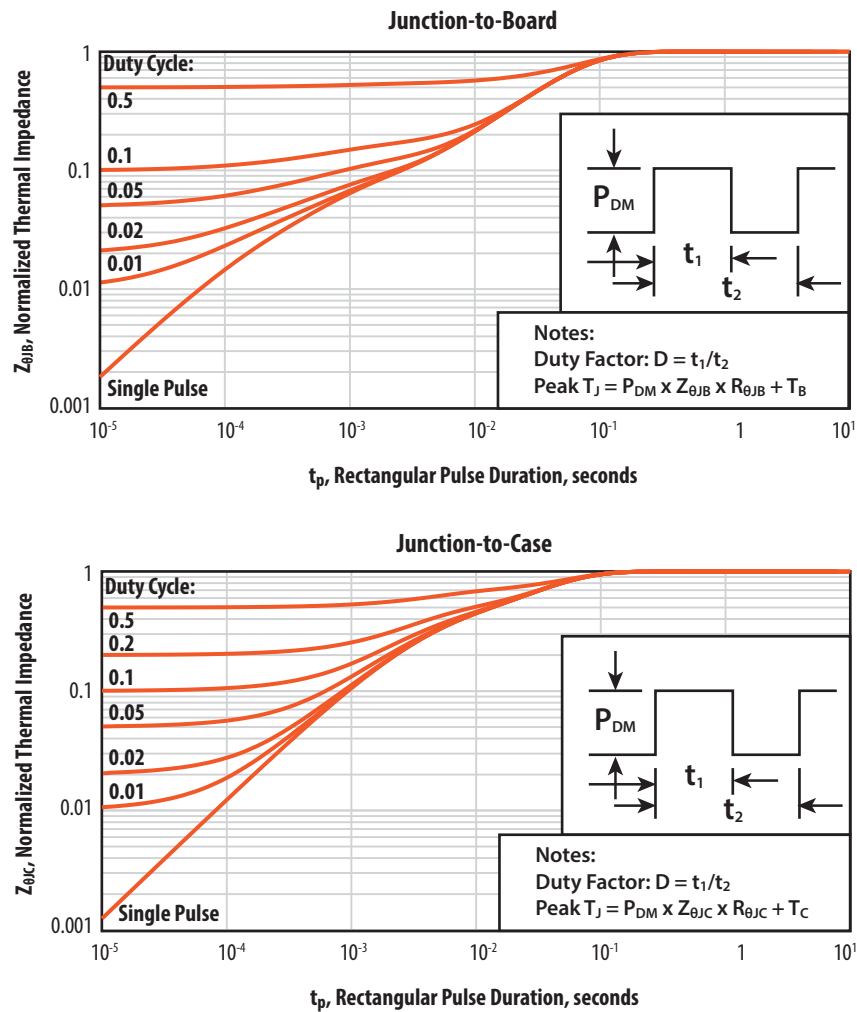
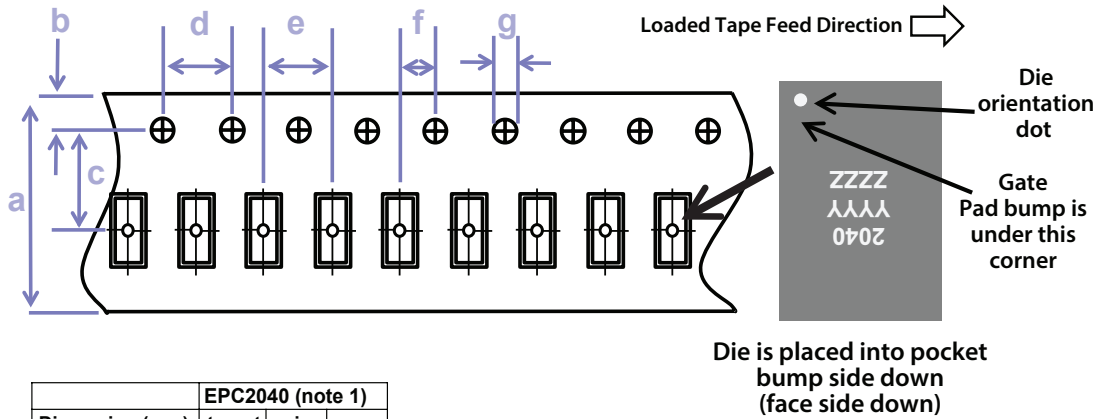
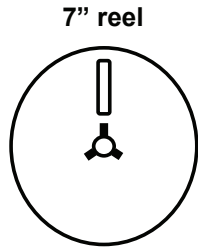


Figure 11: Transient Thermal Response Curves



**TAPE AND REEL CONFIGURATION**

4mm pitch, 8mm wide tape on 7" reel

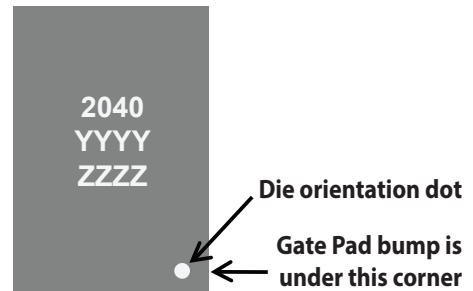


Dimension (mm)	EPC2040 (note 1)		
	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

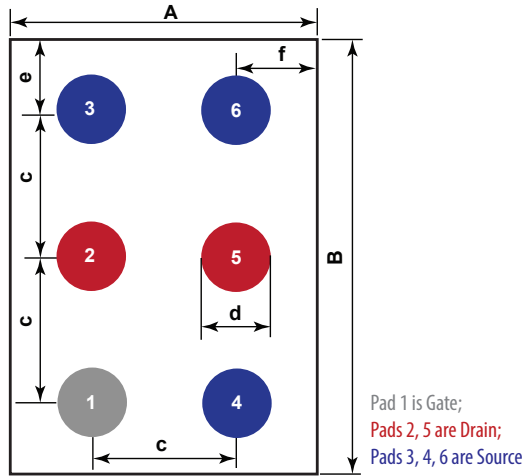
Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.  
 Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

**DIE MARKINGS**

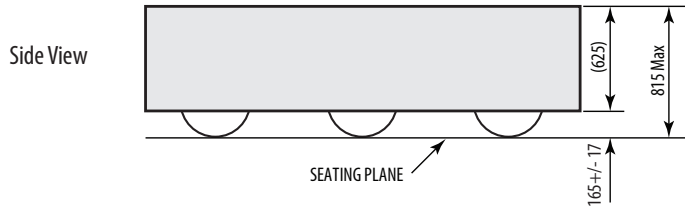
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking line 3
EPC2040	2040	YYYY	ZZZZ



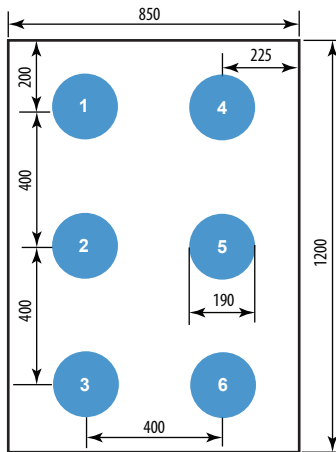
**DIE OUTLINE**  
Solder Bump View



DIM	Micrometers		
	MIN	Nominal	MAX
A	820	850	880
B	1170	1200	1230
c		400	
d	187	208	229
e	185	200	215
f	210	225	240



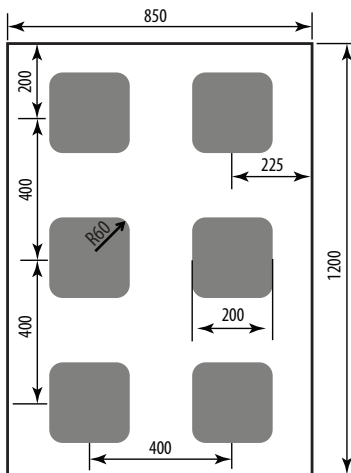
**RECOMMENDED LAND PATTERN**  
(measurements in  $\mu\text{m}$ )



The land pattern is solder mask defined  
Solder mask is 10  $\mu\text{m}$  smaller per side than bump

Pad 1 is Gate;  
Pads 2, 5 are Drain;  
Pads 3, 4, 6 are Source

**RECOMMENDED STENCIL DRAWING**  
(measurements in  $\mu\text{m}$ )



Recommended stencil should be 4mil (100  $\mu\text{m}$ ) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at  
<http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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Revised May, 2017