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FAIRCHILD SEMICONDUCTOR®

June 2011

FXL2SD106
Low-Voltage Dual-Supply 6-Bit Voltage Translator with Auto-Direction Sensing

Features

- Bi-Directional Interface between Two Levels: 1.1V and 3.6V
- Fully Configurable: Inputs and Outputs Track V_{CC} Level
- Non-Preferential Power-up; Either V_{CC} May Be Powered-up First
- Outputs Remain in 3-State until Active V_{CC} Level is Reached
- Outputs Switch to 3-State if Either V_{CC} is at GND
- Power-Off Protection
- Bus hold on Data Inputs Eliminates Need for Pull-up Resistors (Do NOT Use Resistors on the A or B Ports)
- OE and CLK IN are Referenced to V_{CCA} Voltage
- Packaged in 16-Terminal DQFN (2.5mm x 3.5mm)
- Direction Control Not Needed
- 80 Mbps Throughput Translating between 1.8V and 2.5V
- ESD Protection Exceeds:
  - 12kV HBM (B port I/O to GND) (per JESD22-A114 & Mil Std 883e 3015.7)
  - 8kV HBM (A port I/O to GND) (per JESD22-A114 & Mil Std 883e 3015.7)
  - 1kV CDM (per ESD STM 5.3)

General Description

The FXL2SD106 is a configurable dual-voltage-supply translator designed for both uni-directional and bi-directional voltage translation between two logic levels. The device allows translation between voltages as high as 3.6V to as low as 1.1V. The A port tracks the V_{CCA} level and the B port tracks the V_{CCB} level. This allows for bi-directional voltage translation over a variety of voltage levels: 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.

The device remains in 3-state until both V_{CC} reach active levels, allowing either V_{CC} to be powered-up first. Internal power-down control circuits place the device in 3-state if either V_{CC} is removed.

The OE input, when low, disables both A and B ports by placing them in a 3-state condition. The FXL2SD106 is designed so that OE and CLK IN are supplied by V_{CCA}.

The device senses an input signal on A or B port automatically. The input signal is transferred to the other port.

The FXL2SD106 is not designed for SD card applications. The internal bus hold circuitry conflicts with pull-up resistors. SD cards have internal pull-up resistors on the CD/DAT3 pins.

Ordering Information

Order Number	Package Number	Package Description
FXL2SD106BQX	MLP16E	16-Terminal Depopulated Quad Very-Thin Flat Pack, No Leads (DQFN), JEDEC MO-241, 2.5mm x 3.5mm

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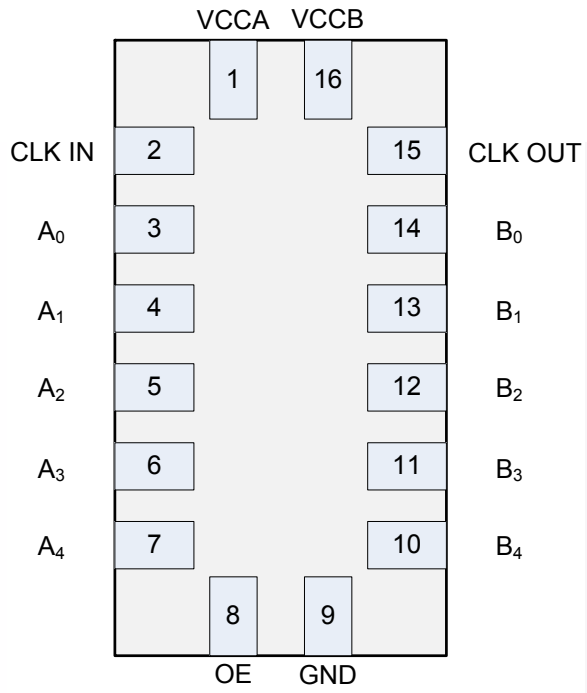
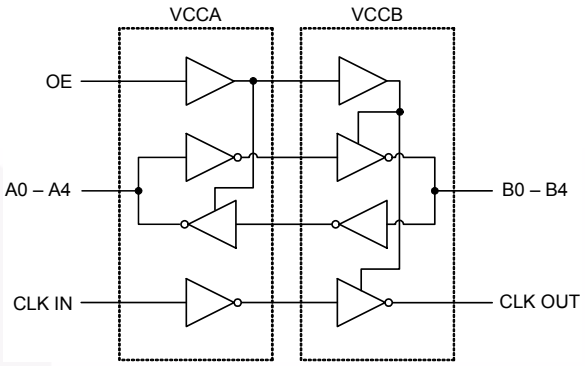
Connection Diagram



Functional Diagram



Pin Description

Number	Name	Description
1	V_{CCA}	A-Side Power Supply
2	CLK IN	A-Side Input
3–7	A_0–A_4	A-Side Inputs or 3-State Outputs
8	OE	Output Enable Input
9	GND	Ground
10–14	B_4–B_0	B-Side Inputs or 3-State Outputs
15	CLK OUT	3-State Output
16	V_{CCB}	B-Side Power Supply

Function Table

Control	Outputs
OE	
LOw Logic Level	3-State
HIGH Logic Level	Normal Operation

Power-Up/Power-Down Sequencing

FXL translators offer an advantage in that either V_{CC} may be powered up first. This benefit derives from the chip design. When either V_{CC} is at 0 volts, outputs are in a high-impedance state. The control input (OE) is designed to track the V_{CCA} supply. A pull-down resistor tying OE to GND should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up / power-down. The size of the pull-down resistor is based upon the current-sinking capability of the device driving the OE pin.

The recommended power-up sequence is the following:

1. Apply power to the first V_{CC}.
2. Apply power to the second V_{CC}.
3. Drive the OE input high to enable the device.

The recommended power-down sequence is the following:

1. Drive OE input low to disable the device.
2. Remove power from either V_{CC}.
3. Remove power from other V_{CC}.

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CCA}, V_{CCB}	Supply Voltage	–0.5V to +4.6V
V_I	DC Input Voltage	
	I/O Port A	–0.5V to +4.6V
	I/O Port B	–0.5V to +4.6V
	OE, CLK IN	–0.5V to +4.6V
V_O	Output Voltage(1)	
	Outputs 3-STATE	–0.5V to +4.6V
	Outputs Active (A_n)	–0.5V to V_{CCA} + 0.5V
	Outputs Active (B_n, CLK OUT)	–0.5V to V_{CCB} + 0.5V
I_{IK}	DC Input Diode Current at $V_I < 0V$	–50mA
I_{OK}	DC Output Diode Current at	
	$V_O < 0V$	–50mA
	$V_O > V_{CC}$	+50mA
I_{OH} / I_{OL}	DC Output Source/Sink Current	–50mA / +50mA
I_{CC}	DC V_{CC} or Ground Current per Supply Pin	±100mA
T_{STG}	Storage Temperature Range	–65°C to +150°C

Note:

1. I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions(2)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CCA} or V_{CCB}	Power Supply Operating	1.1V to 3.6V
	Input Voltage	
	Port A	0.0V to 3.6V
	Port B	0.0V to 3.6V
	OE, CLK IN	0.0V to V_{CCA}
	Dynamic Output Current in I_{OH}/I_{OL} with V_{CC} at	
	3.0V to 3.6V	±18.0mA
	2.3V to 2.7V	±11.8mA
	1.65V to 1.95V	±7.4mA
	1.4V to 1.65V	±5.0mA
	1.1V to 1.4V	±2.6mA
	Static Output Current I_{OH}/I_{OL} with V_{CC} at 1.1V to 3.6V	±20.0µA
T_A	Free Air Operating Temperature	–40°C to +85°C
$\Delta t / \Delta V$	Maximum Input Edge Rate $V_{CCA/B}$ = 1.1V to 3.6V	10ns/V

Note:

2. All unused inputs and I/O pins must be held at V_{CCI} or GND.

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DC Electrical Characteristics (T_A = –40°C to +85°C)

Symbol	Parameter	V_{CCA} (V)	V_{CCB} (V)	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage	1.4–3.6	1.1–3.6	Data inputs A_n, CLK IN, OE	0.6 x V_{CCA}			V
		1.1–1.4	1.1–3.6		0.9 x V_{CCA}			
		1.1–3.6	1.4–3.6	Data inputs B_n	0.6 x V_{CCB}			
		1.1–3.6	1.1–1.4		0.9 x V_{CCB}			
V_{IL}	Low Level Input Voltage	1.4–3.6	1.1–3.6	Data inputs A_n, CLK IN, OE			0.35 x V_{CCA}	V
		1.1 –1.4	1.1–3.6				0.1 x V_{CCA}	
		1.1–3.6	1.4–3.6	Data inputs B_n			0.35 x V_{CCB}	
		1.1–3.6	1.1–1.4				0.1 x V_{CCB}	
V_{OH}[3]	High Level Output Voltage	1.65–3.6	1.1–3.6	Data outputs A_n, I_{HOLD} = –20µA	0.75 x V_{CCA}			V
		1.1–1.4	1.1–3.6			0.8		
		1.1–3.6	1.65–3.6	Data outputs B_n, I_{HOLD} = –20µA	0.75 x V_{CCB}			
		1.1–3.6	1.1–1.4			0.8		
V_{OL}[3]	Low Level Output Voltage	1.65–3.6	1.1–3.6	Data outputs A_n, I_{HOLD} = 20µA			0.2 x V_{CCA}	V
		1.1–1.4	1.1–3.6			0.3		
		1.1–3.6	1.65–3.6	Data outputs B_n, I_{HOLD} = 20µA			0.2 x V_{CCB}	
		1.1–3.6	1.1–1.4			0.3		
$I_{I(ODH)}$[4]	Bushold Input Overdrive High Current	3.6	3.6	Data inputs A_n, B_n	450			µA
		2.7	2.7		300			
		1.95	1.95		200			
		1.6	1.6		120			
		1.4	1.4		80			
$I_{I(ODL)}$[5]	Bushold Input Overdrive Low Current	3.6	3.6	Data inputs A_n, B_n	-450			µA
		2.7	2.7		-300			
		1.95	1.95		-200			
		1.6	1.6		-120			
		1.4	1.4		-80			
I_I	Input Leakage Current	1.1–3.6	3.6	OE, CLK IN, V_I = V_{CCA} or GND			±1.0	µA
I_{OFF}	Power Off Leakage Current	0	3.6	A_n, V_O = 0V to 3.6V			±2.0	µA
		3.6	0	B_n, CLK OUT, V_O = 0V to 3.6V			±2.0	
I_{OZ}[6]	3-State Output Leakage	3.6	3.6	A_n, B_n, CLK OUT, V_O = 0V or 3.6V, OE = V_{IL}			±2.0	µA
		3.6	0	A_n, V_O = 0V or 3.6V, OE = Don't Care			±2.0	
		0	3.6	B_n, CLK OUT, V_O = 0V or 3.6V, OE = Don't Care			±2.0	
$I_{CCA/B}$[7][8]	Quiescent Supply Current	1.1–3.6	1.1–3.6	V_I = V_{CCI} or GND, I_O = 0			5.0	µA
I_{CCZ}[7]	Quiescent Supply Current	1.1–3.6	1.1–3.6	V_I = V_{CCI} or GND, I_O = 0, OE = V_{IL}			5.0	µA
I_{CCA}[7]	Quiescent Supply Current	0	1.1–3.6	V_I = V_{CCB} or GND; I_O = 0			-2.0	µA
		1.1–3.6	0	V_I = V_{CCA} or GND; I_O = 0			2.0	

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DC Electrical Characteristics (T_A = –40°C to +85°C) (Continued)

Symbol	Parameter	V_{CCA} (V)	V_{CCB} (V)	Conditions	Min.	Typ.	Max.	Units
I_{CCB}[7]	Quiescent Supply Current	1.1–3.6	0	VI = V_{CCB} or GND; IO = 0			-2.0	µA
		0	1.1–3.6	VI = V_{CCA} or GND; IO = 0			2.0	

Notes:

3. This is the output voltage for static conditions. Dynamic drive specifications are given in “Dynamic Output Electrical Characteristics.”
4. An external driver must source at least the specified current to switch LOW-to-HIGH.
5. An external driver must source at least the specified current to switch HIGH-to-LOW.
6. “Don’t Care” indicates any valid logic level.
7. V_{CCI} is the V_{CC} associated with the input side.
8. Reflects current per supply, V_{CCA} or V_{CCB}.

Dynamic Output Electrical Characteristics[9]

A Port (A_n)

Output Load: C_L = 15pF, R_L > 1MΩ

		T_A = -40°C to +85°C, V_{CCA} =									
		3.0V to 3.6V		2.3V to 2.7V		1.65V to 1.95V		1.4V to 1.6V		1.1V to 1.3V	
Symbol	Parameter	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Units
t_{rise}[10]	Output Rise Time A Port		3.0		3.5		4.0		5.0	7.5	ns
t_{fall}[11]	Output Fall Time A Port		3.0		3.5		4.0		5.0	7.5	ns
I_{OHD}[10]	Dynamic Output Current High	-18.0		-11.8		-7.4		-5.0		-2.6	mA
I_{OLD}[11]	Dynamic Output Current Low	+18.0		+11.8		+7.4		+5.0		+2.6	mA

B Port (B_n, CLK OUT)

Output Load: C_L = 15pF, R_L > 1MΩ

		T_A = -40°C to +85°C, V_{CCB} =									
		3.0V to 3.6V		2.3V to 2.7V		1.65V to 1.95V		1.4V to 1.6V		1.1V to 1.3V	
Symbol	Parameter	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Units
t_{rise}[10]	Output Rise Time B Port		3.0		3.5		4.0		5.0	7.5	ns
t_{fall}[11]	Output Fall Time B Port		3.0		3.5		4.0		5.0	7.5	ns
I_{OHD}[10]	Dynamic Output Current High	-18.0		-11.8		-7.4		-5.0		-2.6	mA
I_{OLD}[11]	Dynamic Output Current Low	+18.0		+11.8		+7.4		+5.0		+2.6	mA

Notes:

9. Dynamic Output Characteristics are guaranteed, but not tested.
10. See Figure 5.
11. See Figure 6.

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AC Characteristics

V_{CCA} = 3.0V to 3.6V

		T_A = -40°C to +85°C, V_{CCB} =									
		3.0V–3.6V		2.3V–2.7V		1.65V–1.95V		1.4V–1.6V		1.1V–1.3V	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	Units
t_{PLH}, t_{PHL}	A to B	0.2	3.5	0.3	3.9	0.5	5.4	0.6	6.8	22.0	ns
	B to A	0.2	3.5	0.2	3.8	0.3	5.0	0.5	6.0	15.0	ns
t_{PLH}, t_{PHL}	CLK IN to CLK OUT		3.0		3.5		4.5		6.0	15.0	ns
t_{PZL}, t_{PZH}	OE to A, OE to B		1.7		1.7		1.7		1.7	1.7	µs
t_{skew}(12)	A Port, B Port		0.5		0.5		0.5		1.0	1.0	ns

V_{CCA} = 2.3V to 2.7V

		T_A = -40°C to +85°C, V_{CCB} =									
		3.0V–3.6V		2.3V–2.7V		1.65V–1.95V		1.4V–1.6V		1.1V–1.3V	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	Units
t_{PLH}, t_{PHL}	A to B	0.2	3.8	0.4	4.2	0.5	5.6	0.8	6.9	22.0	ns
	B to A	0.3	3.9	0.4	4.2	0.5	5.5	0.5	6.5	15.0	ns
t_{PLH}, t_{PHL}	CLK IN to CLK OUT		3.5		4.0		4.5		6.5	15.0	ns
t_{PZL}, t_{PZH}	OE to A, OE to B		1.7		1.7		1.7		1.7	1.7	µs
t_{skew}(12)	A Port, B Port		0.5		0.5		0.5		1.0	1.0	ns

V_{CCA} = 1.65V to 1.95V

		T_A = -40°C to +85°C, V_{CCB} =									
		3.0V–3.6V		2.3V–2.7V		1.65V–1.95V		1.4V–1.6V		1.1V–1.3V	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	Units
t_{PLH}, t_{PHL}	A to B	0.3	5.0	0.5	5.5	0.8	6.7	0.9	7.5	22.0	ns
	B to A	0.5	5.4	0.5	5.6	0.8	6.7	1.0	7.0	15.0	ns
t_{PLH}, t_{PHL}	CLK IN to CLK OUT		4.5		4.5		6.3		6.7	15.0	ns
t_{PZL}, t_{PZH}	OE to A, OE to B		1.7		1.7		1.7		1.7	1.7	µs
t_{skew}(12)	A Port, B Port		0.5		0.5		0.5		1.0	1.0	ns

V_{CCA} = 1.4V to 1.6V

		T_A = -40°C to +85°C, V_{CCB} =									
		3.0V–3.6V		2.3V–2.7V		1.65V–1.95V		1.4V–1.6V		1.1V–1.3V	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	Units
t_{PLH}, t_{PHL}	A to B	0.5	6.0	0.5	6.5	1.0	7.0	1.0	8.5	22.0	ns
	B to A	0.6	6.8	0.8	6.9	0.9	7.5	1.0	8.5	15.0	ns
t_{PLH}, t_{PHL}	CLK IN to CLK OUT		6.0		6.5		6.7		8.5	15.0	ns
t_{PZL}, t_{PZH}	OE to A, OE to B		1.7		1.7		1.7		1.7	1.7	µs
t_{skew}(12)	A Port, B Port		1.0		1.0		1.0		1.0	1.0	ns

Note:

12. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (A_n or B_n) and switching with the same polarity (Low-to-High or High-to-Low). See Figure 8.

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Maximum Data Rate[13][14]

V_{CCA}	T_A = -40°C to +85°C, V_{CCB} =					Units
	3.0V to 3.6V	2.3V to 2.7V	1.65V to 1.95V	1.4V to 1.6V	1.1V to 1.3V	
	Min.	Min.	Min.	Min.	Typ.	
V_{CCA} = 3.0V to 3.6V	100	100	80	60	20	Mbps
V_{CCA} = 2.3V to 2.7V	100	100	80	60	20	Mbps
V_{CCA} =1.65V to 1.95V	80	80	60	40	20	Mbps
V_{CCA} = 1.4V to 1.6V	60	60	40	40	20	Mbps
	Typ.	Typ.	Typ.	Typ.	Typ.	
V_{CCA} = 1.1V to 1.3V	20	20	20	20	20	Mbps

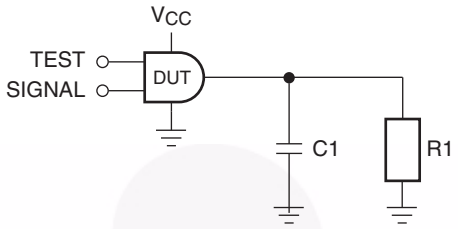
Note:

13. Maximum data rate is guaranteed but not tested.

14. Maximum data rate is specified in megabits per second. See Figure 7. It is equivalent to two times the F-toggle frequency, specified in megahertz. For example, 100 Mbps is equivalent to 50 MHz.

Capacitance

Symbol	Parameter		Conditions	T_A = +25°C Typical	Units
C_{IN}	Input Capacitance, OE, CLK IN		VccA = VccB = GND	4	pF
$C_{I/O}$	Input/Output Capacitance	A_n	VccA = VccB = 3.3V, OE = VccA	5	pF
		B_n, CLK OUT		6	
C_{PD}	Power Dissipation Capacitance		VccA = VccB = 3.3V, Vi = 0V or Vcc, f = 10MHz	25	pF



Test	Input Signal	Output Enable Control
t_{PLH}, t_{PHL}	Data Pulses	V_{CCA}
t_{PZL}	0V	Low to High Switch
t_{PZH}	V_{CCI}	Low to High Switch

Figure 1. AC Test Circuit

AC Load Table

V_{CCO}	CI	RI
1.2V ± 0.1V	15pF	1MΩ
1.5V ± 0.1V	15pF	1MΩ
1.8V ± 0.15V	15pF	1MΩ
2.5V ± 0.2V	15pF	1MΩ
3.3 ± 0.3V	15pF	1MΩ

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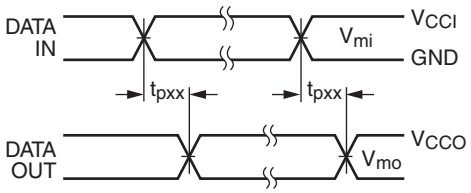
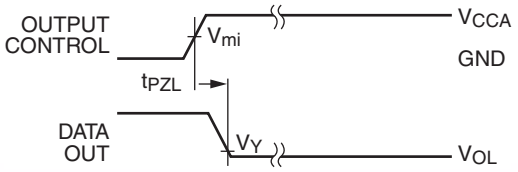


Input $t_R = t_F$ = 2.0ns, 10% to 90%

Input $t_R = t_F$ = 2.5ns, 10% to 90%, @ Vi = 3.0V to 3.6V only

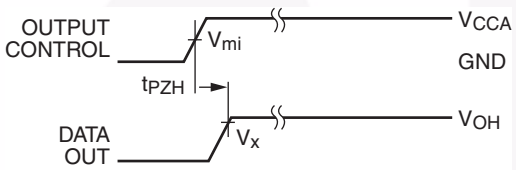
Figure 2. Waveform for Inverting and Non-inverting Functions



Input $t_R = t_F$ = 2.0ns, 10% to 90%

Input $t_R = t_F$ = 2.5ns, 10% to 90%, @ Vi = 3.0V to 3.6V only

Figure 3. 3-STATE Output Low Enable Time for Low Voltage Logic



Input $t_R = t_F$ = 2.0ns, 10% to 90%

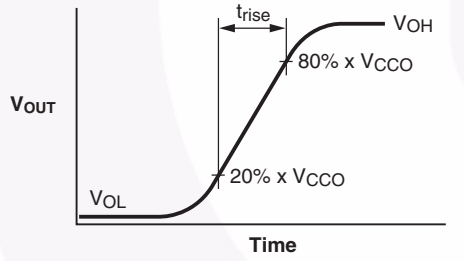
Input $t_R = t_F$ = 2.5ns, 10% to 90%, @ Vi = 3.0V to 3.6V only

Figure 4. 3-STATE Output High Enable Time for Low Voltage Logic

Symbol	Vcc
Vmi(15)	V_{CCI} / 2
Vmo	V_{CCO} / 2
VX	0.9 x V_{CCO}
VY	0.1 x V_{CCO}

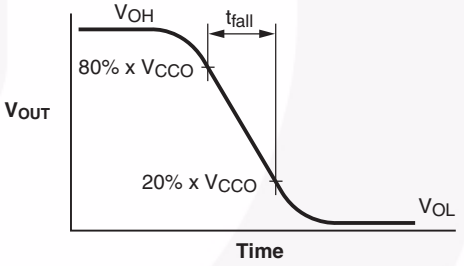
Note:

15. $V_{CCI} = V_{CCA}$ for control pin OE or Vmi = (V_{CCA} / 2).



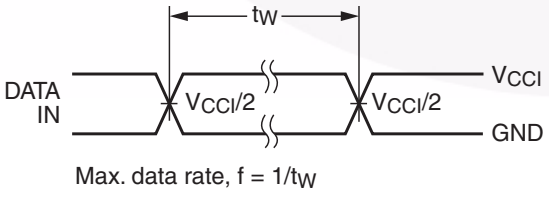
$$I_{OHD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(20\% - 80\%) \times V_{CCO}}{t_{RISE}}$$

Figure 5. Active Output Rise Time and Dynamic Output Current High



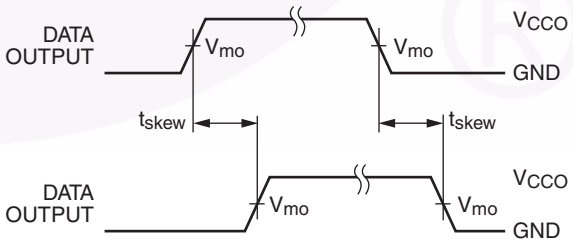
$$I_{OLD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(80\% - 20\%) \times V_{CCO}}{t_{FALL}}$$

Figure 6. Active Output Fall Time and Dynamic Output Current Low



Max. data rate, f = $1/t_W$

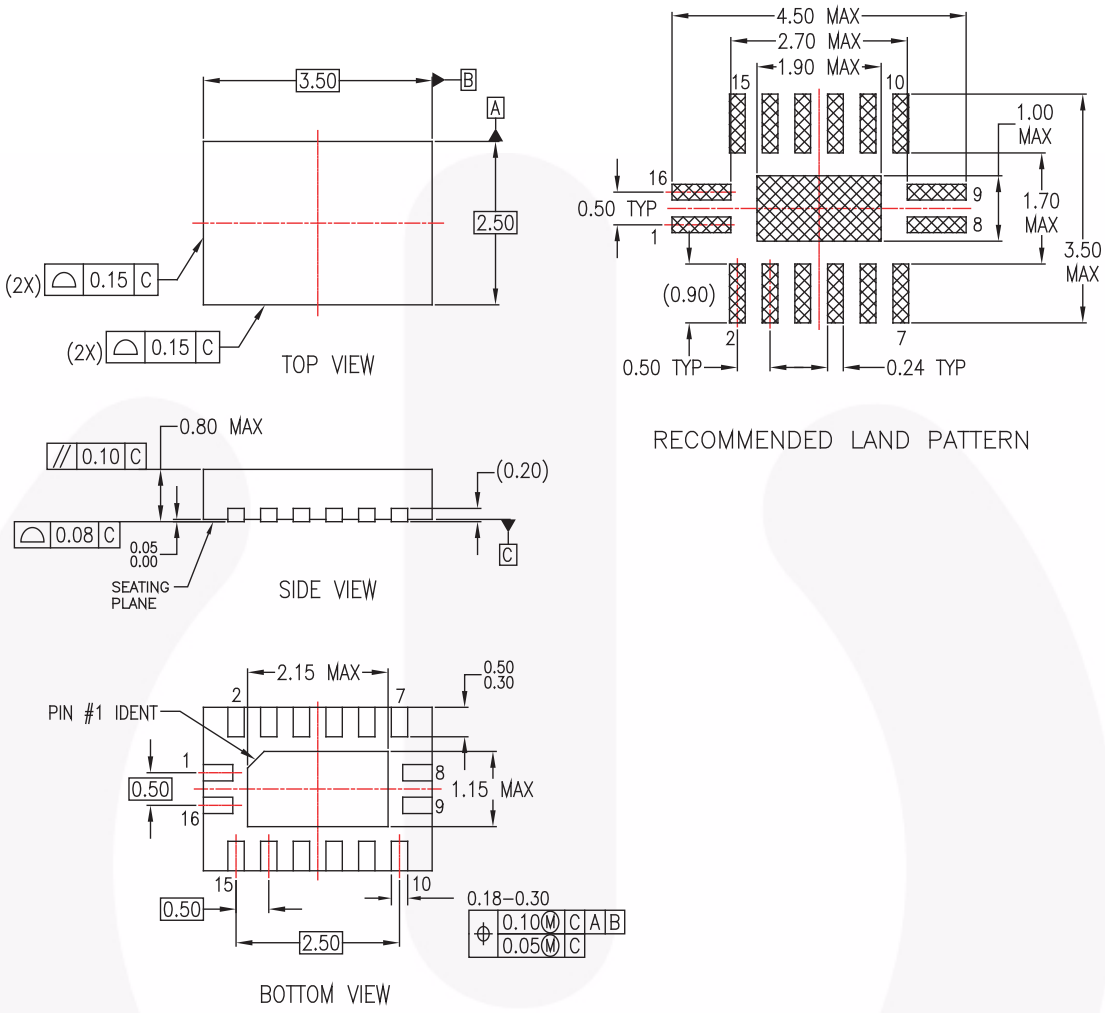
Figure 7. Maximum Data Rate



$t_{skew} = (t_{pHLmax} - t_{pHLmin})$ or $(t_{pLHmax} - t_{pLHmin})$

Figure 8. Output Skew Time

Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO–241, VARIATION AB
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP16ErevA

Figure 9. 16-Terminal Depopulated Quad, Very-Thin Flat Pack, No Leads (DQFN), JEDEC MO-241 2.5mm x 3.5mm

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