

# DDR4 (PC4) ECC LRDIMM VP9MLxx72x4xxx

Viking's DDR4 LRDIMM memory module offers lower operating voltages, higher module densities and faster speed categories than prior generation DDR3 memory. JEDEC DDR4 (JESD79-4) specification provides higher performance with improved reliability and reduced power, thereby representing a significant achievement relative to previous DRAM memory technologies.

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## REVISION HISTORY

Revision	Release Date	Description of Change	Checked By (Full Name)
A	10/07/15	Initial release	
B	3/17/17	Revise logo and color scheme. Change company address	
C	4/17/17	Add 128GB PN's	

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## Legal Information

### Legal Information

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All printed circuit boards (PCBs) have a flammability rating of UL94V-0.

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## Ordering Information and Module Configuration

Viking Part Number	Voltage	Capacity	Module Organization	Device Configuration	Device Package	DIMM Rank	Speed	CAS Latency
VP9ML2G7224HBHSB	1.2V	16GB	2Gx72	1024Mx4 (36)	FBGA	2	PC4-17000	CL15 (15-15-15)
VP9ML2G7224HBJSB	1.2V	16GB	2Gx72	1024Mx4 (36)	FBGA	2	PC4-19200	CL17 (17-17-17)
VP9ML4G7224HEHSB	1.2V	32GB	4Gx72	(1024Mx4)*2 (36)	DDP	4	PC4-17000	CL15 (15-15-15)
VP9ML4G7224HEJSB	1.2V	32GB	4Gx72	(1024Mx4)*2 (36)	DDP	4	PC4-19200	CL17 (17-17-17)
VP9ML8G7224JEHSB	1.2V	64GB	8Gx72	(2048Mx4)*2 (36)	DDP	4	PC4-17000	CL15 (15-15-15)
VP9ML8G7224JEJSB	1.2V	64GB	8Gx72	(2048Mx4)*2 (36)	DDP	4	PC4-19200	CL17 (17-17-17)
VP9ML6G7224JKHSB	1.2V	128GB	16Gx72	(4096Mx4)*2 (36)	4HTSV	4	PC4-17000	CL15 (15-15-15)
VP9ML6G7224JKJSB	1.2V	128GB	16Gx72	(4096M x4)*2 (36)	4HTSV	4	PC4-19200	CL17 (17-17-17)

### Notes:

- The lowercase letters y and z are wildcard characters that indicate DRAM vendor and die revisions and /or for customer specific locked BOMs. Refer to the Viking part number coversheet for details.

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## Features

- JEDEC Standard Power Supply
  - PC4: VDD = VDDQ = 1.2V± 5% (1.14V-1.26V)
  - External VPP = 2.5 Volt +10%, -5%
  - VDDSPD = 2.5V± 10% (2.25-2.75V)
- 288 pin Dual-In-Line Memory Module
- Edge finger connector ramp zone to reduce insertion force
- Point-to-Point topology to reduce loading
- Pseudo-open drain (POD12) DQ lines
- Write DQ CRC (Cyclic Redundancy Check)
- Internally generated VrefDQ
- ECC recovery from command and parity errors
- On-chip CA Parity detection for the command/address bus
- Programmable CAS Latency: 11,12,13,14,15,17
- Programmable CAS Write Latency (CWL).
- Programmable Additive Latency (Posted CAS)
- Per DRAM addressability is supported
- One load for address/command signals using a Registered Clock Driver (RCD)
  - Selectable Fixed burst chop (BC4) of 4 and burst length (BL8) of 8 on-the-fly (OTF) via the mode register set (MRS)
  - 8n prefetch with 2 or 4 selectable bank groups: 16 banks (4 bank groups x 4 banks per bank group)
  - Separate activation, read, write, refresh operations for each bank group
  - 7 mode registers
  - Dynamic On-Die-Termination (ODT) and ODT Park for improved signal integrity.
  - Self Refresh and several Power Down Modes
  - DLL-off mode for power savings
  - ZQ pin Self Calibration for output driver and ODT
  - System Level Timing Calibration Support via Write Leveling and Multi Purpose Register (MPR) Read Pattern
  - Serial Presence Detect with EEPROM
  - On-DIMM Thermal Sensor
  - Asynchronous Reset
  - Bidirectional Differentially Buffered Data Strokes(DQS)
  - LRDIMM dimensions within JEDEC MO-309 maximum limits
  - RoHS Compliant

## DDR4 SPEED BIN Nomenclature

Module Standard	SDRAM Standard	Clock
PC4-12800	DDR4-1600	800 MHz
PC4-14900	DDR4-1866	933 MHz
PC4-17000	DDR4-2133	1066 MHz
PC4-19200	DDR4-2400	1200 MHz

## DDR4 Timing Summary

MT/s	tCK (ns)	CAS Latency (tCK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
<b>DDR4-1600</b>	1.25	11	13.75	13.75	35	48.75	11-11-11
<b>DDR4-1866</b>	1.071	13	13.92	13.92	34	47.92	13-13-13
<b>DDR4-2133</b>	0.93	15	14.06	14.06	33	47.06	15-15-15
<b>DDR4-2400</b>	0.83	17	14.16	14.16	32	46.16	17-17-17

### Notes:

- CL = CAS Latency, tRCD = Activate –to-Command Time, tRP = Precharge Time. Refer to Speed Bin tables for details

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## Addressing

		2048Mbx4 8Gb DDP DRAM
Bank Address	# of Bank Groups	4
	BG Address	BG0~BG1
	Bank Address in a BG	BA0~BA1
Row Address		A0~A15
Column Address		A0~ A9
Page size		512B

**Note:**

Samsung Datasheet specifies 512B for x4 Device.

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## DDR4 288-pin LRDIMM Pin Wiring Assignments/Configurations

Pin#	Description	Pin#	Description	Pin#	Description	Pin#	Description	Pin#	Description	Pin#	Description
1	12V_NC	145	12V_NC	52	DQS17_c	196	DQS8_c	102	DQ38	246	VSS
2	VSS	146	VREFCA	53	VSS	197	DQS8_t	103	VSS	247	DQ39
3	DQ4	147	VSS	54	CB6	198	VSS	104	DQ34	248	VSS
4	VSS	148	DQ5	55	VSS	199	CB7	105	VSS	249	DQ35
5	DQ0	149	VSS	56	CB2	200	VSS	106	DQ44	250	VSS
6	VSS	150	DQ1	57	VSS	201	CB3	107	VSS	251	DQ45
7	DQS9_t	151	VSS	58	RESET_n	202	VSS	108	DQ40	252	VSS
8	DQS9_c	152	DQS0_c	59	VDD	203	CKE1	109	VSS	253	DQ41
9	VSS	153	DQS0_t	60	CKE0	204	VDD	110	DQS14_t	254	VSS
10	DQ6	154	VSS	61	VDD	205	RFU	111	DQS14_c	255	DQS5_c
11	VSS	155	DQ7	62	ACT_n	206	VDD	112	VSS	256	DQS5_t
12	DQ2	156	VSS	63	BG0	207	BG1	113	DQ46	257	VSS
13	VSS	157	DQ3	64	VDD	208	ALERT_n	114	VSS	258	DQ47
14	DQ12	158	VSS	65	A12/BC_n	209	VDD	115	DQ42	259	VSS
15	VSS	159	DQ13	66	A9	210	A11	116	VSS	260	DQ43
16	DQ8	160	VSS	67	VDD	211	A7	117	DQ52	261	VSS
17	VSS	161	DQ9	68	A8	212	VDD	118	VSS	262	DQ53
18	DQS10_t	162	VSS	69	A6	213	A5	119	DQ48	263	VSS
19	DQS10_c	163	DQS1_c	70	VDD	214	A4	120	VSS	264	DQ49
20	VSS	164	DQS1_t	71	A3	215	VDD	121	DQS15_t	265	VSS
21	DQ14	165	VSS	72	A1	216	A2	122	DQS15_c	266	DQS6_c
22	VSS	166	DQ15	73	VDD	217	VDD	123	VSS	267	DQS6_t
23	DQ10	167	VSS	74	CK0_t	218	CK1_t	124	DQ54	268	VSS
24	VSS	168	DQ11	75	CK0_c	219	CK1_c	125	VSS	269	DQ55
25	DQ20	169	VSS	76	VDD	220	VDD	126	DQ50	270	VSS
26	VSS	170	DQ21	77	VTT	221	VTT	127	VSS	271	DQ51
27	DQ16	171	VSS	78	EVENT_n	222	PARITY	128	DQ60	272	VSS
28	VSS	172	DQ17	79	A0	223	VDD	129	VSS	273	DQ61
29	DQS11_t	173	VSS	80	VDD	224	BA1	130	DQ56	274	VSS
30	DQS11_c	174	DQS2_c	81	BA0	225	A10/AP	131	VSS	275	DQ57
31	VSS	175	DQS2_t	82	RAS_n/A16	226	VDD	132	DQS16_t	276	VSS
32	DQ22	176	VSS	83	VDD	227	RFU	133	DQS16_c	277	DQS7_c
33	VSS	177	DQ23	84	S0_n	228	WE_n/A14	134	VSS	278	DQS7_t
34	DQ18	178	VSS	85	VDD	229	VDD	135	DQ62	279	VSS
35	VSS	179	DQ19	86	CAS_n/A15	230	NC	136	VSS	280	DQ63
36	DQ28	180	VSS	87	ODT0	231	VDD	137	DQ58	281	VSS

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Pin#	Description	Pin#	Description	Pin#	Description	Pin#	Description	Pin#	Description	Pin#	Description
37	VSS	181	DQ29	88	VDD	232	A13	138	VSS	282	DQ59
38	DQ24	182	VSS	89	S1_n	233	VDD	139	SA0	283	VSS
39	VSS	183	DQ25	90	VDD	234	A17 NC	140	SA1	284	VDDSPD
40	DQS12_t	184	VSS	91	ODT1	235	C[2] NC	141	SCL	285	SDA
41	DQS12_c	185	DQS3_c	92	VDD	236	VDD	142	VPP	286	VPP
42	VSS	186	DQS3_t	93	S2_n C[0]	237	S3_n C[1]	143	VPP	287	VPP
43	DQ30	187	VSS	94	VSS	238	SA2	144	RFU	288	VPP
44	VSS	188	DQ31	95	DQ36	239	VSS				
45	DQ26	189	VSS	96	VSS	240	DQ37				
46	VSS	190	DQ27	97	DQ32	241	VSS				
47	CB4	191	VSS	98	VSS	242	DQ33				
48	VSS	192	CB5 NC	99	DQS13_t	243	VSS				
49	CB0	193	VSS	100	DQS13_c	244	DQS4_c				
50	VSS	194	CB1	101	VSS	245	DQS4_t				
51	DQS17_t	195	VSS								

**Notes:**

- Pin 230 is defined as NC for UDIMMs and LRDIMMs. Pin 230 is defined as SAVE\_n (ADR) for NVDIMMs.
- A15 needed for 4Gbit DRAM, A16 needed for 8Gbit DRAM, A17 needed for 16Gbit DRAM
- DDR4 pin-out include the following additional pins beyond DDR3: Vpp, ACT\_n, A17, BG0, BG1, Alert\_n.
- The following DDR3 pins are no longer required for DDR4: BC#, BA2, VREFDQ
- Address A17 is only valid for 16Gbit DRAM
- RAS\_n is a multiplexed function with A16. (A16 needed for 8Gbit DRAM)
- CAS\_n is a multiplexed function with A15. (A15 needed for 4Gbit DRAM)
- WE\_n is a multiplexed function with A14

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## Input/Output Functional Descriptions

SYMBOL	TYPE	FUNCTION
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS0_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0, C1, C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table.
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4 have BG0 and BG1.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provided the row address for ACTIVATE Commands and the column address for Read/Write commands th select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.

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SYMBOL	TYPE	FUNCTION
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific datasheets to determine which DQ is used.
CB	Input / Output	Check Bit Input/ Output: Bi-directional ECC portion of data bus for x72 configurations
DQS_t, DQS_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t and DQSL_t, are paired with differential signals DQS_c and DQSL_c respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
PAR	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW.
ALERT_n	Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. IF there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
Vpp	Supply	DRAM Activation Power Supply: 2.5V (2.375V min , 2.75 max)
VREFCA	Supply	Reference voltage for CA

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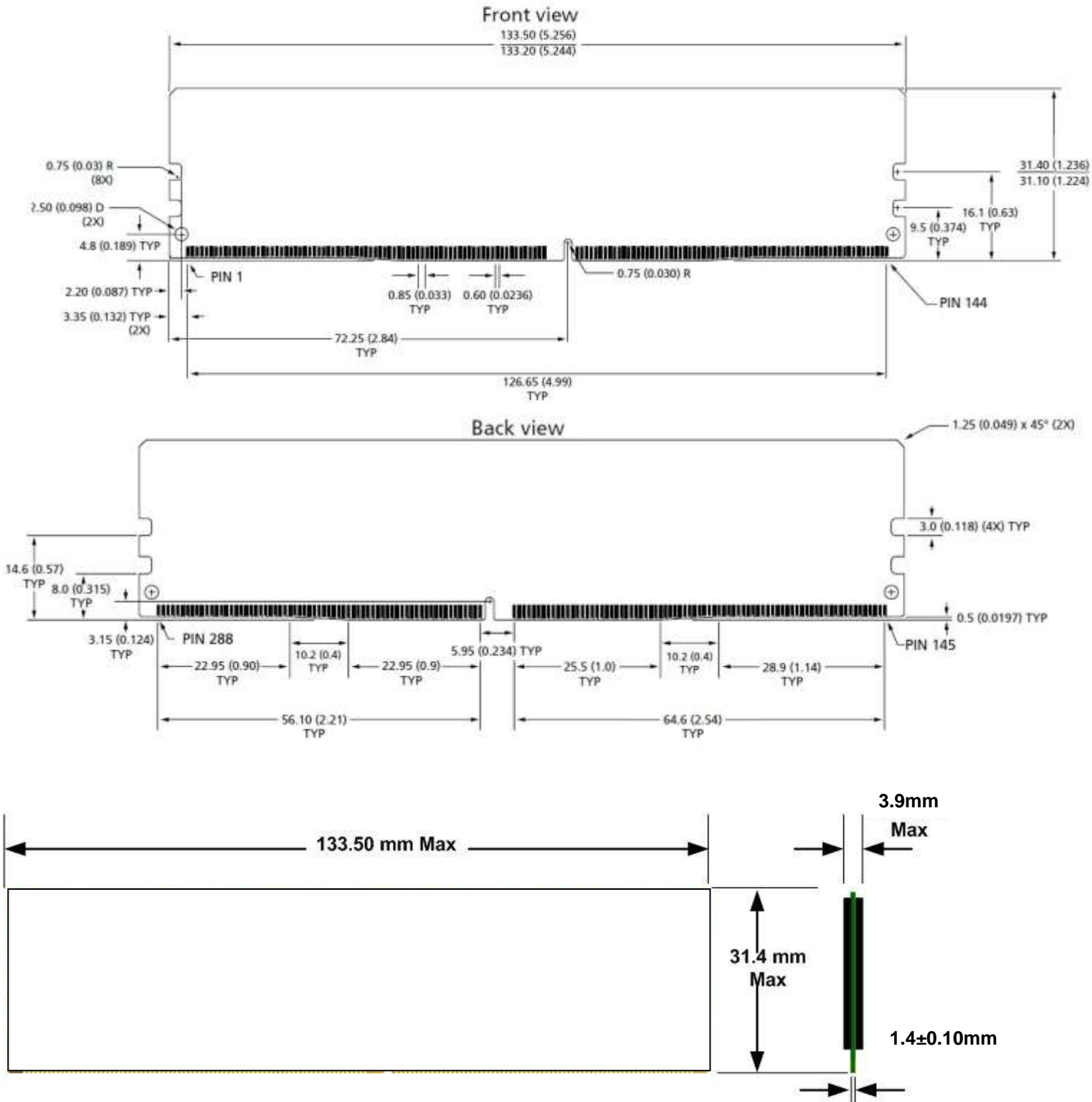
SYMBOL	TYPE	FUNCTION
ZQ	Supply	Reference Pin for ZQ calibration

**Notes:**

1. The input only pins (BG0-BG-1, BA0-BA1, A0-A17, ACT\_n, RAS\_n/A16, CAS\_n/A15, WE\_n/A14, CS\_n, CKE, ODT, and RESET\_n) do not supply termination.

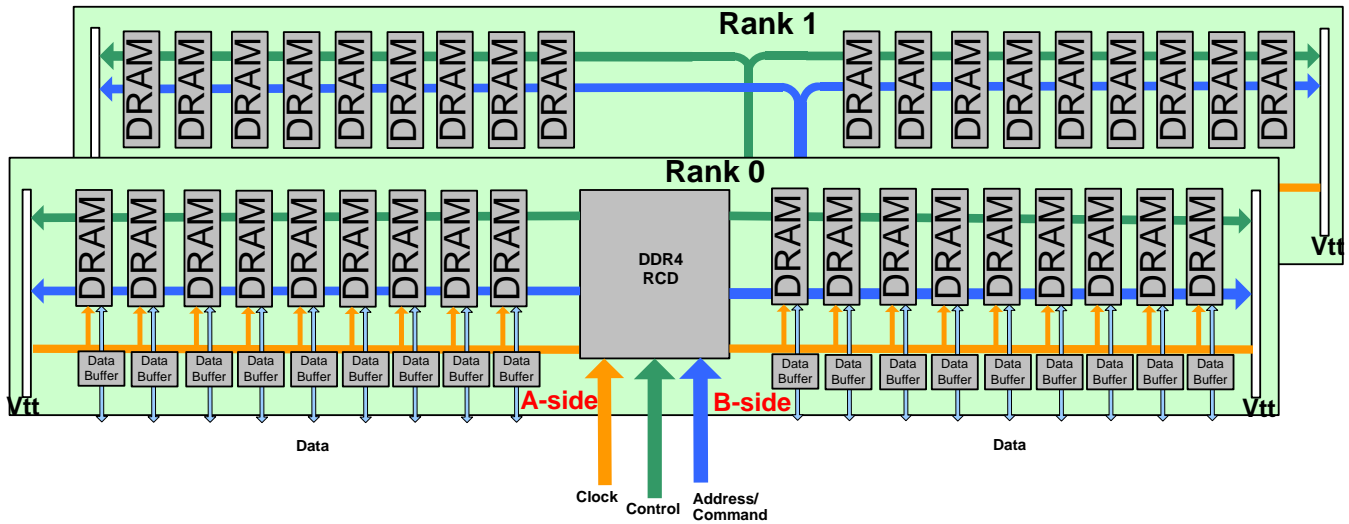
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### MECHANICAL OUTLINE



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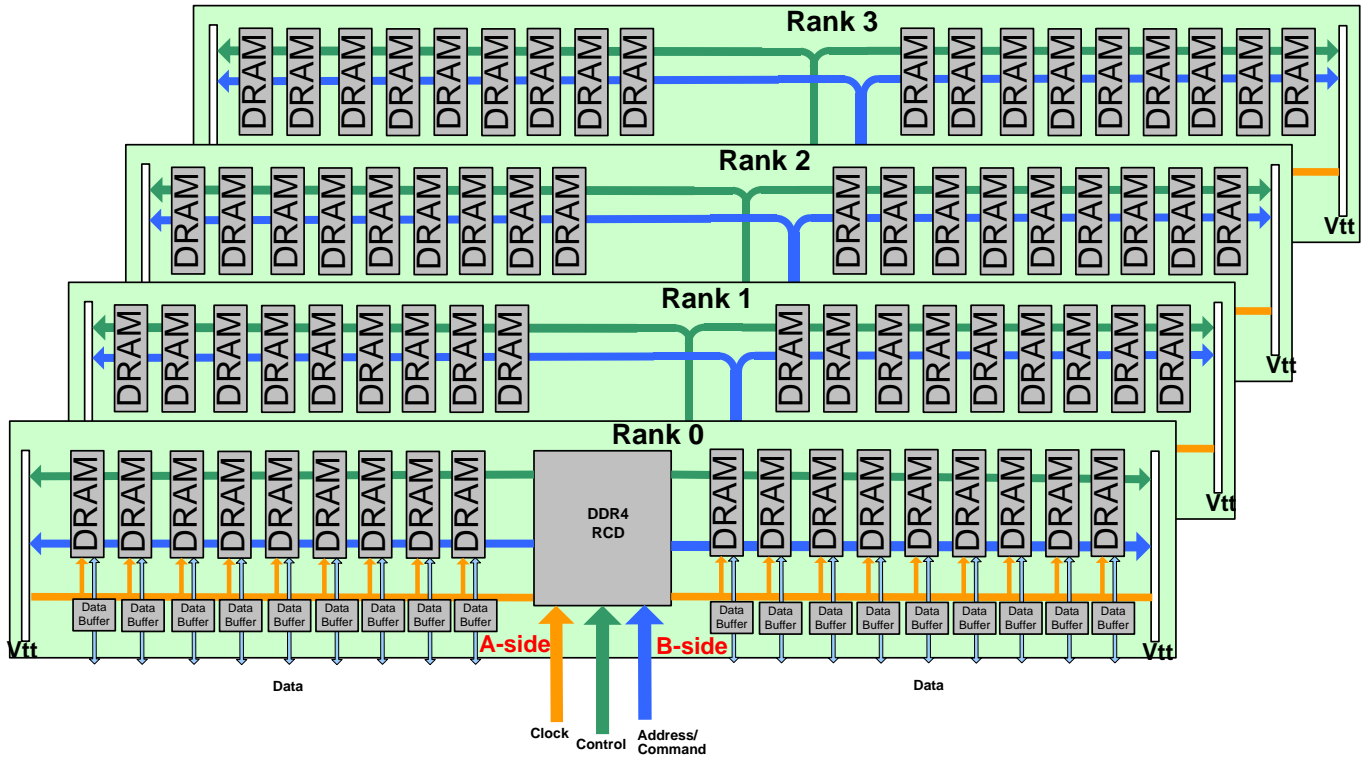
## FUNCTIONAL BLOCK DIAGRAM DUAL RANK



## DDR4 HOST MEMORY INTERFACE

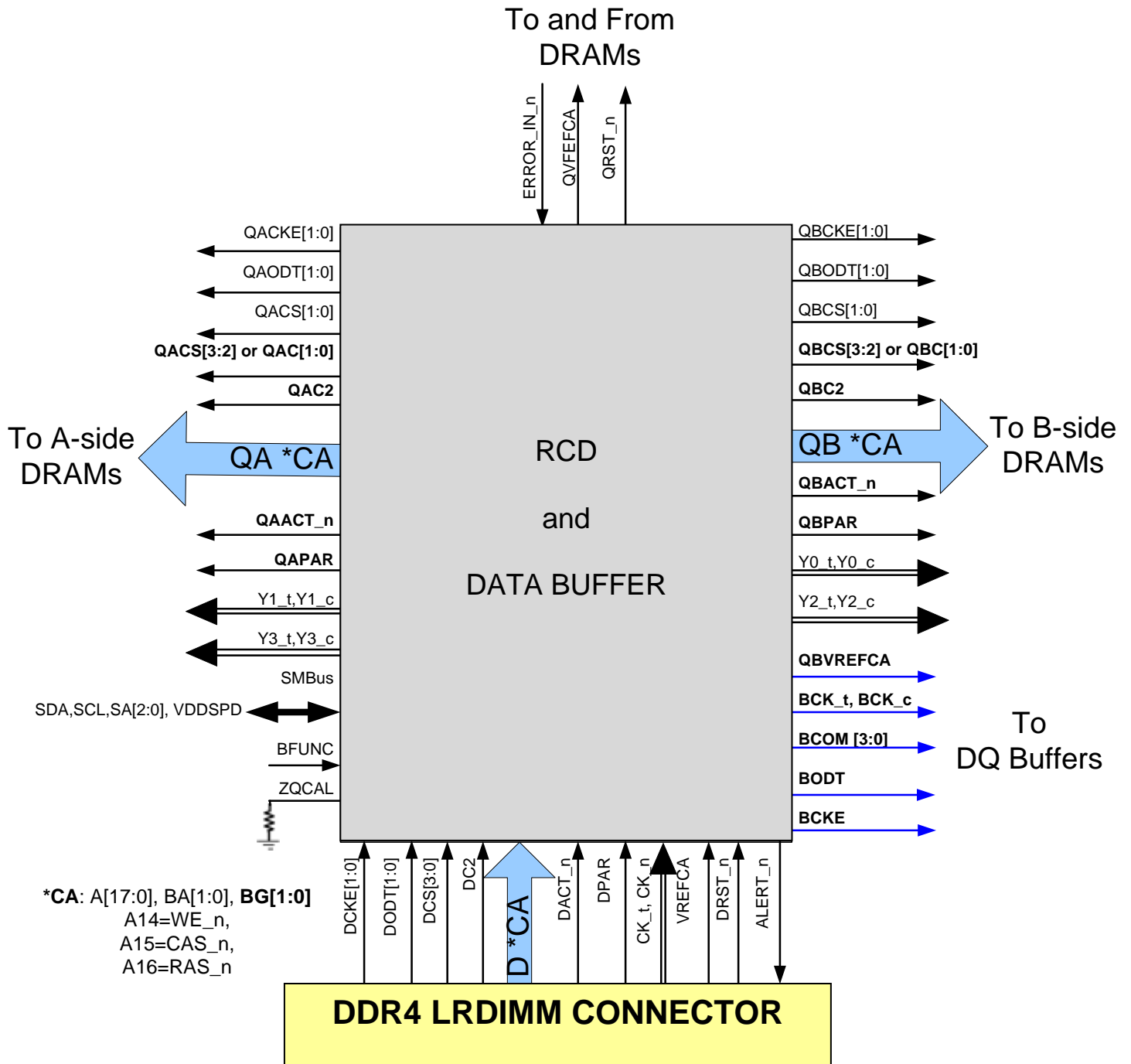
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## FUNCTIONAL BLOCK DIAGRAM QUAD RANK

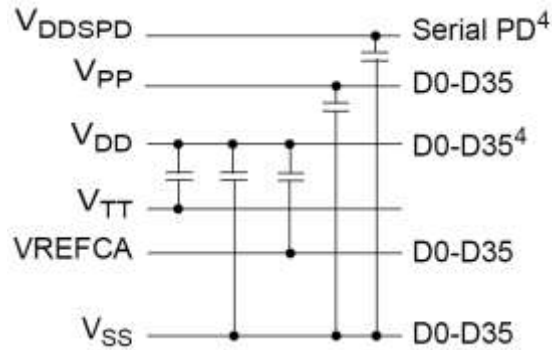


## DDR4 HOST MEMORY INTERFACE

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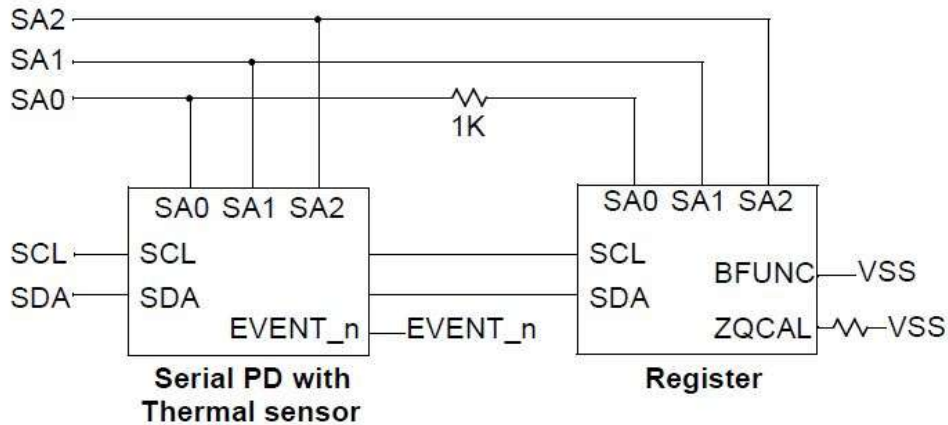
## SPD



### NOTE:

1. ZQ resistors are 240:  $\pm 1\%$ . For all other resistor values refer to the appropriate wiring diagram.
2. See the Net Structure diagrams for all resistors associated with the command, address and control bus.
3. TEN pin of SDRAMs is tied to VSS.
4. VDDSPD is also applied to the register. VDD is also applied to the register and data buffers.

## ON DIMM Thermal Sensor



### NOTE:

1. All LRDIMMs support Thermal sensor on DIMM

### Temperature Sensor Characteristics

Grade Range	range	Temperature Sensor Accuracy			Units	NOTE
		Min.	Typ.	Max.		
B	$75 < T_a < 95$	-	$\pm 0.5$	$\pm 1.0$		-
	$40 < T_a < 125$	-	$\pm 1.0$	$\pm 2.0$		-
	$-20 < T_a < 125$	-	$\pm 2.0$	$\pm 3.0$	$^{\circ}\text{C}$	-
Resolution		0	0.25		$^{\circ}\text{C}$ /LSB	-



## Registering Clock Driver Specification

### Timing & Capacitance Values

Symbol	Parameter	Conditions	DDR4-1600/1866/2133		DDR4-2400		Units	Notes
			Min	Max	Min	Max		
fclock	Input Clock Frequency	application frequency	625	1080	625	1350	MHz	
tCH/tCL	Pulse duration, CK_t, CK_c HIGH or LOW		0.4	-	0.4	-	tck	
tACT	Inputs active time <sup>4</sup> before DRST_n is taken HIGH	DCKE0/1 = LOW and DCS0/1_n = HIGH	8	-	8	-	tck	
tPDM	Propagation delay, single-bit switching, CK_t/ CK_c to output	1.2V Operation	1	1.3	1	1.3	ns	
tDIS	output disable time	Rising edge of Yn_t to output float	0.5*tC K + tQSK1 (min)	-	0.5*tC K + tQSK1 (min)	-	ps	
tEN	output enable time	Output valid to rising edge of Yn_t	0.5*tC K - tQSK1 (max)	-	0.5*tC K - tQSK1 (max)	-	ps	
CI	Input capacitance, Data inputs	NOTE <sup>1,2</sup>	0.8	1.1	0.8	1	pF	
CCK	Input capacitance, CK_t, CK_c	NOTE <sup>1,2</sup>	0.8	1.1	0.8	1		
CIR	Input capacitance, DRST_n	VI=VDD or VSS ; VDD=1.2V	0.5	2	0.5	2		

**Note:**

1. This parameter does not include package capacitance
2. Data inputs are DCKE0/1, DODT0/1, DA0..DA17, DBA0..DBA1, DBG0..DBG1, DACT\_n, DC0..DC2, DPAR, DCS0/1\_n

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### Clock Driver Characteristics

Symbol	Parameter	Conditions	DDR4-1600/1866/2133		DDR4-2400		Units	Notes
			Min	Max	Min	Max		
t <sub>jit</sub> (cc)	Cycle-to-cycle period jitter	CK_t/CK_c stable	0	0.025 x tCK	0	0.025 x tCK	ps	
t <sub>STAB</sub>	Stabilization time		-	5	-	5	us	
t <sub>CKsk</sub>	Clock Output skew		-	10	-	10	ps	
t <sub>jit(per)</sub>	Yn Clock Period jitter		-0.025 * tCK	0.025 * tCK	-0.025 * tCK	0.025 * tCK	ps	
t <sub>jit(hper)</sub>	Half period jitter		-0.032 * tCK	0.032 * tCK	-0.032 * tCK	0.032 * tCK	ps	
t <sub>Qsk1</sub>	Qn Output to clock tolerance		-0.125 * tCK	0.125 * tCK	-0.125 * tCK	0.125 * tCK	ps	
t <sub>dynoff</sub>	Maximum re-driven dynamic clock off-set		-	50	-	45	ps	

## OVERVIEW OF DDR4 LRDIMM MODULE OPERATION

The DDR4 architecture is generally a point-to-point topology with a dedicated channel design. The highest system performance levels can be achieved when the system is configured with 1 DIMM Per Channel (1DPC). DDR4 has more features than DDR3 with a pseudo-open drain (POD12) 1.2v I/O for the data channel, trained Vref, bank groups and write CRC (Cyclic Redundancy Check). The POD12 interface only applies to the data channel. The address command channel behave like DDR3 using mid-point termination and mid-point Vref. The new bank group interleaving feature in DDR4 maximizes data transfer bandwidth.

The DDR4 LRDIMM has a Registered Clock Driver (RCD) on the address, command and control lines which are center terminated as they were in DDR3. The RCD supports both RDIMM and LRDIMM modes and the default is RDIMM mode. Mode register MR7 (Manufacturing use only to program the RCD) configures the DDR4 RCD using multi-step mode register programming. MR Mode Register Read via MPR Multi-Purpose Register contains the control word bits that select the working mode.

DDR4 DRAM use pseudo-open drain (POD12) 1.2v drivers with Vdd terminations on DQ lines to increase data rates; unlike DDR3 DRAM that uses stub-series terminated logic drivers, The DRAM addressing scheme in DDR4 is organized into bank groups, Side A and Side B. The host DDR4 memory controller interleaves (multiplexes) among the bank groups to achieve high data rates. DDR4 architecture is a 8n prefetch with bank groups, including the use of two or four selectable bank groups. This will permit the DDR4 memory devices to have separate activation, read, write or refresh operations simultaneously underway in each of the unique bank groups to improve overall memory efficiency and bandwidth, especially when small memory granularities are used.

The data written to the DIMM is read back the same way. However when writing to the internal registers with a "load mode" operation, a specific address is required. This requires the controller to know if the rank is mirrored or not. There is a bit assignment in the SPD that indicates whether the module has been designed with a mirrored feature or not.

DDR4 offers ECC recovery from command and parity errors to prevent the host system from crashing. The use of CRC parity is an optional feature on address command and data; (Error command blocking when parity enabled and post CA parity. If the DIMM does not support CRC, the values of 0x00 will fill the CRC table. The new CA parity feature on the command/address bus provides a low-cost method of verifying the integrity of command and address transfers over a link, for all operations.

Some of the main attributes of DDR4 memory are:

- 1) The ACT\_n activate pin replaces RAS#, CAS#, and WE# commands
- 2) PAR and Alert\_n for error checking
- 3) Bank group Interleaving
- 4) Improved training modes upon power-up
- 5) Nominal and dynamic ODT: Improvements to the ODT protocol and a new Park Mode allow for a nominal termination and dynamic write termination without having to drive the ODT pin
- 6) DQ bus gear-down mode for 2667Mhz data rates and beyond
- 7) External VPP at 2.5V (for wordline boost)
- 8) 1.2V VDD power with power-saving features that include MPSM Maximum Power Savings Mode, Low Power Auto Self Refresh, Temperature Controlled Refresh, Fine Granularity Refresh, CMD/ADDT latency and DLL off mode
- 9) Internally generated VrefDQ and Calibration.
  - VrefDQ is supplied by the DRAM internally
  - VrefCA is supplied by the board

### Important Note:

Longer boot-up times may be experienced in certain situations for controller initiated functions such as VrefDQ calibration, write leveling and other trainings for the DIMM.

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## DDR4 MODE REGISTERS

	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
<b>MR0</b>	RFU	Write Recovery and RTP			DLL Reset	Test Mode	CAS Latency CL			Burst Type	CL	Burst Length BL	
<b>MR1</b>	Qoff	TDQS	Rtt_NOM			Write Leveling	RFU	RFU	Additive Latency		Ron		DLL Enable
<b>MR2</b>	Write CRC	RFU	Rtt_WR		RFU	Auto Self Refresh		CWL			RFU	RFU	RFU
<b>MR3</b>	MPR Read Format		Write CMD Latency with CRC and DM		Fine Granularity Refresh			Temp Sensor	Per-DRAM Addr Mode	Gear down	MPR Enable	MPR Page	
<b>MR4</b>	Write Preamble	Read Preamble	Read Preamble Training Enable	Self Refresh Abort Enable	CS-to-Address Latency CAL			RFU	VrefDQ Monitor Enable	Temp Refresh Mode	Temp. Refresh Range	Max Power Down Enable	RFU
<b>MR5</b>	Read DBI Enable	Write DBI Enable	Data Mask Enable	Parity Persistent Error	Rtt_PARK			ODT input in Power Down	Panty Error Status	CRC Error Clear	CMD Address Parity Latency		
<b>MR6</b>	tCCD_L and tDLLK Timing			RFU	RFU	VrefDQ Training enable	VrefDQ Training Range	VretDQ Training Value					
<b>MR7</b>	<b>Manufacturing use only to program the RCD</b>												

### Notes:

1. Refer to JEDEC documentation for detail of the control/status bits.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT	NOTES
Voltage on any pin relative to GND	Vin, Vout	-0.3 ~ 1.5	V	1,
Voltage on VDD supply relative to GND	VDD	-0.3 ~ 1.5	V	1,3
Voltage on VDDQ supply relative to GND	VDDQ	-0.3 ~ 1.5	V	1,3
Voltage on VPP supply relative to GND	VPP	-0.3 ~ 3.0	V	4
Module operating temperature (ambient)	Topr	0 ~ 55	°C	1,5
Storage temperature	Tstg	-55 ~ +100	°C	1,2

#### Notes:

1. Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51- 2 standard.  
may affect reliability.
3. VDD and VDDQ must be within 300 mV of each other at all times and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV.
4. VPP must be equal or greater than VDD/VDDQ at all times.
5. Refer to JEDEC JC451 specification.

### DRAM Component Operating Temperature Range

SYMBOL	PARAMETER	RATING	UNITS	NOTES
Toper	Normal Operating Temperature Range	0 to 85	°C	1,2
	Extended Temperature Range	85 to 95	°C	1,3

#### Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
  - a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability.
  - b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). DDR4 SDRAM's support Auto Self-Refresh and in Extended Temperature Range and please refer to component datasheet and/or the DIMM SPD for tREFI requirements in the Extended Temperature Range

### tREFI by Device Density

PARAMETER	SYMBOL	8Gb	16Gb	UNITS	
Average periodic refresh interval	tREFI	0°C ≤ Tcase ≤ 85°C	7.8	7.8	μs
		85°C ≤ Tcase ≤ 95°C	3.9	3.9	μs

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## AC & DC Operating Conditions

### DC OPERATING CONDITIONS AND CHARACTERISTICS (POD12)

SYMBOL	PARAMETER	RATING			UNITS	NOTES
		Min	Typ	Max		
VDD	Supply Voltage VDD: PG4:1.2V±5%, PG4L: 1.05 (TBD)	1.14	1.2	1.26	v	1,2,3
VDDQ	Supply Voltage for Output. Values in ( ) are at 70% of VDD	1.14 (0.798)	1.2 (0.84)	1.26 (0.882)	v	1
VPP	2.5V +10%, -5%	2.375	2.5	2.75	v	3
VDDSPD	2.5V± 10%	2.25	2.5	2.75	v	

#### Notes:

- POD12 1.2 V Pseudo Open Drain Interface has a VDDQ value of 1.2V but the reference voltage allows POD12 to be used with other VDDQ values. POD12 signals have pull-up-only parallel input termination and have an asymmetric output drive impedance. For example, if the output drivers were using a 60 ohm pull-up drive impedance then the pull-down drivers would be expected to produce a 40 ohm pull-down drive impedance. POD12 does not explicitly call for series termination resistors, so it is suitable for point-to-point as well as multi-drop stub environments which may require some additional termination.
1. JESD8-24 specifies Vref to be 70% of VDDQ. Under all conditions VDDQ must be less than or equal to VDD.
  2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
  3. DC bandwidth is limited to 20MHz.

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## DC CHARACTERISTICS, IDD CURRENTS

### IDD DEFINITIONS

SYMBOL	DDR4 IDD, IDDQ, and IPP Specs
IDD0A	Operating One Bank Active-Precharge Current (AL=CL-1)
IPP0	Operating One Bank Active-Precharge IPP Current
IDD1A	Operating One Bank Active-Read-Precharge Current (AL=CL-1)
IPP1	Operating One Bank Active-Read-Precharge IPP Current
IDD2NA	Precharge Standby Current (AL=CL-1)
IPP2N	Precharge Standby IPP Current
IDD2NL	Precharge Standby Current with CAL enabled
IDD2NG	Precharge Standby Current with Gear Down mode enabled
IDD2ND	Precharge Standby Current with DLL disabled
IDD2N_par	Precharge Standby Current with CA parity enabled
IPP2P	Precharge Power-Down IPP Current
IDD3NA	Active Standby Current (AL=CL-1)
IPP3N	Active Standby IPP Current
IPP3P	Active Power-Down IPP Current
IDD4RA	Operating Burst Read Current (AL=CL-1)
IDD4RB	Operating Burst Read Current with Read DBI
IPP4R	Operating Burst Read IPP Current
IDDQ4RB	(Optional) Operating Burst Read IDDQ Current with Read DBI
IDD4WA	Operating Burst Write Current (AL=CL-1)
IDD4WB	Operating Burst Write Current with Write DBI
IDD4WC	Operating Burst Write Current with Write CRC
IDD4W_par	Operating Burst Write Current with CA Parity
IPP4W	Operating Burst Write IPP Current
IPP5B	Burst Refresh Write IPP Current (1x REF)
IDD5F2	Burst Refresh Current (2x REF)
IPP5F2	Burst Refresh Write IPP Current (2x REF)
IDD5F4	Burst Refresh Current (4x REF)
IPP5F4	Burst Refresh Write IPP Current (4x REF)
IPP6N	Self Refresh IPP Current: Normal Temperature Range
IPP6E	Self Refresh IPP Current: Extended Temperature Range
IDD6R	Self-Refresh Current: Reduced Temperature Range
IPP6R	Self Refresh IPP Current: Reduced Temperature Range
IPP6A	Auto Self-Refresh IPP Current
IPP7	Operating bank Interleave Read IPP Current
IPP8	Maximum Power Down IPP Current

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**Notes:**

- 1) DDR4 IDD and IDDQ specs include the same DDR3 IDD and IDDQ specs with these exceptions:
  - a. IDD2P0 and IDD2P1 are replaced with a single IDD2P. There's no longer any difference in power for the DLL because of better DLL power management inside the DRAM device without any benefit for using slow exit.
  - b. IDD6 is renamed IDD6N Self Refresh Current: Normal Temperature Range
  - c. IDD6ET is renamed IDD6E Self-Refresh Current: Extended Temperature Range
  - d. IDD6TC is renamed IDD6AAut0 Self-Refresh Current
  - e. IDD8 is redefined from (optional) RESET Low Current to IDD8 Maximum Power Down Current, TBD
- 2) IDD values are an average (not peak) current drawn throughout the entire time that it takes to execute the set of conditions specified by JEDEC standards.
- 3) Consult with Viking for tools to help specify the Total Design Power (TDP)

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## IDD SPEC Table

IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted. IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted.

### IDD CURRENTS, DUAL RANK, 8Gbit

Symbol	DDR4-2133	DDR4-2400	Units
	15-15-15	17-17-17	
	1.2V	1.2V	
IDD0 <sup>1</sup>	874.8	891	mA
IDD0A <sup>1</sup>	918	954	mA
IDD1 <sup>1</sup>	1101.6	1144.8	mA
IDD1A <sup>1</sup>	1143	1197	mA
IDD2N <sup>2</sup>	756	792	mA
IDD2NA <sup>1</sup>	702	720	mA
IDD2NT <sup>1</sup>	702	720	mA
IDD2NL <sup>1</sup>	540	558	mA
IDD2NG <sup>1</sup>	648	666	mA
IDD2ND <sup>1</sup>	612	630	mA
IDD2N_par <sup>1</sup>	666	684	mA
IDD2P <sup>2</sup>	540	540	mA
IDD2Q <sup>2</sup>	684	720	mA
IDD3N <sup>2</sup>	1260	1260	mA
IDD3NA <sup>2</sup>	1368	1368	mA
IDD3P <sup>2</sup>	720	756	mA
IDD4R <sup>1</sup>	1881	2034	mA
IDD4RA <sup>1</sup>	1933.2	2095.2	mA
IDD4RB <sup>1</sup>	1890	2043	mA
IDD4W <sup>1</sup>	1782	1879.2	mA
IDD4WA <sup>1</sup>	1854	1963.8	mA
IDD4WB <sup>1</sup>	1782	1879.2	mA
IDD4WC <sup>1</sup>	1594.8	1634.4	mA
IDD4W_par <sup>1</sup>	1924.2	2046.6	mA
IDD5B <sup>1</sup>	4134.6	4132.8	mA
IDD5F2 <sup>1</sup>	2973.6	2995.2	mA
IDD5F4 <sup>1</sup>	2538	2561.4	mA
IDD6N <sup>2</sup>	792	792	mA
IDD6E <sup>2</sup>	1188	1188	mA
IDD7 <sup>1</sup>	4080.6	4516.2	mA
IDD8 <sup>2</sup>	360	360	mA

**Notes:**

1. One module rank in the active IDD/PP, the other rank in IDD2P/PP3N.
2. All ranks in this IDD/PP condition.
3. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR4 SDRAM devices support the following options or requirements referred to in this material.
4. Values as per Samsung Datasheet.

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### IDD CURRENTS, QUAD RANK, 8Gbit

Symbol	32GB(4Gx72) Module				Unit	NOTE
	DDR4-2133		DDR4-2400			
	15-15-15		17-17-17			
	1.2V		1.2V			
	IDD Max.	IPP Max.	IDD Max.	IPP Max.		
/DD0	2830	234	3050	234	mA	
/DD0A	2890	234	3120	234	mA	
/DD1	3460	234	3710	234	mA	
/DD1A	3510	216	3780	216	mA	
/DD2N	2590	216	2830	216	mA	
/DD2NA	2720	216	2960	216	mA	
/DD2NT	2630	216	2870	216	mA	
/DD2NL	2560	216	2780	216	mA	
/DD2NG	2650	216	2870	216	mA	
/DD2ND	2560	216	2780	216	mA	
/DD2N_par	2650	216	2870	216	mA	
/DD2P	1850	216	1940	216	mA	
/DD2Q	2520	216	2760	216	mA	
/DD3N	2750	216	3000	216	mA	
/DD3NA	2840	216	3090	216	mA	
/DD3P	2140	216	2300	216	mA	
/DD4R	4460	216	4800	216	mA	
/DD4RA	4490	216	4880	216	mA	
/DD4RB	4470	216	4840	216	mA	
/DD4W	4350	216	4680	216	mA	
/DD4WA	4420	216	4750	216	mA	
/DD4WB	4350	216	4680	216	mA	
/DD4WC	4220	216	4540	216	mA	
/DD4W_par	4510	216	4880	216	mA	
/DD5B	5040	486	5260	486	mA	
/DD5F2	4590	432	4790	432	mA	
/DD5F4	4030	360	4230	360	mA	
/DD6N	1190	288	1190	288	mA	
/DD6E	1480	288	1480	288	mA	
/DD6R	980	216	980	216	mA	
/DD6A	1190	288	1190	288	mA	
/DD7	6290	297	6540	297	mA	
/DD8	700	144	700	144	mA	

**NOTE :**

1. DIMM IDD SPEC is based on the condition that de-activated rank(IDLE) is IDD2N.
2. IDD current measure method and detail patterns are described on DDR4 component datasheet.
3. VDD and VDDQ are merged on module PCB.
4. DIMM IDD SPEC is measured with Qoff condition. (IDDQ values are not considered)

**DIMM Rank Status**

DIMM	Operating Rank	The other Rank
/DD0	/DD0	/DD2N
/DD1	/DD1	/DD2N
/DD2P	/DD2P	/DD2P
/DD2N	/DD2N	/DD2N
/DD2Q	/DD2Q	/DD2Q
/DD3P	/DD3P	/DD3P
/DD3N	/DD3N	/DD3N
/DD4R	/DD4R	/DD2N
/DD4W	/DD4W	/DD2N
/DD5B	/DD5B	/DD2N
/DD6	/DD6	/DD6
/DD7	/DD7	/DD2N
/DD8	/DD8	/DD8

## Input/Output Capacitance

### Silicon Pad I/O Capacitance

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400		Unit	NOTE
		min	max	min	max		
Cio	Input/output capacitance	0.55	1.4	0.55	1.15	pF	1,2,3
CDIO	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	pF	1,2,3,11
CDDQS	Input/output capacitance delta DQS_t and DQS_c	-	0.05	-	0.05	pF	1,2,3,5
CCK	Input capacitance, CK_t and CK_c	0.2	0.8	0.2	0.7	pF	1,3
CDCK	Input capacitance delta CK_t and CK_c	-	0.05	-	0.05	pF	1,3,4
CI	Input capacitance(CTRL, ADD, CMD pins only)	0.2	0.8	0.2	0.7	pF	1,3,6
CDI_CTRL	Input capacitance delta(All CTRL pins only)	-0.1	0.1	-0.1	0.1	pF	1,3,7,8
CDI_ADD_CMD	Input capacitance delta(All ADD/CMD pins only)	-0.1	0.1	-0.1	0.1	pF	1,2,9,10
CALERT	Input/output capacitance of ALERT	0.5	1.5	0.5	1.5	pF	1,3
CZQ	Input/output capacitance of ZQ	0.5	2.3	0.5	2.3	pF	1,3,12
CTEN	Input capacitance of TEN	0.2	2.3	0.2	2.3	pF	1,3,13

- NOTE:**
1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure tbd.
  2. DQ, DM\_n, DQS\_T, DQS\_c, TDQS\_T, TDQS\_C. Although the DM, TDQS\_T and TDQS\_C pins have different functions, the loading matches DQ and DQS
  3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
  4. Absolute value CK\_T-CK\_C
  5. Absolute value of CIO(DQS\_T)-CIO(DQS\_c)
  6. CI applies to ODT, CS\_n, CKE, A0-A17, BA0-BA1, BG0-BG1, RAS\_n/A16, CAS\_n/A15, WE\_n/A14, ACT\_n and PAR.
  7. CDI\_CTRL applies to ODT, CS\_n and CKE
  8.  $CDI\_CTRL = CI(CTRL) - 0.5 * (CI(CLK\_T) + CI(CLK\_C))$
  9. CDI\_ADD\_CMD applies to, A0-A17, BA0-BA1, BG0-BG1, RAS\_n/A16, CAS\_n/A15, WE\_n/A14, ACT\_n and PAR.
  10.  $CDI\_ADD\_CMD = CI(ADD\_CMD) - 0.5 * (CI(CLK\_T) + CI(CLK\_C))$
  11.  $CDIO = CIO(DQ,DM) - 0.5 * (CIO(DQS\_T) + CIO(DQS\_c))$
  12. Maximum external load capacitance on ZQ pin: tbd pF.
  13. TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information.

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## Electrical Characteristics and AC Timing

### Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

#### DDR4-1600 Speed Bins and Operations

Speed Bin			DDR4-1600		Unit	NOTE	
CL-nRCD-nRP			11-11-11				
Parameter	Symbol		min	max			
Internal read command to first data	tAA		13.75	18	ns	10	
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 2nCK	tAA(max) +2nCK	ns	10	
ACT to internal read or write delay time	tRCD		13.75	-	ns	10	
PRE command period	tRP		13.75	-	ns	10	
ACT to PRE command period	tRAS		35	9 x tREFI	ns	10	
ACT to ACT or REF command period	tRC		48.75	-	ns	10	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,9
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3
Supported CL Settings			10,11,12		nCK		
Supported CL Settings with read DBI			12,13,14		nCK		
Supported CWL Settings			9,11		nCK		

#### DDR4-1866 Speed Bins and Operations

Speed Bin			DDR4-1866		Unit	NOTE	
CL-nRCD-nRP			13-13-13				
Parameter	Symbol		min	max			
Internal read command to first data	tAA		13.92	18	ns	10	
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 2nCK	tAA(max) +2nCK	ns	10	
ACT to internal read or write delay time	tRCD		13.92	-	ns	10	
PRE command period	tRP		13.92	-	ns	10	
ACT to PRE command period	tRAS		34	9 x tREFI	ns	10	
ACT to ACT or REF command period	tRC		47.92	-	ns	10	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9

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Speed Bin				DDR4-1866		Unit	NOTE
CL-nRCD-nRP				13-13-13			
Parameter		Symbol	min	max			
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,9
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,6
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3
Supported CL Settings				10,11,12,13,14		nCK	
Supported CL Settings with read DBI				12,13,14,15,16		nCK	
Supported CWL Settings				9,10,11,12		nCK	

### DDR4-2133 Speed Bins and Operations

Speed Bin				DDR4-2133		Unit	NOTE
CL-nRCD-nRP				15-15-15			
Parameter		Symbol	min	max			
Internal read command to first data		tAA	14.06 (13.75) <sub>s</sub>	18	ns	10	
Internal read command to first data with read DBI enabled		tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	10	
ACT to internal read or write delay time		tRCD	14.06 (13.75) <sub>s</sub>	-	ns	10	
PRE command period		tRP	14.06 (13.75) <sub>s</sub>	-	ns	10	
ACT to PRE command period		tRAS	33	9 x tREFI	ns	10	
ACT to ACT or REF command period		tRC	47.06 (46.75) <sub>s</sub>	-	ns	10	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,9
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,7
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,7
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,7
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,7
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4

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Speed Bin				DDR4-2133		Unit	NOTE
CL-nRCD-nRP				15-15-15			
Parameter		Symbol		min	max		
CL = 16		CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16		nCK	
Supported CL Settings with read DBI				12,13,14,15,16,18,19		nCK	

### DDR4-2400 Speed Bins and Operations

Speed Bin			DDR4-2400		Unit	NOTE	
CL-nRCD-nRP			17-17-17				
Parameter		Symbol	min	max			
Internal read command to first data		tAA	14.16 (13.75) <sub>5</sub>	18	ns	10	
Internal read command to first data with read DBI enabled		tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	10	
ACT to internal read or write delay time		tRCD	14.16 (13.75) <sub>5</sub>	-	ns	10	
PRE command period		tRP	14.16 (13.75) <sub>5</sub>	-	ns	10	
ACT to PRE command period		tRAS	32	9 x tREFI	ns	10	
ACT to ACT or REF command period		tRC	46.16 (45.75) <sub>5</sub>	-	ns	10	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,9
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,8
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,8
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.938	<1.071	ns	1,2,3,4,8
	CL = 16	CL = 19	tCK(AVG)	0.938	<1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.938		
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.938	ns	1,2,3

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Speed Bin		DDR4-2400		Unit	NOTE
CL-nRCD-nRP		17-17-17			
Parameter	Symbol	min	max		
Supported CL Settings		10,11,12,13,14,15,16,17,18		nCK	
Supported CL Settings with read DBI		12,13,14,15,16,18,19,20,21		nCK	
Supported CWL Settings		9,10,11,12,14,16		nCK	

### DDR4-2666 Speed Bins and Operating Conditions

Speed Bin		DDR4-2666		Unit	NOTE
CL-nRCD-nRP		22-19-19			
Parameter	Symbol	Min	Max		
Internal read command to first data	tAA	16.5	21.5	ns	
ACT to internal read or write delay time	tRCD	14.25	-	ns	
PRE command period	tRP	14.25	-	ns	
ACT to PRE command period	tRAS	32	9 x tREFI	ns	
ACT to ACT or REF command period	tRC	46.25	-	ns	
CWL = 9,11	CL = 13	tCK(AVG)	Reserved	ns	1,2,3,4,9
CL = 14	tCK(AVG)	1.25	1.5	ns	1,2,3,8
CWL = 10,12	CL = 14	tCK(AVG)	Reserved	ns	1,2,3,4,9
CL = 15	tCK(AVG)	Reserved	ns	1,2,3,4,9	
CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,9
CWL = 11,14	CL = 16	tCK(AVG)	Reserved	ns	1,2,3,4,9
CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,9
CL = 20	tCK(AVG)	0.937	<1.071	ns	1,2,3,9
CWL = 12,16	CL = 18	tCK(AVG)	Reserved	ns	1,2,3,4,9
CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,9
CL = 22	tCK(AVG)	0.833	<0.937	ns	1,2,3,9
CWL = 14,18	CL = 20	tCK(AVG)	Reserved	ns	1,2,3,4,9
CL = 22	tCK(AVG)	0.75	0.833	ns	1,2,3,4,9
CL = 24	tCK(AVG)	0.75	0.833	ns	1,2,3,9
Supported CL Settings	11,12,13,14,15,16,17,18,19,20,22,24	nCK			
Supported nRCD Timings minimum	12	nCK			
Supported nRP Timings minimum	12	nCK			
Supported CWL Settings	9,10,11,12,14,16,18	nCK			



## Speed Bin Table Note

### Absolute Specification

VDDQ = VDD = 1.20V +/- 0.06 V

VPP = 2.5V +0.25/-0.125 V

The values defined with above-mentioned table are DLL ON case.

DDR4-1600, 1866, 2133 and 2400 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog -data and strobe output are synchronized by the DLL -all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (1.5, 1.25, 1.071, 0.938 or 0.833 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next 'Supported CL', where tAA = 12.5ns and tCK(avg) = 1.3 ns should only be used for CL = 10 calculation.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.938 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
9. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
10. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.

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## Timing Parameters by Speed Grade

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
<b>Clock Timing</b>									
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	8	-	8	-	ns	23
Average Clock Period	tCK(avg)	See Speed Bins Table						ps	
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Absolute clock Low pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	25
Clock Period Jitter- total	JIT(per)_tot	-0.1	0.1	-0.1	0.1	-0.1	0.1	UI	26
Clock Period Jitter- deterministic	JIT(per)_dj	tbd						UI	27
Clock Period Jitter during DLL locking period	tJIT(per, lck)	tbd						UI	
Cycle to Cycle Period Jitter	tJIT(cc)_tot	0.2		0.2		0.2		UI	26
Cycle to Cycle Period Jitter- deterministic	tJIT(cc)_dj	tbd						UI	27
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	tbd						UI	
Duty cycle Jitter	tJIT(duty)	tbd						UI	
Cumulative error across 2 cycles	tERR(2per)	tbd						UI	
Cumulative error across 3 cycles	tERR(3per)	tbd						UI	
Cumulative error across 4 cycles	tERR(4per)	tbd						UI	
Cumulative error across 5 cycles	tERR(5per)	tbd						UI	
Cumulative error across 6 cycles	tERR(6per)	tbd						UI	
Cumulative error across 7 cycles	tERR(7per)	tbd						UI	
Cumulative error across 8 cycles	tERR(8per)	tbd						UI	
Cumulative error across 9 cycles	tERR(9per)	tbd						UI	
Cumulative error across 10 cycles	tERR(10per)	tbd						UI	
Cumulative error across 11 cycles	tERR(11per)	tbd						UI	
Cumulative error across 12 cycles	tERR(12per)	tbd						UI	
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tbd						UI	
<b>Command and Address Timing</b>									
CAS_n to CAS_n command delay for same bank group	tCCD_L	5	-	5	-	6	-	nCK	
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	tRRD_S(1K)	Max(4nCK,5ns)	-	Max(4nCK,4.2ns)	-	Max(4nCK,3.7ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK,5ns)	-	Max(4nCK,4.2ns)	-	Max(4nCK,3.7ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,7.5ns)	-	Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Four activate window for 2KB page size	tFAW_2K	35	-	30	-	30	-	ns	
Four activate window for 1KB page size	tFAW_1K	25	-	23	-	21	-	ns	
Four activate window for 1KB page size	tFAW_1/2K	20	-	17	-	15	-	ns	
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-		1,2,e
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-		1
Internal READ Command to PRECHARGE Command delay	tRTP	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		
WRITE recovery time	tWR	15	-	15	-	15	-	ns	1
WRITE recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max(4nCK,3.75ns)	-	tWR+max(5nCK,3.75ns)	-	tWR+max(5nCK,3.75ns)	-	ns	1,29
Delay from start of internal write transaction to internal read command for different bank groups with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+max(4nCK,3.75ns)	-	tWTR_S+max(5nCK,3.75ns)	-	tWTR_S+max(5nCK,3.75ns)	-	ns	2,30
Delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+max(4nCK,3.75ns)	-	tWTR_L+max(5nCK,3.75ns)	-	tWTR_L+max(5nCK,3.75ns)	-	ns	3,31
DLL locking time	tDLLK	TBD	-		-		-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-		
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK	
Multi-Purpose Register Write Recovery Time	tWR_MPR	MIN = tMOD + AL + PL	-	MIN = tMOD + AL + PL	-	MIN = tMOD + AL + PL	-		
<b>CS_n to Command Address Latency</b>									
CS_n to Command Address Latency	tCAL	3	-	4	-	4	-	nCK	
<b>DRAM Data Timing</b>									
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	tbd	-	tbd	-	tbd	tCK(avg)/2	14,1,9
DQS_t,DQS_c to DQ skew deterministic, per group, per access	tDQSQ	-	tbd	-	tbd	-	tbd	tCK(avg)/2	15,1,7,19
DQ output hold time from DQS_t,DQS_c	tQH	tbd	-	-	-	-	-	tCK(avg)/2	14,1,8,19
DQ output hold time deterministic from DQS_t, DQS_c	tQH	tbd	-	-	-	-	-	UI	15,1,7,19
DQS_t,DQS_c to DQ Skew total, per group, per access; DBI enabled	tDQSQ	-	tbd	-	tbd	-	tbd	UI	14,20
DQ output hold time total from DQS_t, DQS_c; DBI enabled	tQH	TBD	-	TBD	-	TBD	-	UI	14,20
DQ to DQ offset , per group, per access referenced to DQS_t, DQS_c	tDQSQ	TBD	TBD	TBD	TBD	TBD	TBD	UI	16,17
<b>Data Strobe Timing</b>									
DQS_t,DQS_c differential output high time	tQSH	TBD	TBD	TBD	TBD	TBD	TBD	tCK(avg)/2	22
DQS_t,DQS_c differential output low time	tQSL	TBD	TBD	TBD	TBD	TBD	TBD	tCK(avg)/2	21
<b>MPSM Timing</b>									
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	TBD	-	TBD	-	TBD	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-		
CS setup time to CKE	tMPX_S	TBD	-	TBD	-	TBD	-		
CS hold time to CKE	tMPX_H	TBD	-	TBD	-	TBD	-		
<b>Calibration Timing</b>									

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing									
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min) + 10ns)	-	max (5nCK,tRFC(min) + 10ns)	-	max (5nCK,tRFC(min) + 10ns)	-		
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-		
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-		
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-		
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max (5nCK,10ns)+PL	-	max (5nCK,10ns)+PL	-	max (5nCK,10ns)+PL	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-		
Power Down Timing									
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen t commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-		
Exit Precharge Power Down with DLL frozen t commands requiring a locked DLL	tXPDLL	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-		3
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-		32,33
Command pass disable delay	tCPDED	4	-	4	-	4	-		
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI		6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-		7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-		7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRPBC4DEN	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	nCK	7,8
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
PDA Timing									
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)	-	max(16nCK,10ns)	-	max(16nCK,10ns)	-		
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD			
ODT Timing									
Asynchronous RTT turn-on delay (Power-Down with	tAONAS	1	9	1	9	1	9	ns	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
DLL frozen)									
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1	9	1	9	1	9	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	
Write Leveling Timing									
First DQS <sub>t</sub> /DQS <sub>n</sub> rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	nCK	13
DQS <sub>t</sub> /DQS <sub>n</sub> delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	nCK	13
Write leveling setup time from rising CK <sub>t</sub> , CK <sub>c</sub> crossing to rising DQS <sub>t</sub> /DQS <sub>n</sub> crossing	tWLS	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS <sub>t</sub> /DQS <sub>n</sub> crossing to rising CK <sub>t</sub> , CK <sub>c</sub> crossing	tWLH	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE							ns	
CA Parity Timing									
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	4	-	4	-	4		
Delay from errant command to ALERT <sub>n</sub> assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns		
Pulse width of ALERT <sub>n</sub> signal when asserted	tPAR_ALERT_PW	48	96	56	112	64	128	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RS <sub>P</sub>	-	43	-	50	-	57	nCK	
Parity Latency [ 1715.64, JC42.3C]	PL	4		4		4		nCK	
CRC Error Reporting									
CRC error to ALERT <sub>n</sub> latency	tCRC_ALERT	3	13	3	13	3	13	ns	
CRC ALERT <sub>n</sub> pulse width	CRC_ALERT_PW	6	10	6	10	6	10	nCK	
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max (4nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	ns	10
delay from start of internal write transaction to internal delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_C RC_DM	tWTR_S+max (4nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	ns	11
delay from start of internal write transaction to internal delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_C RC_DM	tWTR_L+max (4nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	ns	12
Geardown timing									
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	tXPR_GEAR	TBD		TBD		TBD			
CKE HIGH Assert Geardown Enable time(T2/CKE)	tXS_GEAR	TBD		TBD		TBD			
MRS command to Sync pulse time(T3)	tSYNC_GEAR	TBD	TBD	TBD	TBD	TBD	TBD		
Sync pulse to First valid command(T4)	tCMD_GEAR	TBD		TBD		TBD			
Geardown setup time	tGEAR_setup	TBD	TBD	TBD	TBD	TBD	TBD		
Geardown hold time	tGEAR_hold	TBD	TBD	TBD	TBD	TBD	TBD		
tREFI									
tRFC1 (min)	2Gb	160	-	160	-	160	-	ns	
	4Gb	260	-	260	-	260	-	ns	
	8Gb	350	-	350	-	350	-	ns	
	16Gb	TBD by JEDEC board spec)	-	TBD	-	TBD	-	ns	
tRFC2 (min)	2Gb	110	-	110	-	110	-	ns	
	4Gb	160	-	160	-	160	-	ns	
	8Gb	260	-	260	-	260	-	ns	
	16Gb	TBD by JEDEC board spec)	-	TBD	-	TBD	-	ns	
tRFC4 (min)	2Gb	90	-	90	-	90	-	ns	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
	4Gb	110	-	110	-	110	-	ns	
	8Gb	160	-	160	-	160	-	ns	
	16Gb	TBD by JEDEC board spec)	-	TBD	-	TBD	-	ns	

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## Timing Parameters by Speed Grade, continued

Speed		DDR4-2400		DDR4-2667		DDR4-3200		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
<b>Clock Timing</b>									
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	8	-	8	-	ns	23
Average Clock Period	tCK(avg)	See Speed Bins Table						ps	
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Absolute clock Low pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	25
Clock Period Jitter- total	JIT(per)_tot	-42	42	-0.1	0.1	-0.1	0.1	UI	26
Clock Period Jitter- deterministic	JIT(per)_dj	tbd						UI	27
Clock Period Jitter during DLL locking period	tJIT(per, lck)	tbd						UI	
Cycle to Cycle Period Jitter	tJIT(cc)_tot	83		0.2		0.2		UI	26
Cycle to Cycle Period Jitter- deterministic	tJIT(cc)_dj	tbd						UI	27
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	tbd						UI	
Duty cycle Jitter	tJIT(duty)	tbd						UI	
Cumulative error across 2 cycles	tERR(2per)	tbd						UI	
Cumulative error across 3 cycles	tERR(3per)	tbd						UI	
Cumulative error across 4 cycles	tERR(4per)	tbd						UI	
Cumulative error across 5 cycles	tERR(5per)	tbd						UI	
Cumulative error across 6 cycles	tERR(6per)	tbd						UI	
Cumulative error across 7 cycles	tERR(7per)	tbd						UI	
Cumulative error across 8 cycles	tERR(8per)	tbd						UI	
Cumulative error across 9 cycles	tERR(9per)	tbd						UI	
Cumulative error across 10 cycles	tERR(10per)	tbd						UI	
Cumulative error across 11 cycles	tERR(11per)	tbd						UI	
Cumulative error across 12 cycles	tERR(12per)	tbd						UI	
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tbd						UI	
<b>Command and Address Timing</b>									
CAS_n to CAS_n command delay for same bank group	tCCD_L	6	-	tbd	-	-	-	nCK	
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	-	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK, 5.3ns)	-	-	-	-	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	tRRD_S(1K)	Max(4nCK, 3.3ns)	-	-	-	-	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK, 3.3ns)	-	-	-	-	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK, 6.4ns)	-	-	-	-	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK, 4.9ns)	-	-	-	-	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK, 4.9ns)	-	-	-	-	-	nCK	
Four activate window for 2KB page size	tFAW_2K	30						ns	

Speed		DDR4-2400		DDR4-2667		DDR4-3200		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Four activate window for 1KB page size	tFAW_1K	21						ns	
Four activate window for 1KB page size	tFAW_1/2K	13						ns	
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK,2.5ns)	-		-		-		1,2,e
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK,7.5ns)	-		-		-		1
Internal READ Command to PRECHARGE Command delay	tRTP	max (4nCK,7.5ns)	-		-		-		
WRITE recovery time	tWR	15	-		-		-	ns	1
WRITE recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max(5nCK,3.75ns)	-		-		-	ns	1,29
Delay from start of internal write transaction to internal read command for different bank groups with both CRC and OM enabled	tWTR_S_CRC_DM	tWTR_S+max(5nCK,3.75ns)	-		-		-	ns	2,30
Delay from start of internal write transaction to internal read command for same bank group with both CRC and OM enabled	tWTR_L_CRC_DM	tWTR_L+max(5nCK,3.75ns)	-		-		-	ns	3,31
DLL locking time	tDLLK	TBD						nCK	
Mode Register Set command cycle time	tMRD	8	-		-		-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-		-		-		
Multi-Purpose Register Recovery Time	tMPRR	1	-		-		-	nCK	
Multi-Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-		-		-		
<b>CS_n to Command Address Latency</b>									
CS_n to Command Address Latency	tCAL	5	-		-		-	nCK	
<b>DRAM Data Timing</b>									
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	tbd	-	tbd	-	tbd	tCK(avg)/2	14,1,9
DQS_t,DQS_c to DQ skew deterministic, per group, per access	tDQSQ	-	tbd	-	tbd	-	tbd	tCK(avg)/2	15,1,7,19
DQ output hold time from DQS_t,DQS_c	tQH	tbd	-		-		-	tCK(avg)/2	14,1,8,19
DQ output hold time deterministic from DQS_t, DQS_c	tQH	tbd	-		-		-	UI	15,1,7,19
DQS_t,DQS_c to DQ Skew total, per group, per access; DBI enabled	tDQSQ	-	tbd	-	tbd	-	tbd	UI	14,20
DQ output hold time total from DQS_t, DQS_c; DBI enabled	tQH	TBD	-	TBD	-	TBD	-	UI	14,20
DQ to DQ offset , per group, per access refer-enced to DQS_t, DQS_c	tDQSQ	TBD	TBD	TBD	TBD	TBD	TBD	UI	16, 17
<b>Data Strobe Timing</b>									
DQS_t,DQS_c differential output high time	tQSH	TBD	TBD	TBD	TBD	TBD	TBD	tCK(avg)/2	22
DQS_t,DQS_c differential output low time	tQSL	TBD	TBD	TBD	TBD	TBD	TBD	tCK(avg)/2	21
<b>MPSM Timing</b>									
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-				-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-				-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-				-		
Exit MPSM to commands not requiring a locked DLL	tXMP	TBD	-				-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-				-		
CS setup time to CKE	tMPX_S	TBD	-				-		
CS hold time to CKE	tMPX_H	TBD	-				-		
<b>Calibration Timing</b>									
Power-up and RESET calibration time	tZQinit	1024	-				-	nCK	
Normal operation Full calibration time	tZQoper	512	-				-	nCK	



Speed		DDR4-2400		DDR4-2667		DDR4-3200		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Normal operation Short calibration time	tZQCS	128	-				-	nCK	
<b>Reset/Self Refresh Timing</b>									
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK,tRFC(min)+10ns)	-				-		
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-				-		
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT(min)	tRFC4(min)+10ns	-				-		
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+10ns	-				-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLL(min)	-				-		
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-				-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10ns)	-				-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max(5nCK,10ns)+PL	-				-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10ns)	-				-		
<b>Power Down Timing</b>									
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen t commands not requiring a locked DLL	tXP	max(4nCK,6ns)	-				-		
Exit Precharge Power Down with DLL frozen t commands requiring a locked DLL	tXPDLL	max(10nCK,24ns)	-				-		3
CKE minimum pulse width	tCKE	max(3nCK,5ns)	-				-		32,33
Command pass disable delay	tCPDED	4	-				-		
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI				9*tREFI		6
Timing of ACT command to Power Down entry	tACTPDEN	2	-				-		7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-				-		7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-				-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/ tCK(avg))	-				-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-				-	nCK	5
Timing of WR command to Power Downentry (BC4MRS)	tWRPBC4DEN	WL+2+(tWR/ tCK(avg))	-				-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4DEN	WL+2+WR+1	-				-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	2	-				-	nCK	7,8
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-				-		
<b>PDA Timing</b>									
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)	-	max(16nCK,10ns)	-	max(16nCK,10ns)	-		
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD			
<b>ODT Timing</b>									
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1	9					ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1	9					ns	
RTT dynamic change skew	tADC	0.3	0.7					tCK(avg)	
<b>Write Leveling Timing</b>									
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-					nCK	13
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-					nCK	13

Speed		DDR4-2400		DDR4-2667		DDR4-3200		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-					tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_c crossing	tWLH	0.13	-					tCK(avg)	
Write leveling output delay	tWLO	0	9.5					ns	
Write leveling output error	tWLOE							ns	
<b>CA Parity Timing</b>									
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	Max(2nCK,3ns)						
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns						
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	72	144					nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RS_P	-	64					nCK	
Parity Latency [ 1715.64, JC42.3C]	PL	5						nCK	
<b>CRC Error Reporting</b>									
CRC error to ALERT_n latency	tCRC_ALERT	-	13					ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10					nCK	
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max (5nCK,3.75ns)						ns	10
delay from start of internal write transaction to internal delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_C_RC_DM	tWTR_S+max (5nCK,3.75ns)						ns	11
delay from start of internal write transaction to internal delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_C_RC_DM	tWTR_L+max (5nCK,3.75ns)						ns	12
<b>Geardown timing</b>									
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	tXPR_GEAR	tXPR		tXPR					
CKE HIGH Assert Geardown Enable time(T2/CKE)	tXS_GEAR	tXS		tXS					
MRS command to Sync pulse time(T3)	tSYNC_GEAR	tMOD(min)+4nCK		tMOD(min)+4nCK					28
Sync pulse to First valid command(T4)	tCMD_GEAR			tMOD		tMOD			28
Geardown setup time	tGEAR_setup			2	-	2	-	nCK	
Geardown hold time	tGEAR_hold			2	-	2	-	nCK	
<b>tREFI</b>									
tRFC1 (min)	2Gb	160	-	160	-	160	-	ns	
	4Gb	260	-	260	-	260	-	ns	
	8Gb	350	-	350	-	350	-	ns	
	16Gb	TBD by JEDEC board spec)	-	TBD	-	TBD	-	ns	
tRFC2 (min)	2Gb	110	-	110	-	110	-	ns	
	4Gb	160	-	160	-	160	-	ns	
	8Gb	260	-	260	-	260	-	ns	
	16Gb	TBD by JEDEC board spec)	-	TBD	-	TBD	-	ns	
tRFC4 (min)	2Gb	90	-	90	-	90	-	ns	
	4Gb	110	-	110	-	110	-	ns	
	8Gb	160	-	160	-	160	-	ns	
	16Gb	TBD by JEDEC board spec)	-	TBD	-	TBD	-	ns	

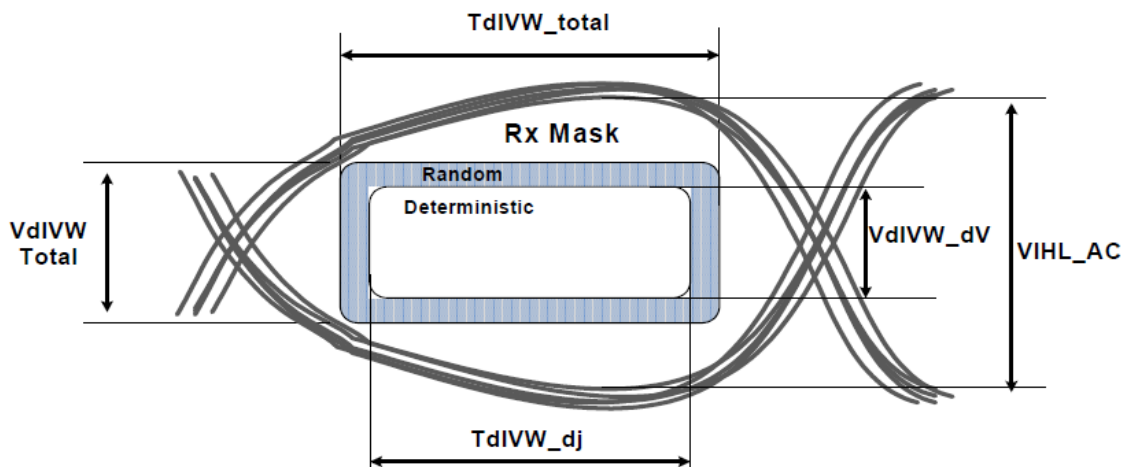
**Notes:**

- Start of internal write transaction is defined as follows:  
 For BL8 (Fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL.  
 For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.  
 For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
- A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
- Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
- tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
- WR in clock cycles as programmed in MR0.
- tREFI depends on TOPER.
- CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
- Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See 0.1.3 "Power-Down clarifications - Case 2" in RB11112 .

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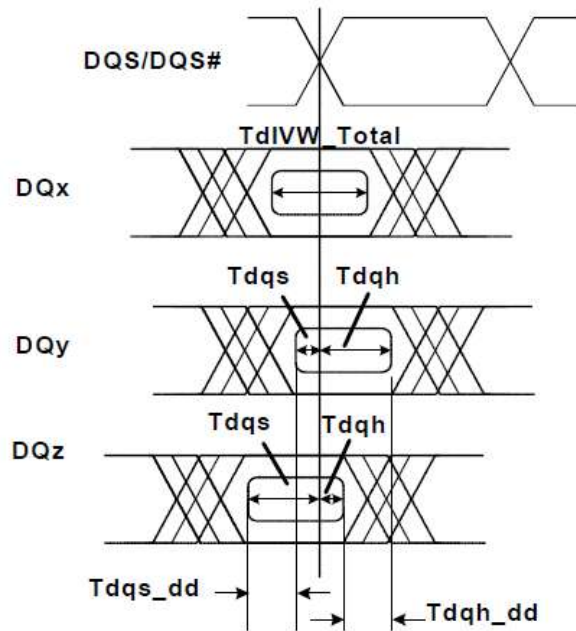
- DQ Receiver(Rx) compliance mask
- 9. For these parameters, the DDR4 SDRAM device supports  $t_{nPARAM}[nCK]=RU(t_{PARAM}[ns])/t_{CK}(avg)[ns]$ , which is in clock cycles assuming all input clock jitter specifications are satisfied
- 10. When CRC and DM are both enabled,  $t_{WR\_CRC\_DM}$  is used in place of  $t_{WR}$ .
- 11. When CRC and DM are both enabled  $t_{WTR\_S\_CRC\_DM}$  is used in place of  $t_{WTR\_S}$ .
- 12. When CRC and DM are both enabled  $t_{WTR\_L\_CRC\_DM}$  is used in place of  $t_{WTR\_L}$ .
- 13. The max values are system dependent.
- 14. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.
- 15. The deterministic component of the total timing. Measurement method tbd.
- 16. DQ to DQ static offset relative to strobe per group. Measurement method tbd.
- 17. This parameter will be characterized and guaranteed by design.
- 18. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual  $t_{jit}(per)_{total}$  of the input clock. (output Deratings are relative to the SDRAM input clock). Example tbd.
- 19. DRAM DBI mode is off.
- 20. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
- 21.  $t_{QSL}$  describes the instantaneous differential output low pulse width on  $DQS\_t - DQS\_c$ , as measured from on falling edge to the next consecutive rising edge
- 22.  $t_{QSH}$  describes the instantaneous differential output high pulse width on  $DQS\_t - DQS\_c$ , as measured from on falling edge to the next consecutive rising edge
- 23. There is no maximum cycle time limit besides the need to satisfy the refresh interval  $t_{REFI}$
- 24.  $t_{CH}(abs)$  is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
- 25.  $t_{CL}(abs)$  is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
- 26. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.
- 27. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
- 28. This parameter has to be even number of clocks
- 29. When CRC and DM are both enabled,  $t_{WR\_CRC\_DM}$  is used in place of  $t_{WR}$ .
- 30. When CRC and DM are both enabled  $t_{WTR\_S\_CRC\_DM}$  is used in place of  $t_{WTR\_S}$ .
- 31. When CRC and DM are both enabled  $t_{WTR\_L\_CRC\_DM}$  is used in place of  $t_{WTR\_L}$ .
- 32. After CKE is registered LOW, CKE signal level shall be maintained below  $V_{ILDC}$  for  $t_{CKE}$  specification ( Low pulse width).
- 33. After CKE is registered HIGH, CKE signal level shall be maintained above  $V_{IHDC}$  for  $t_{CKE}$  specification ( HIGH pulse width).  
 $UI=t_{CK}(avg).min/2$

## DQ input receiver compliance mask for voltage and timing

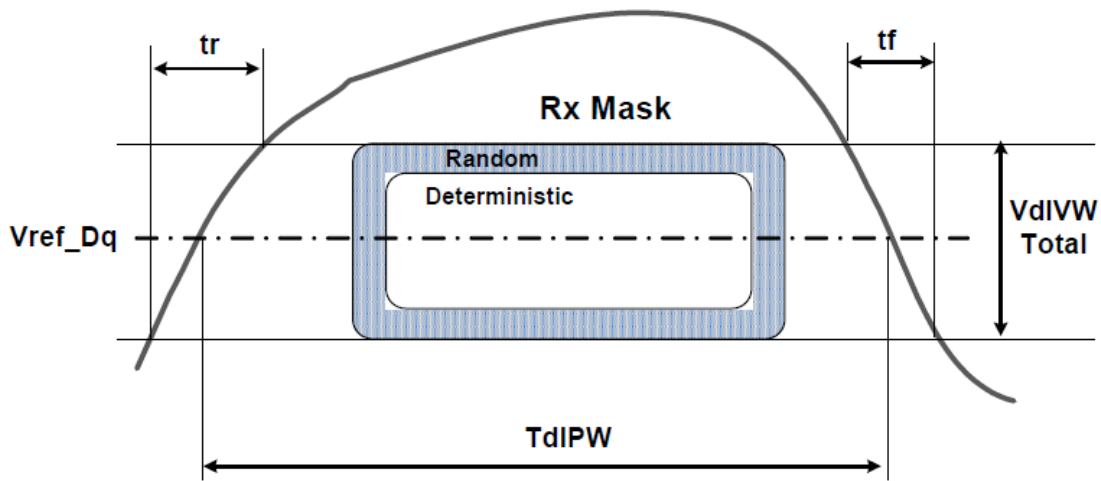


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DQ to DQS timing definitions Tdqs, Tdqh, TdIVW\_total, Tdqs\_dd, Tdqh\_dd



DQ TdIPW and SRIN\_divVW definition (for each input pulse)



Note:  $SRIN\_divVW = V_{diVW\_Total} / (t_r \text{ or } t_f)$

Voltage and Timing Parameters for DQ input receiver compliance mask

Symbol	Parameter	DDR4-1600 DDR4-1867 DDR4-2133	DDR4-2400 DDR4-2667	DDR4-3200	Unit	Notes
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		Min	Max	Min	Max	Min	Max		
VdIVW_total	Vin Rx Mask input p-p total	-	tbd	-	tbd	-	tbd	mV	1,2,3,5,7
VdIVW_dV	Vin Rx input swing deterministic voltage	-	tbd	-	tbd	-	tbd	mV	1,2,6
TdIVW_total	Total DQ Rx input timing window	-	tbd	-	tbd	-	tbd	UI	1,2,4,5,7
TdIVW_dj	DQ Rx deterministic jitter	-	tbd	-	tbd	-	tbd	UI	1,2,6
VIHL_AC	DQ AC input swing pk-pk	-	tbd	-	tbd	-	tbd	mV	1,8
TdIPW	DQ input pulse width	-	tbd	-	tbd	-	tbd	UI	1,9
Tdqs	DQ to DQS Setup offset	-	tbd	-	tbd	-	tbd	UI	1,10
Tdqh	DQ to DQS Hold offset	-	tbd	-	tbd	-	tbd	UI	1,10
Tdqs_dd	DQ to DQ Setup offset	-	tbd	-	tbd	-	tbd	UI	1,11
Tdqh_dd	DQ to DQ Hold offset	-	tbd	-	tbd	-	tbd	UI	1,11
SRIN_dIVW	Input Slew Rate over VdIVW	-	tbd	-	tbd	-	tbd	V/ns	1,12

**Notes:**

1. For DQ in receive mode.
2. Data Rx mask voltage and timing total input valid window. Data Rx mask applied per bit post training and should include voltage and temperature drift terms. Design Target BER < tbd. Measurement method tbd.
3. Rx voltage input AC swing peak-peak requirement over the total TdIVW\_total.
4. Rx differential DQ to DQS jitter total timing window at the VdIVW voltage levels centered at Vref.
5. Defined over the DQ internal Vref range 1.
6. Deterministic component of the total Rx mask voltage or timing. Parameter will be characterized and guaranteed by design. Measurement method tbd
7. Overshoot and Undershoot Specifications tbd.
8. DQ signal swing into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level.
9. DQ minimum input pulse width defined at the Vref level.
10. DQ to DQS setup or hold offset defined within byte. Tdqs and Tdqh are the minimum hold and setup per DQ pin for a given component.
11. DQ to DQ setup or hold delta offset defined within byte as the static difference in Tdqs(max) & Tdqs(min) or Tdqh(max)-Tdqh(min) per device.
12. Input slew rate over VdIVW Mask centered at Vref

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