Si8660/61/62/63 Data Sheet

Low Power Six-Channel Digital Isolator

Silicon Lab's family of ultra-low-power digital isolators are CMOS devices offering substantial data rate, propagation delay, power, size, reliability, and external BOM advantages over legacy isolation technologies. The operating parameters of these products remain stable across wide temperature ranges and throughout device service life for ease of design and highly uniform performance. All device versions have Schmitt trigger inputs for high noise immunity and only require VDD bypass capacitors.

Data rates up to 150 Mbps are supported, and all devices achieve propagation delays of less than 10 ns. Ordering options include a choice of isolation ratings (1.0, 2.5, 3.75 and 5 kV) and a selectable fail-safe operating mode to control the default output state during power loss. All products >1 kV_{RMS} are safety certified by UL, CSA, VDE, and CQC, and products in wide-body packages support reinforced insulation withstanding up to 5 kV_{RMS}.

Applications

- Industrial automation systems
- Medical electronics
- Hybrid electric vehicles
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power inverters
- Communication systems

Safety Regulatory Approvals

- UL 1577 recognized
  - Up to 5000 V_{RMS} for 1 minute
- CSA component notice 5A approval
  - IEC 60950-1, 62368-1, 60601-1 (reinforced insulation)
- VDE certification conformity
  - VDE 0884-10
  - EN60950-1 (reinforced insulation)
- CQC certification approval
  - GB4943.1

KEY FEATURES

- High-speed operation
  - DC to 150 Mbps
- No start-up initialization required
- Wide Operating Supply Voltage
  - 2.5–5.5 V
- Up to 5000 V_{RMS} isolation
- 60-year life at rated working voltage
- High electromagnetic immunity
- Ultra low power (typical)
  - 5 V Operation
    - 1.6 mA per channel at 1 Mbps
    - 5.5 mA per channel at 100 Mbps
  - 2.5 V Operation
    - 1.5 mA per channel at 1 Mbps
    - 3.5 mA per channel at 100 Mbps
- Schmitt trigger inputs
- Selectable fail-safe mode
  - Default high or low output (ordering option)
- Precise timing (typical)
  - 10 ns propagation delay
  - 1.5 ns pulse width distortion
  - 0.5 ns channel-channel skew
  - 2 ns propagation delay skew
  - 5 ns minimum pulse width
- Transient Immunity 50 kV/µs
- AEC-Q100 qualification
- Wide temperature range
  - –40 to 125 °C
- RoHS-compliant packages
  - SOIC-16 wide body
  - SOIC-16 narrow body
  - QSOP-16

1. Ordering Guide

Table 1.1. Ordering Guide for Valid OPNs [1,2,3]

Ordering Part Number (OPN)	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Max Data Rate (Mbps)	Default Output State	Isolation Rating (kV)	Temp (°C)	Package
QSOP-16 Packages							
Si8660BB-B-IU	6	0	150	Low	2.5	–40 to 125 °C	QSOP-16
Si8660EB-B-IU	6	0	150	High	2.5	–40 to 125 °C	QSOP-16
Si8661BB-B-IU	5	1	150	Low	2.5	–40 to 125 °C	QSOP-16
Si8661EB-B-IU	5	1	150	High	2.5	–40 to 125 °C	QSOP-16
Si8662BB-B-IU	4	2	150	Low	2.5	–40 to 125 °C	QSOP-16
Si8662EB-B-IU	4	2	150	High	2.5	–40 to 125 °C	QSOP-16
Si8663BB-B-IU	3	3	150	Low	2.5	–40 to 125 °C	QSOP-16
Si8663EB-B-IU	3	3	150	High	2.5	–40 to 125 °C	QSOP-16
SOIC-16 Packages							
Si8660BA-B-IS1	6	0	150	Low	1.0	–40 to 125 °C	NB SOIC-16
Si8660BB-B-IS1	6	0	150	Low	2.5	–40 to 125 °C	NB SOIC-16
Si8660BC-B-IS1	6	0	150	Low	3.75	–40 to 125 °C	NB SOIC-16
Si8660EC-B-IS1	6	0	150	High	3.75	–40 to 125 °C	NB SOIC-16
Si8660BD-B-IS	6	0	150	Low	5.0	–40 to 125 °C	WB SOIC-16
Si8660ED-B-IS	6	0	150	High	5.0	–40 to 125 °C	WB SOIC-16
Si8661BB-B-IS1	5	1	150	Low	2.5	–40 to 125 °C	NB SOIC-16
Si8661BC-B-IS1	5	1	150	Low	3.75	–40 to 125 °C	NB SOIC-16
Si8661EC-B-IS1	5	1	150	High	3.75	–40 to 125 °C	NB SOIC-16
Si8661BD-B-IS	5	1	150	Low	5.0	–40 to 125 °C	WB SOIC-16
Si8661ED-B-IS	5	1	150	High	5.0	–40 to 125 °C	WB SOIC-16
Si8661BD-B-IS2	5	1	150	Low	5.0	–40 to 125 °C	WB SOIC-16 (8 mm creepage)[4]
Si8662BB-B-IS1	4	2	150	Low	2.5	–40 to 125 °C	NB SOIC-16
Si8662BC-B-IS1	4	2	150	Low	3.75	–40 to 125 °C	NB SOIC-16
Si8662EC-B-IS1	4	2	150	High	3.75	–40 to 125 °C	NB SOIC-16
Si8662BD-B-IS	4	2	150	Low	5.0	–40 to 125 °C	WB SOIC-16
Si8662ED-B-IS	4	2	150	High	5.0	–40 to 125 °C	WB SOIC-16
Si8663BB-B-IS1	3	3	150	Low	2.5	–40 to 125 °C	NB SOIC-16
Si8663BC-B-IS1	3	3	150	Low	3.75	–40 to 125 °C	NB SOIC-16
Si8663EC-B-IS1	3	3	150	High	3.75	–40 to 125 °C	NB SOIC-16
Si8663BD-B-IS	3	3	150	Low	5.0	–40 to 125 °C	WB SOIC-16

Ordering Part Number (OPN)	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Max Data Rate (Mbps)	Default Output State	Isolation Rating (kV)	Temp (°C)	Package
Si8663ED-B-IS	3	3	150	High	5.0	–40 to 125 °C	WB SOIC-16

Notes:

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. “Si” and “SI” are used interchangeably.
3. An "R" at the end of the part number denotes tape and reel packaging option.
4. The package designated IS2 has a design that eliminates tie bars, thus allowing for extra creepage distance while maintaining standard WB SOIC-16 package dimensions and land pattern.

Table of Contents

2. Functional Description

2.1 Theory of Operation

The operation of an Si866x channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si866x channel is shown in the figure below.

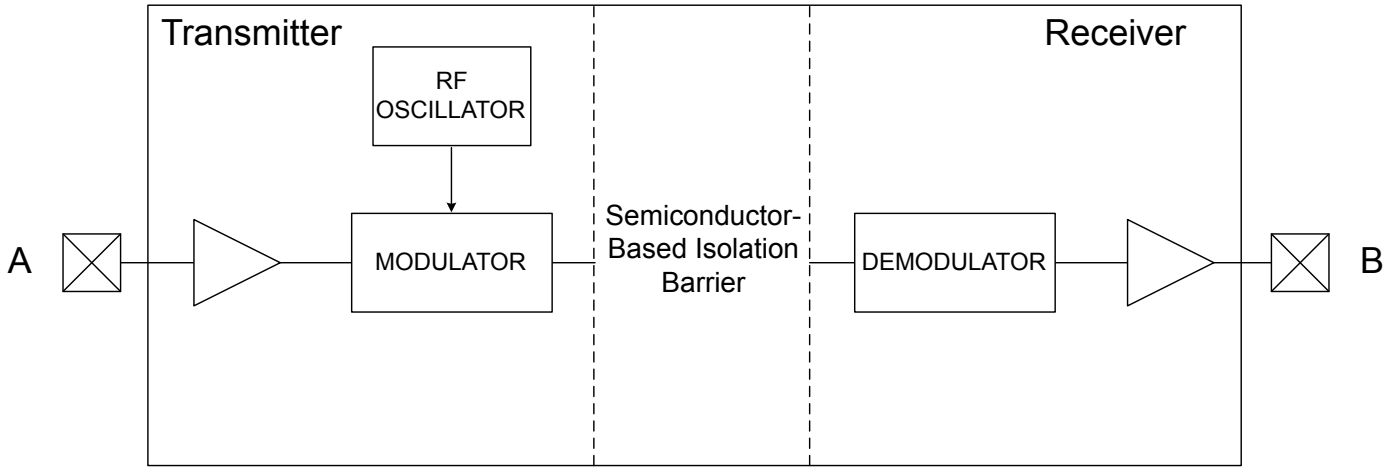


Figure 2.1. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See the figure below for more details.

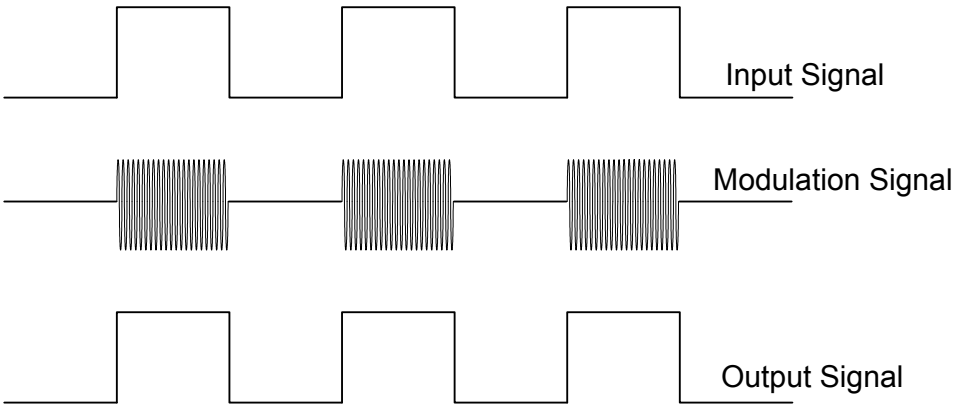


Figure 2.2. Modulation Scheme

2.2 Eye Diagram

The figure below illustrates an eye-diagram taken on an Si8660. For the data source, the test used an Anritsu (MP1763C) Pulse Pattern Generator set to 1000 ns/div. The output of the generator's clock and data from an Si8660 were captured on an oscilloscope. The results illustrate that data integrity was maintained even at the high data rate of 150 Mbps. The results also show that 2 ns pulse width distortion and 350 ps peak jitter were exhibited.

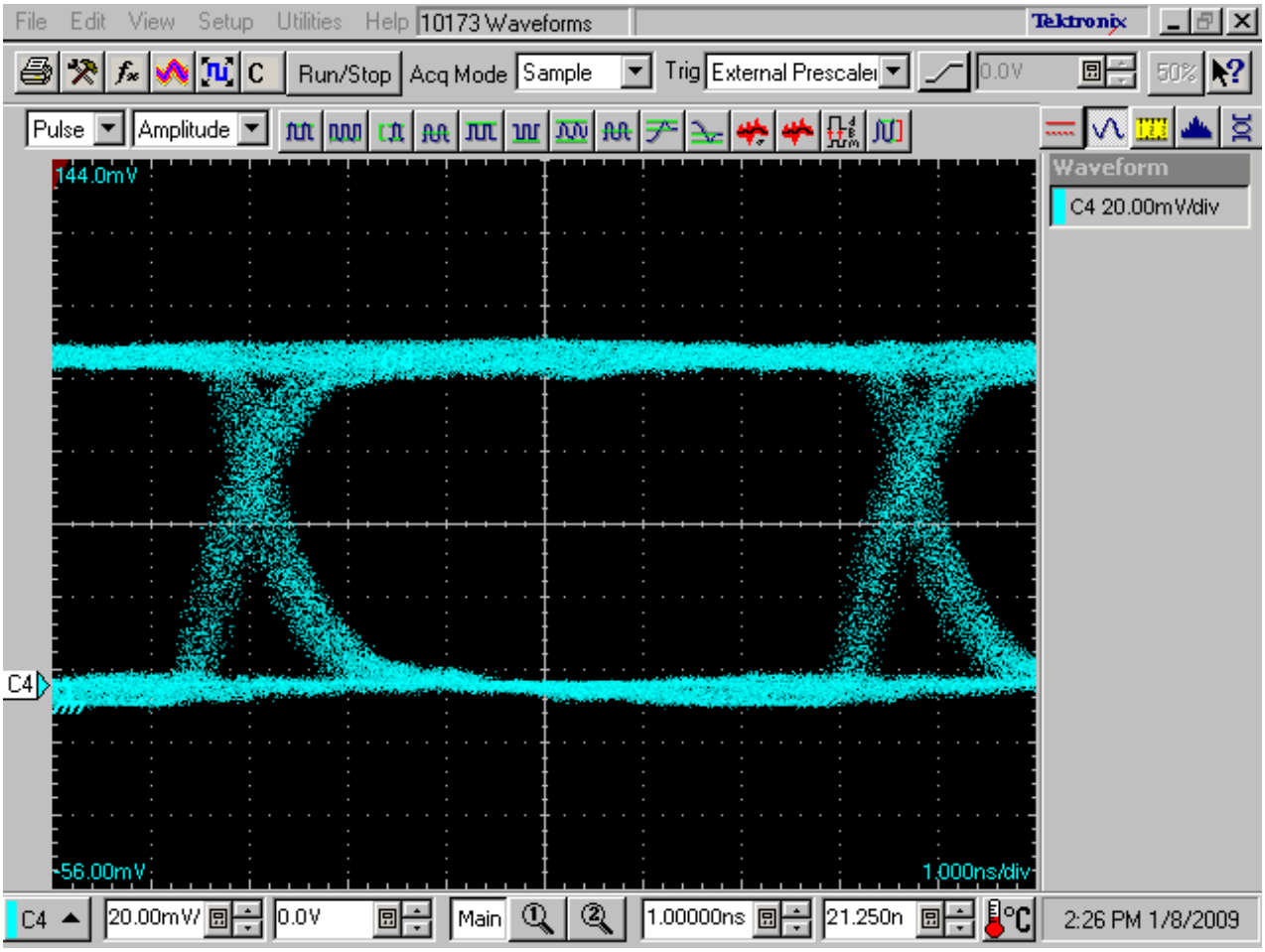


Figure 2.3. Eye Diagram

3. Device Operation

Device behavior during start-up, normal operation, and shutdown is shown in Figure 3.1 Device Behavior during Normal Operation on page 8, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Refer to the table below to determine outputs when power supply (VDD) is not present.

Table 3.1. Si866x Logic Operation

V_I Input [1,2]	VDDI State[1,3,4]	VDDO State[1,3,4]	V_O Output[1,2]	Comments
H	P	P	H	Normal operation.
L	P	P	L	
X [5]	UP	P	L[6] H[6]	Upon transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 µs.
X[5]	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V_O returns to the same state as V_I within 1 µs.

Notes:

1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance.
3. "Powered" state (P) is defined as 2.5 V < VDD < 5.5 V.
4. "Unpowered" state (UP) is defined as VDD = 0 V.
5. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
6. See 1. Ordering Guide for details. This is the selectable fail-safe operating mode (ordering option). Some devices have default output state = H, and some have default output state = L, depending on the ordering part number (OPN). For default high devices, the data channels have pull-ups on inputs/outputs. For default low devices, the data channels have pull-downs on inputs/outputs.

3.1 Device Startup

Outputs are held low during powerup until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs.

3.2 Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. Both Side A and Side B each have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, Side A unconditionally enters UVLO when V_{DD1} falls below $V_{DD1(UVLO–)}$ and exits UVLO when V_{DD1} rises above $V_{DD1(UVLO+)}$. Side B operates the same as Side A with respect to its V_{DD2} supply.

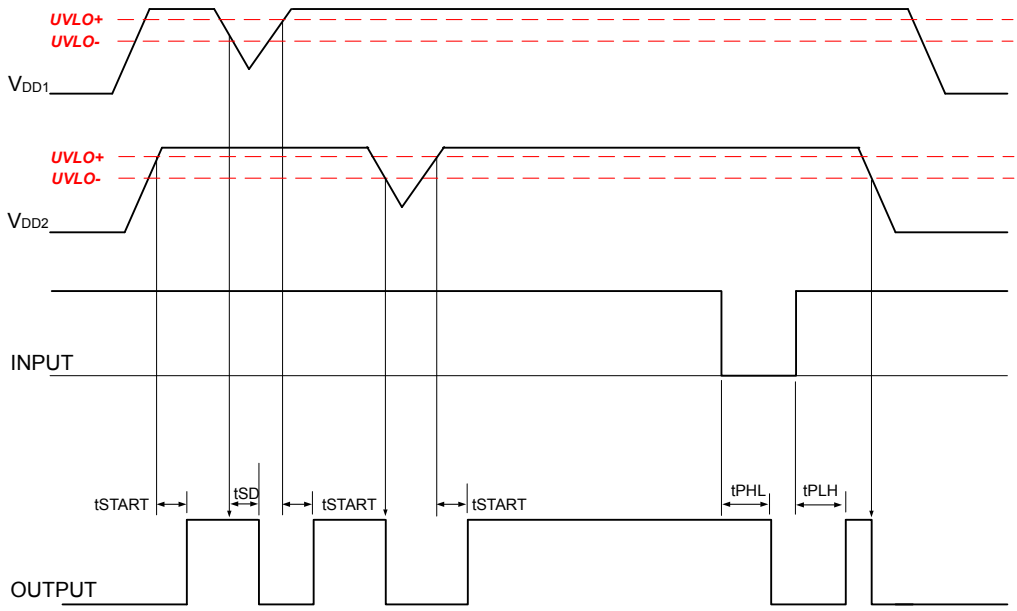


Figure 3.1. Device Behavior during Normal Operation

3.3 Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with >30 V_{AC}) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with <30 V_{AC}) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 4.5 Regulatory Information [1] on page 22 and 4. Electrical Specifications detail the working voltage and creepage/clearance capabilities of the Si86xx. These tables also detail the component standards (UL1577, IEC60747, CSA 5A), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 60950-1, 60601-1, etc.) requirements before starting any design that uses a digital isolator.

3.3.1 Supply Bypass

The Si866x family requires a 0.1 µF bypass capacitor between V_{DD1} and GND1 and V_{DD2} and GND2. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy.

3.3.2 Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

3.4 Fail-Safe Operating Mode

Si86xx devices feature a selectable (by ordering option) mode whereby the default output state (when the input supply is unpowered) can either be a logic high or logic low when the output supply is powered. See Table 3.1 Si866x Logic Operation on page 7 and 1. Ordering Guide for more information.

3.5 Typical Performance Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to the electrical characteristics tables for actual specification limits.

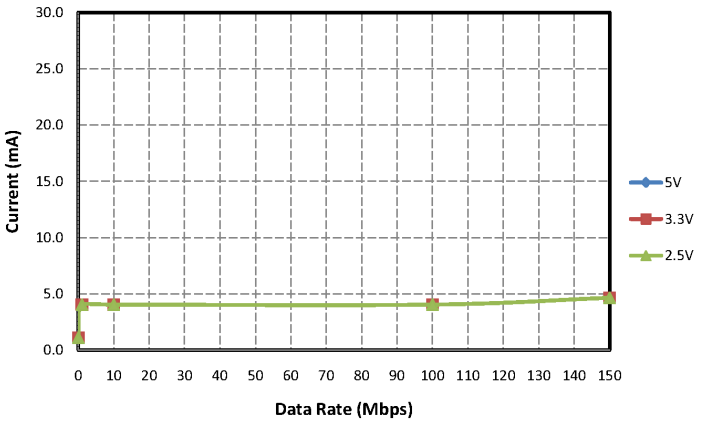


Figure 3.2. Si8660 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation

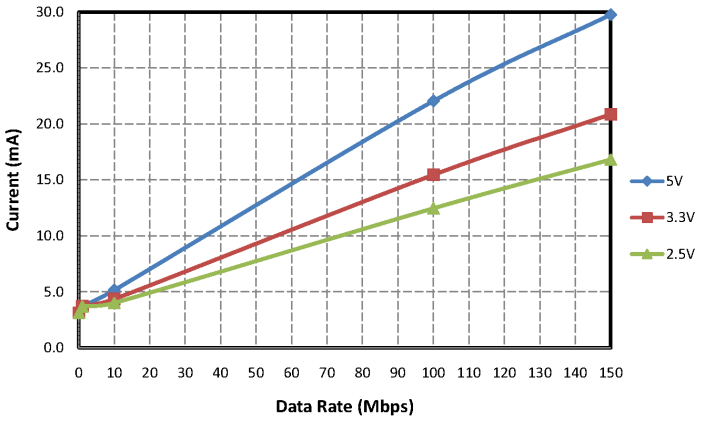


Figure 3.3. Si8661 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

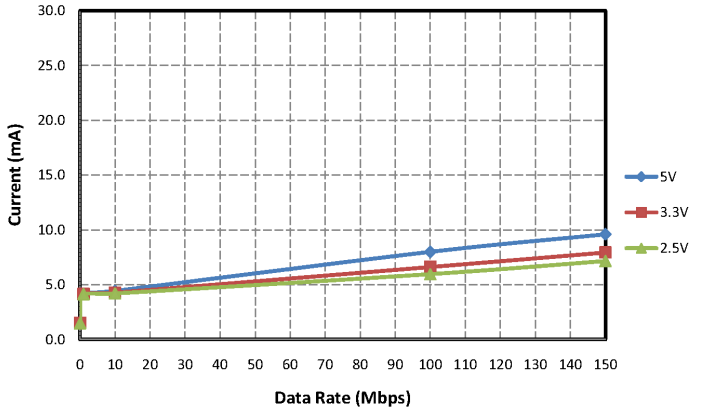


Figure 3.4. Si8662 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

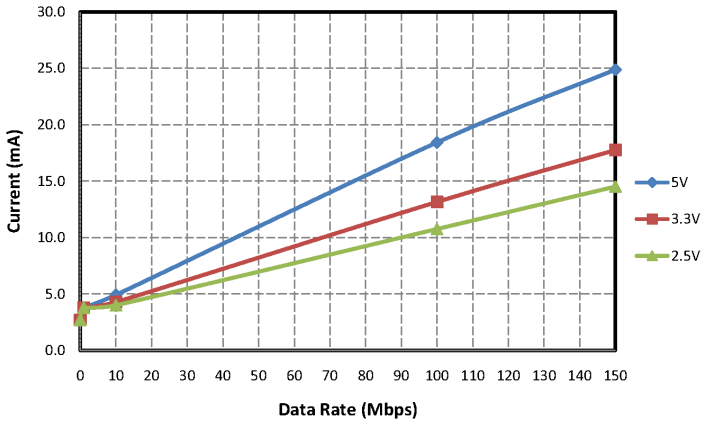


Figure 3.5. Si8660 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

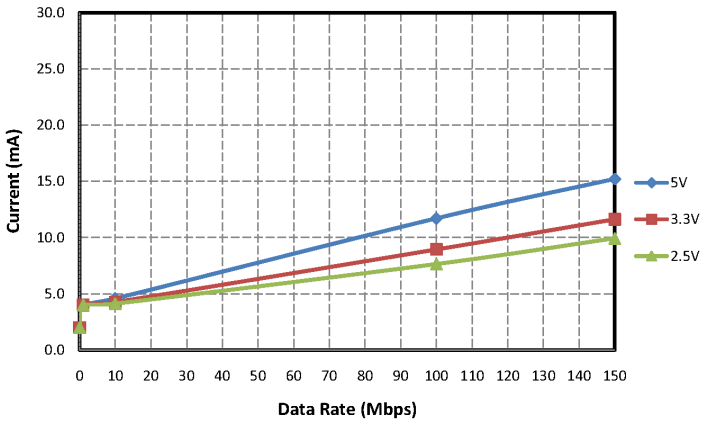


Figure 3.6. Si8661 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

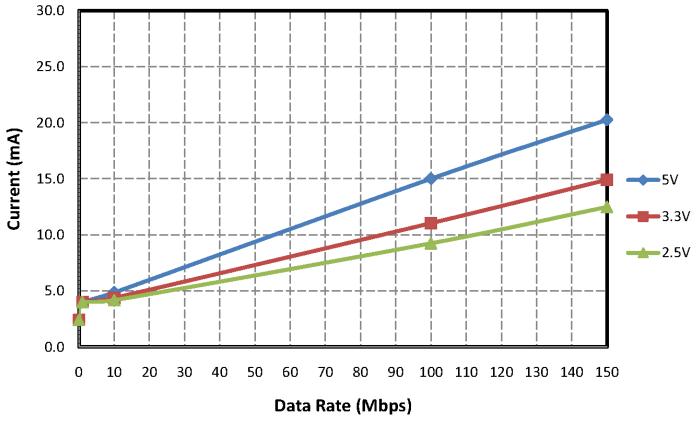


Figure 3.7. Si8662 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

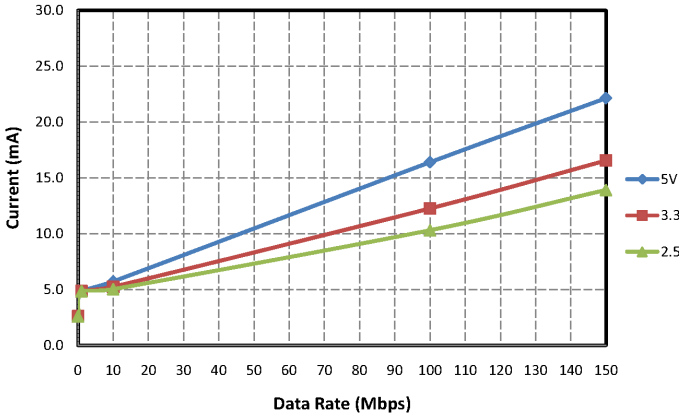


Figure 3.8. Si8663 Typical V_{DD1} or V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

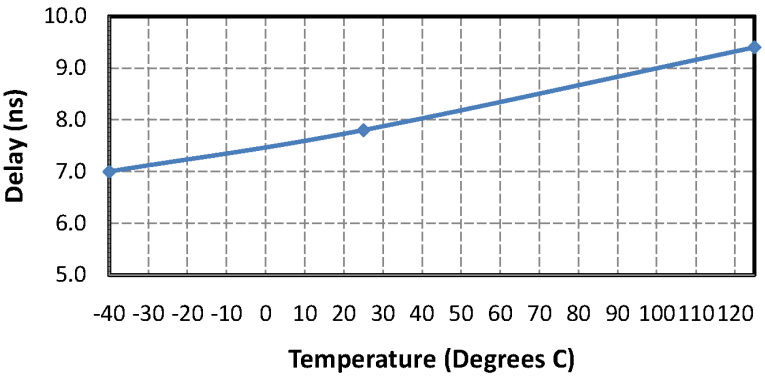


Figure 3.9. Propagation Delay vs. Temperature

4. Electrical Specifications

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Junction Operating Temperature	T_J	—	—	150	°C
Ambient Operating Temperature [1]	T_A	–40	25	125	°C
Supply Voltage	V_{DD1}	2.375	—	5.5	V
	V_{DD2}	2.375	—	5.5	V

Note:
1. The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

Table 4.2. Electrical Characteristics

(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	1.95	2.24	2.375	V
VDD Undervoltage Threshold	VDDUV–	V_{DD1}, V_{DD2} falling	1.88	2.16	2.325	V
VDD Undervoltage Hysteresis	VDD_{HYS}		50	70	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.4	1.67	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.0	1.23	1.4	V
Input Hysteresis	V_{HYS}		0.38	0.44	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance [1]	Z_O		—	50	—	Ω
DC Supply Current (All Inputs 0 V or at Supply)						
Si8660Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.2	1.9	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.5	5.3	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	8.8	12.3	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	3.7	5.6	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8661Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.7	2.7	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.4	5.1	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	7.9	11.1	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	4.8	7.2	
Si8662Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	2.2	3.3	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.0	4.5	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	7.5	10.5	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	5.6	8.4	
Si8663Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	2.6	3.9	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	2.6	3.9	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	6.5	9.1	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	6.5	9.1	
1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, Cl = 15 pF on all Outputs)						
Si8660Bx, Ex						
V_{DD1}			—	5.0	7.0	mA
V_{DD2}			—	4.2	5.9	
Si8661Bx, Ex						
V_{DD1}			—	4.9	6.9	mA
V_{DD2}			—	4.6	6.4	
Si8662Bx, Ex						
V_{DD1}			—	5.1	7.1	mA
V_{DD2}			—	4.7	6.6	
Si8663Bx, Ex						
V_{DD1}			—	4.9	6.8	mA
V_{DD2}			—	4.9	6.8	
10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, Cl = 15 pF on all Outputs)						
Si8660Bx, Ex						
V_{DD1}			—	5.0	7.0	mA
V_{DD2}			—	5.9	8.3	
Si8661Bx, Ex						
V_{DD1}			—	5.2	7.3	mA
V_{DD2}			—	6.1	8.5	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8662Bx, Ex						
V_{DD1}			—	5.6	7.9	mA
V_{DD2}			—	5.9	8.2	
Si8663Bx, Ex						
V_{DD1}			—	5.7	8.0	mA
V_{DD2}			—	5.7	8.0	
100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, Cl = 15 pF on All Outputs)						
Si8660Bx, Ex						
V_{DD1}			—	5.0	7.0	mA
V_{DD2}			—	26.2	34.1	
Si8661Bx, Ex						
V_{DD1}			—	8.8	11.8	mA
V_{DD2}			—	23	29.8	
Si8662Bx, Ex						
V_{DD1}			—	12.8	16.6	mA
V_{DD2}			—	19.4	25.2	
Si8663Bx, Ex						
V_{DD1}			—	16.4	21.3	mA
V_{DD2}			—	16.4	21.3	
Timing Characteristics						
Si866xBx, Ex						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	5.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 4.1 Propagation Delay Timing on page 14	5.0	8.0	13	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 4.1 Propagation Delay Timing on page 14	—	0.2	4.5	ns
Propagation Delay Skew [2]	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew	t_{PSK}		—	0.4	2.5	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF (See Figure 4.1 Propagation Delay Timing on page 14)	—	2.5	4.0	ns
Output Fall Time	t_f	C_L = 15 pF (See Figure 4.1 Propagation Delay Timing on page 14)	—	2.5	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See	—	350	—	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Common Mode Transient Immunity	CMTI	V_I = V_{DD} or 0 V V_{CM} = 1500 V (See Figure 4.2 Common Mode Transient Immunity Test Circuit on page 15)	35	50	—	kV/µs
Startup Time [3]	t_{SU}		—	15	40	µs

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

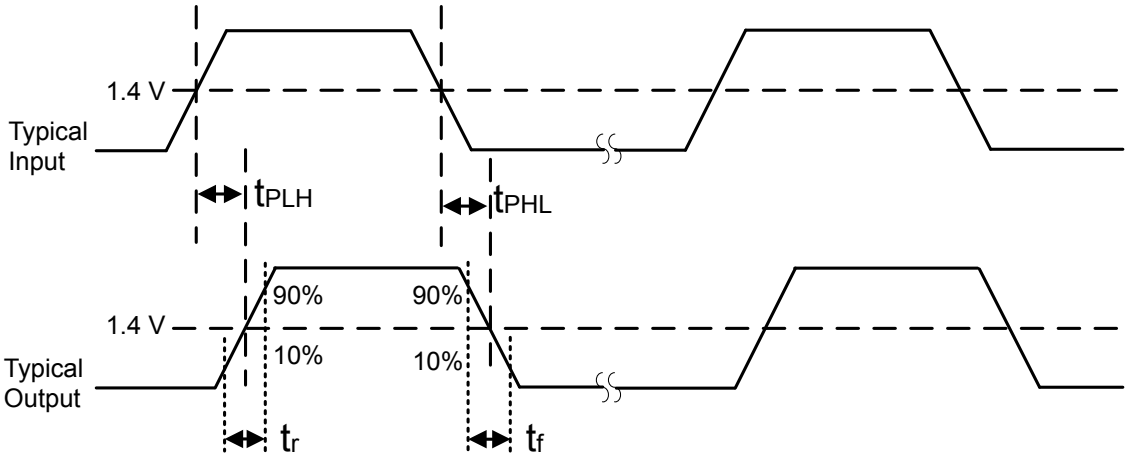


Figure 4.1. Propagation Delay Timing

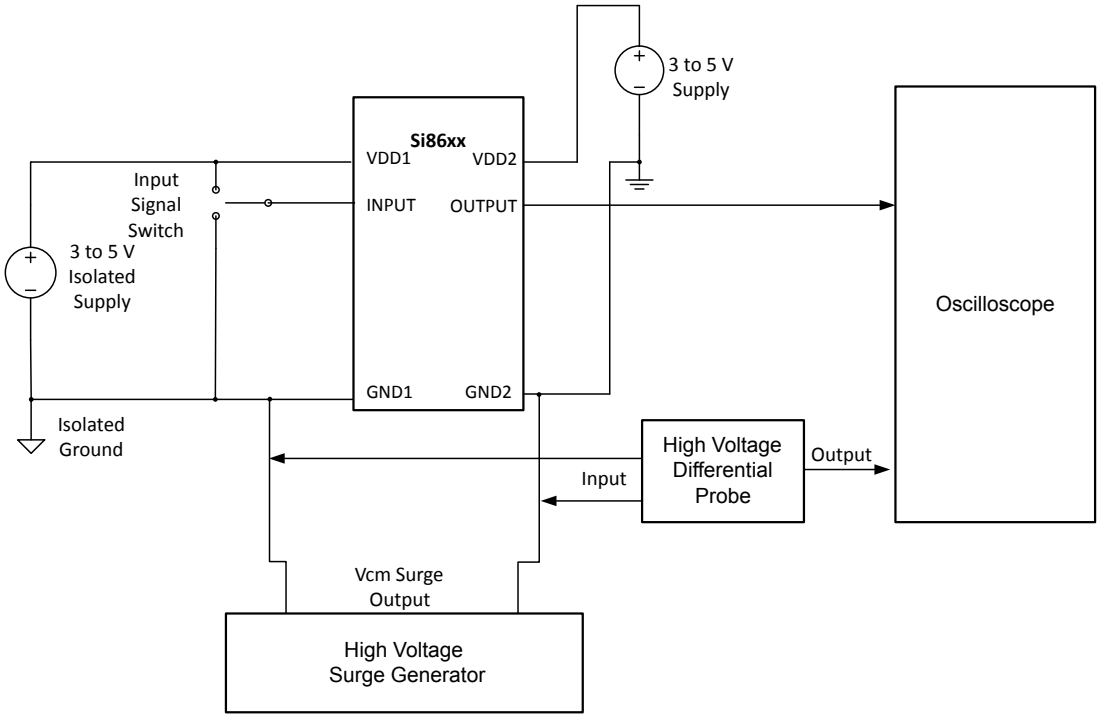


Figure 4.2. Common Mode Transient Immunity Test Circuit

Table 4.3. Electrical Characteristics

(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	1.95	2.24	2.375	V
VDD Undervoltage Threshold	VDDUV–	V_{DD1}, V_{DD2} falling	1.88	2.16	2.325	V
VDD Undervoltage Hysteresis	VDD_{HYS}		50	70	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.4	1.67	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.0	1.23	1.4	V
Input Hysteresis	V_{HYS}		0.38	0.44	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	3.1	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance	Z_O		—	50	—	Ω
DC Supply Current (All Inputs 0 V or at Supply)						

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8660Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.2	1.9	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.5	5.3	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	8.8	12.3	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	3.7	5.6	
Si8661Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.7	2.7	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.4	5.1	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	7.9	11.1	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	4.8	7.2	
Si8662Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	2.2	3.3	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.0	4.5	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	7.5	10.5	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	5.6	8.4	
Si8663Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	2.6	3.9	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	2.6	3.9	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	6.5	9.1	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	6.5	9.1	
1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, Cl = 15 pF on All Outputs)						
Si8660Bx, Ex						
V_{DD1}			—	5.0	7.0	mA
V_{DD2}			—	4.2	5.9	
Si8661Bx, Ex						
V_{DD1}			—	4.9	6.9	mA
V_{DD2}			—	4.6	6.4	
Si8662Bx, Ex						
V_{DD1}			—	5.1	7.1	mA
V_{DD2}			—	4.7	6.6	
Si8663Bx, Ex						
V_{DD1}			—	4.9	6.8	mA
V_{DD2}			—	4.9	6.8	
10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, Cl = 15 pF on All Outputs)						

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8660Bx, Ex						
V_{DD1}			—	5.0	7.0	mA
V_{DD2}			—	5.0	7.0	
Si8661Bx, Ex						
V_{DD1}			—	5.0	7.0	mA
V_{DD2}			—	5.3	7.4	
Si8662Bx, Ex						
V_{DD1}			—	5.3	7.4	mA
V_{DD2}			—	5.2	7.3	
Si8663Bx, Ex						
V_{DD1}			—	5.2	7.3	mA
V_{DD2}			—	5.2	7.3	
100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, Cl = 15 pF on All Outputs)						
Si8660Bx, Ex						
V_{DD1}			—	5.0	7.0	mA
V_{DD2}			—	18.3	23.8	
Si8661Bx, Ex						
V_{DD1}			—	7.4	9.9	mA
V_{DD2}			—	16.4	21.3	
Si8662Bx, Ex						
V_{DD1}			—	10	13	mA
V_{DD2}			—	14.1	18.3	
Si8663Bx, Ex						
V_{DD1}			—	12.3	15.9	mA
V_{DD2}			—	12.3	15.9	
Timing Characteristics						
Si866xBx, Ex						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	5.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 4.1 Propagation Delay Timing on page 14	5.0	8.0	13	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 4.1 Propagation Delay Timing on page 14	—	0.2	4.5	ns
Propagation Delay Skew [2]	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew	t_{PSK}		—	0.4	2.5	ns
All Models						

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Rise Time	t_r	C_L = 15 pF See Figure 4.1 Propagation Delay Timing on page 14	—	2.5	4.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 4.1 Propagation Delay Timing on page 14	—	2.5	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 2.3 Eye Diagram on page 6	—	350	—	ps
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V V_{CM} = 1500 V (See Figure 4.2 Common Mode Transient Immunity Test Circuit on page 15)	35	50	—	kV/µs
Startup Time [3]	t_{SU}		—	15	40	µs

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4.4. Electrical Characteristics

(V_{DD1} = 2.5 V ±5%, V_{DD2} = 2.5 V ±5%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	1.95	2.24	2.375	V
VDD Undervoltage Threshold	VDDUV–	V_{DD1}, V_{DD2} falling	1.88	2.16	2.325	V
VDD Undervoltage Hysteresis	VDD_{HYS}		50	70	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.4	1.67	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.0	1.23	1.4	V
Input Hysteresis	V_{HYS}		0.38	0.44	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	2.3	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	50	—	Ω
DC Supply Current (All Inputs 0 V or at Supply)						
Si8660Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.2	1.9	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.5	5.3	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	8.8	12.3	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	3.7	5.6	
Si8661Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.7	2.7	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.4	5.1	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	7.9	11.1	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	4.8	7.2	
Si8662Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	2.2	3.3	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.0	4.5	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	7.5	10.5	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	5.6	8.4	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8663Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	2.6	3.9	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	2.6	3.9	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	6.5	9.1	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	6.5	9.1	
1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, Cl = 15 pF on All Outputs)						
Si8660Bx, Ex						
V_{DD1}			—	5.0	7.0	mA
V_{DD2}			—	4.2	5.9	
Si8661Bx, Ex						
V_{DD1}			—	4.9	6.9	mA
V_{DD2}			—	4.6	6.4	
Si8662Bx, Ex						
V_{DD1}			—	5.1	7.1	mA
V_{DD2}			—	4.7	6.6	
Si8663Bx, Ex						
V_{DD1}			—	4.9	6.8	mA
V_{DD2}			—	4.9	6.8	
10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, Cl = 15 pF on All Outputs)						
Si8660Bx, Ex						
V_{DD1}			—	5.0	7.0	mA
V_{DD2}			—	4.6	6.4	
Si8661Bx, Ex						
V_{DD1}			—	5.0	6.9	mA
V_{DD2}			—	4.9	6.9	
Si8662Bx, Ex						
V_{DD1}			—	5.2	7.2	mA
V_{DD2}			—	4.9	6.9	
Si8663Bx, Ex						
V_{DD1}			—	5.0	7.0	mA
V_{DD2}			—	5.0	7.0	
100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, Cl = 15 pF on All Outputs)						
Si8660Bx, Ex						
V_{DD1}			—	5.0	7.0	mA
V_{DD2}			—	14.7	19.1	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8661Bx, Ex						
V_{DD1}			—	6.7	9.1	mA
V_{DD2}			—	13.4	17.4	
Si8662Bx, Ex						
V_{DD1}			—	8.7	11.3	mA
V_{DD2}			—	11.7	15.2	
Si8663Bx, Ex						
V_{DD1}			—	10.3	13.4	mA
V_{DD2}			—	10.3	13.4	
Timing Characteristics						
Si866xBx, Ex						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	5.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 4.1 Propagation Delay Timing on page 14	5.0	8.0	14	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 4.1 Propagation Delay Timing on page 14	—	0.2	5.0	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	5.0	ns
Channel-Channel Skew	t_{PSK}		—	0.4	2.5	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 4.1 Propagation Delay Timing on page 14	—	2.5	4.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 4.1 Propagation Delay Timing on page 14	—	2.5	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 2.3 Eye Diagram on page 6	—	350	—	ps
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V V_{CM} = 1500 V (See Figure 4.2 Common Mode Transient Immunity Test Circuit on page 15)	35	50	—	kV/µs
Startup Time[3]	t_{SU}		—	15	40	µs

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4.5. Regulatory Information [1]

CSA
The Si866x is certified under CSA Component Acceptance Notice 5A. For more details, see Master Contract Number 232873.
60950-1, 62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Up to 250 V_{RMS} working voltage and 2 MOPP (Means of Patient Protection).
VDE
The Si866x is certified according to VDE 0884-10. For more details, see certificate 40018443.
0884-10: Up to 1200 V_{peak} for basic insulation working voltage.
60950-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
UL
The Si866x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage for basic protection.
CQC
The Si866x is certified under GB4943.1-2011. For more details, see certificates CQC13001096110 and CQC13001096239.
Rated up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
Note: 1. Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec. Regulatory Certifications apply to 3.75 kV_{RMS} rated devices which are production tested to 4.5 kV_{RMS} for 1 sec. Regulatory Certifications apply to 5.0 kV_{RMS} rated devices which are production tested to 6.0 kV_{RMS} for 1 sec. For more information, see 1. Ordering Guide.

Table 4.6. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value			Unit
			WB SOIC-16	NB SOIC-16	QSOP-16	
Nominal External Air Gap (Clearance)[1]	CLR		8.0	4.9	3.6	mm
Nominal External Tracking (Creepage) [1]	CPG		8.0	4.01	3.6	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.014	0.014	0.014	mm
Tracking Resistance	CTI or PTI	IEC60112	600	600	600	V_{RMS}
Erosion Depth	ED		0.019	0.019	0.031	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	10^{12}	10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	2.0	2.0	2.0	pF
Input Capacitance[3]	C_I		4.0	4.0	4.0	pF

Parameter	Symbol	Test Condition	Value			Unit
			WB SOIC-16	NB SOIC-16	QSOP-16	

Note:

1. The values in this table correspond to the nominal creepage and clearance values. VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC-16 package and QSOP-16 packages and 8.5 mm minimum for the WB SOIC-16 package. UL does not impose a clearance and creepage minimum for component-level certifications. CSA certifies the clearance and creepage of the WB SOIC-16 package with designation "IS2" as 8 mm minimum. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC 16, 3.6 mm minimum for the QSOP-16, and 7.6 mm minimum for the WB SOIC-16 package with package designation "IS" as listed in the data sheet.
2. To determine resistance and capacitance, the Si86xx is converted into a 2-terminal device. Pins 1–8 are shorted together to form the first termina and pins 9–16 are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

Table 4.7. IEC 60664-1 Ratings

Parameter	Test Conditions	Specification		
		WB SOIC-16	NB SOIC-16	QSOP-16
Basic Isolation Group	Material Group	I	I	I
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV	I-IV	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-IV	I-III	I-III
	Rated Mains Voltages ≤ 400 V_{RMS}	I-III	I-II	I-II
	Rated Mains Voltages ≤ 600 V_{RMS}	I-III	I-II	I-II

Table 4.8. VDE 0884-10 Insulation Characteristics for Si86xxxx[1]

Parameter	Symbol	Test Condition	Characteristic			Unit
			WB SOIC-16	NB SOIC-16	QSOP-16	
Maximum Working Insulation Voltage	V_{IORM}		1200	630	630	Vpeak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = VPR, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	2250	1182	1182	Vpeak
Transient Overvoltage	V_{IOTM}	t = 60 sec	6000	6000	6000	Vpeak
Surge Voltage	V_{IOSM}	Tested per IEC 60065 with surge voltage of 1.2 µs/50 µs Si866xxB/C/D tested with 4000 V	3077	3077	3077	Vpeak
Pollution Degree (DIN VDE 0110, Table 1)			2	2	2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	$>10^9$	$>10^9$	Ω

Note:
1. Maintenance of the safety data is ensured by protective circuits. The Si86xxxx provides a climate classification of 40/125/21.

Table 4.9. VDE 0884-10 Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Max			Unit
			WB SOIC-16	NB SOIC-16	QSOP-16	
Case Temperature	T_S		150	150	150	°C
Safety Input, Output, or Supply Current	I_S	θ_{JA} = 100 °C/W (WB SOIC-16) 105 °C/W (NB SOIC-16, QSOP-16) V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	220	215	215	mA
Device Power Dissipation[2]	P_D		415	415	415	mW

Note:
1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figure 4.3 (WB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per VDE 0884-10 on page 25 and Figure 4.4 (NB SOIC-16, QSOP-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per VDE 0884-10 on page 25.
2. The Si86xx is tested with VDD1 = VDD2 = 5.5 V; T_J = 150 ºC; C_L = 15 pF, input a 150 Mbps 50% duty cycle square wave.

Table 4.10. Thermal Characteristics

Parameter	Symbol	WB SOIC-16	NB SOIC-16/QSOP-16	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	100	105	°C/W

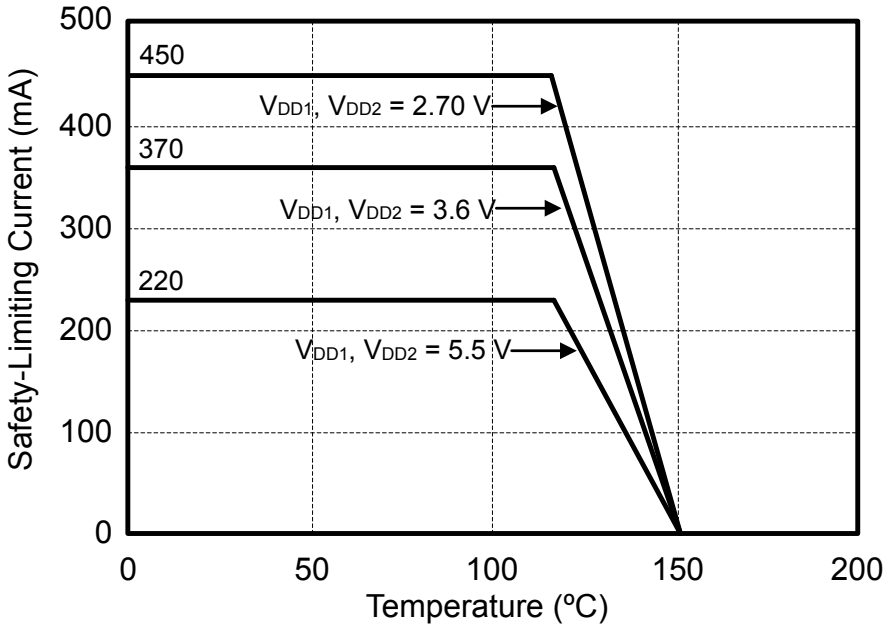


Figure 4.3. (WB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per VDE 0884-10

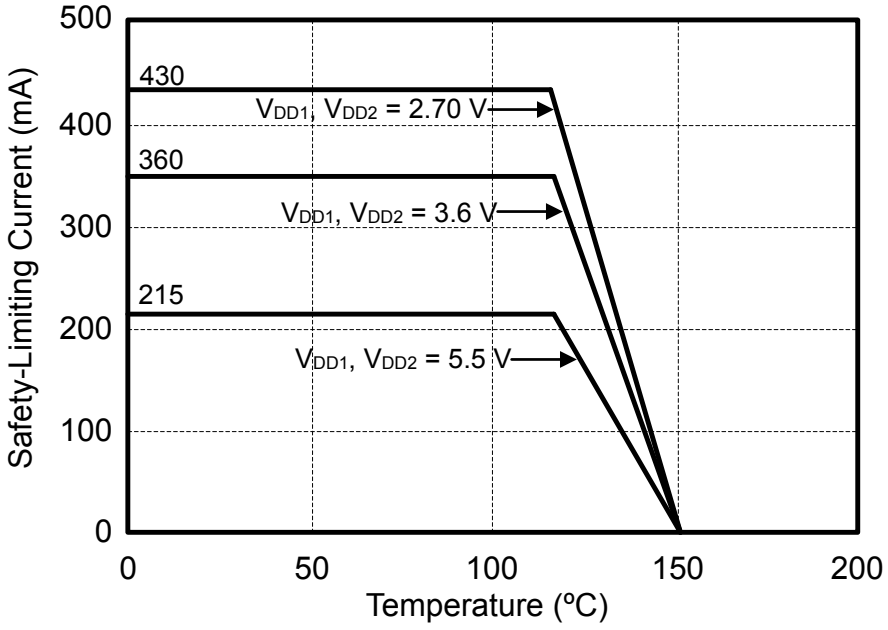


Figure 4.4. (NB SOIC-16, QSOP-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per VDE 0884-10

Table 4.11. Absolute Maximum Ratings [1]

Parameter	Symbol	Min	Max	Unit
Storage Temperature [2]	T_{STG}	–65	150	°C
Ambient Temperature Under Bias	T_A	–40	125	°C
Junction Temperature	T_J	—	150	°C
Supply Voltage	V_{DD1}, V_{DD2}	–0.5	7.0	V
Input Voltage	V_I	–0.5	V_{DD} + 0.5	V
Output Voltage	V_O	–0.5	V_{DD} + 0.5	V
Output Current Drive Channel	I_O	—	10	mA
Lead Solder Temperature (10 s)		—	260	°C
Maximum Isolation (Input to Output) (1 sec) NB SOIC-16, QSOP-16		—	4500	V_{RMS}
Maximum Isolation (Input to Output) (1 sec) WB SOIC-16		—	6500	V_{RMS}

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet.
2. VDE certifies storage temperature from –40 to 150 °C.

5. Pin Descriptions

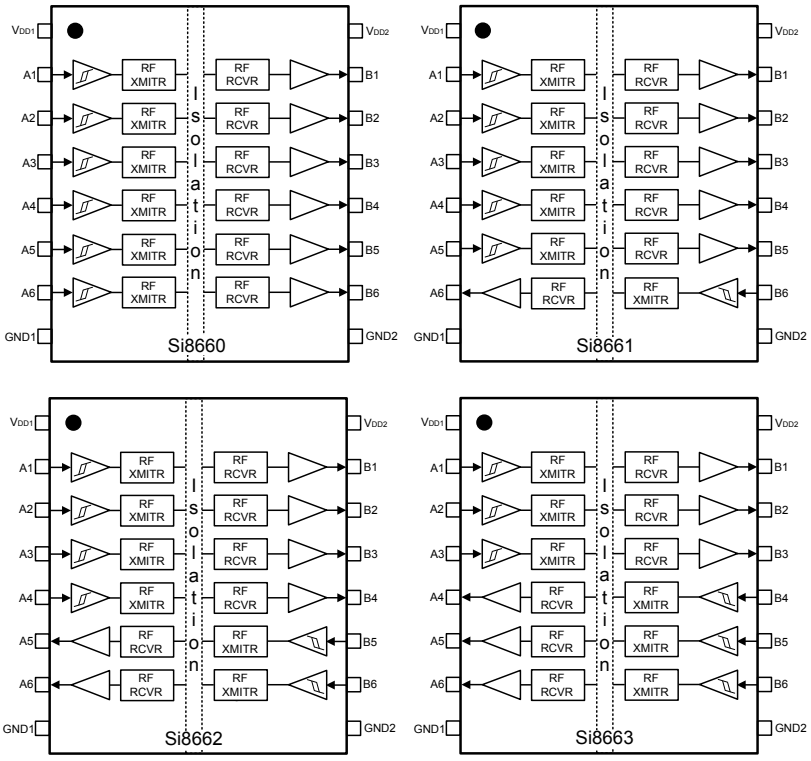


Figure 5.1. Si866x Pinout

Table 5.1. Si866x Pin Descriptions

Name	SOIC-16 Pin#	Type	Description
V_{DD1}	1	Supply	Side 1 power supply.
A1	2	Digital Input	Side 1 digital input.
A2	3	Digital Input	Side 1 digital input.
A3	4	Digital Input	Side 1 digital input.
A4	5	Digital I/O	Side 1 digital input or output.
A5	6	Digital I/O	Side 1 digital input or output.
A6	7	Digital I/O	Side 1 digital input or output.
GND1	8	Ground	Side 1 ground.
GND2	9	Ground	Side 2 ground.
B6	10	Digital I/O	Side 2 digital input or output.
B5	11	Digital I/O	Side 2 digital input or output.
B4	12	Digital I/O	Side 2 digital input or output.
B3	13	Digital Output	Side 2 digital output.
B2	14	Digital Output	Side 2 digital output.
B1	15	Digital Output	Side 2 digital output.
V_{DD2}	16	Supply	Side 2 power supply.

6. Package Outline (16-Pin Wide Body SOIC)

The figure below illustrates the package details for the Si86xx digital isolator in a 16-pin wide-body SOIC package. The table below lists the values for the dimensions shown in the illustration.

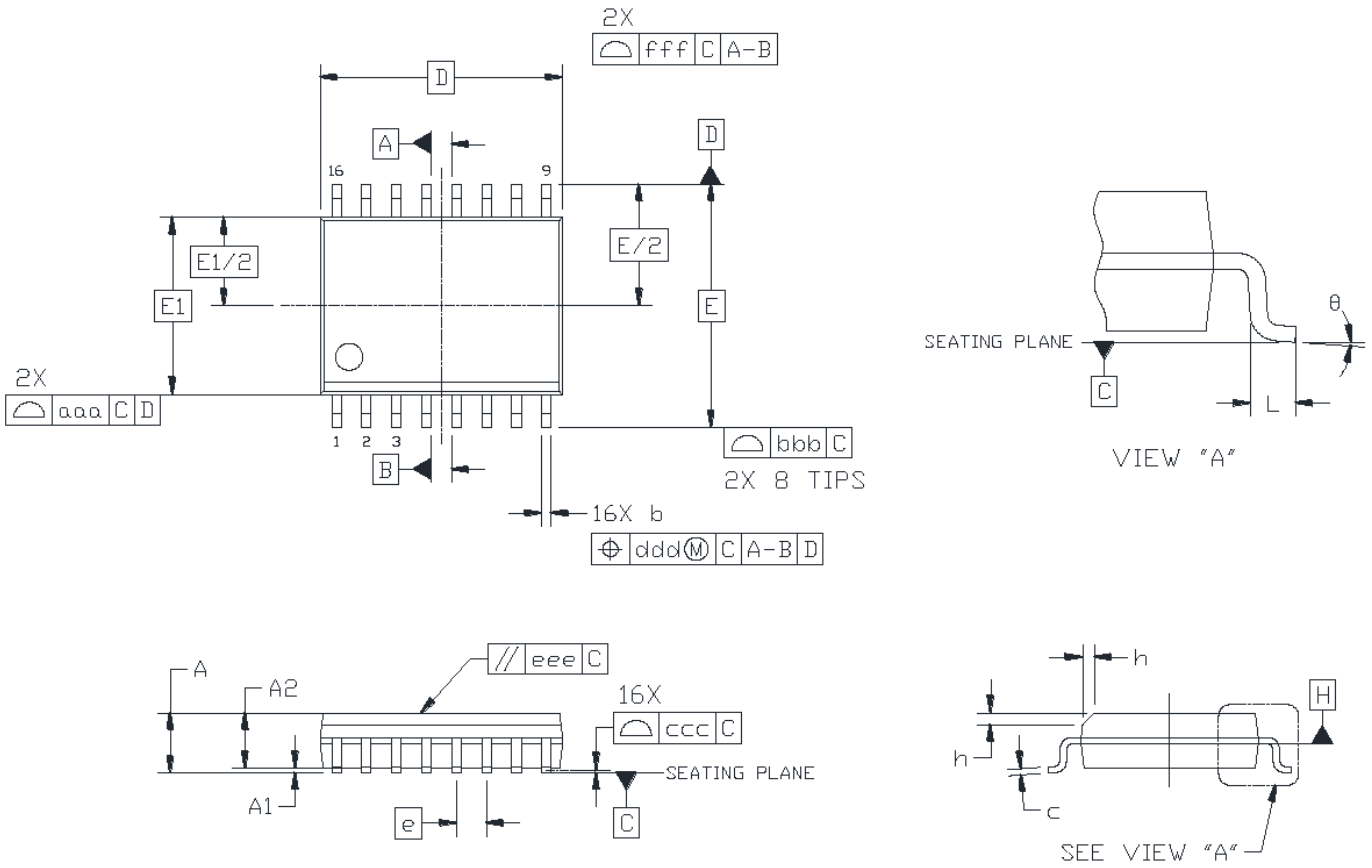


Figure 6.1. 16-Pin Wide Body SOIC

Table 6.1. 16-Pin Wide Body SOIC Package Diagram Dimensions

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	0°	8°
ααα	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020 specification for small body, lead-free components.

7. Land Pattern (16-Pin Wide-Body SOIC)

The figure below illustrates the recommended land pattern details for the Si86xx in a 16-pin wide-body SOIC package. The table below lists the values for the dimensions shown in the illustration.

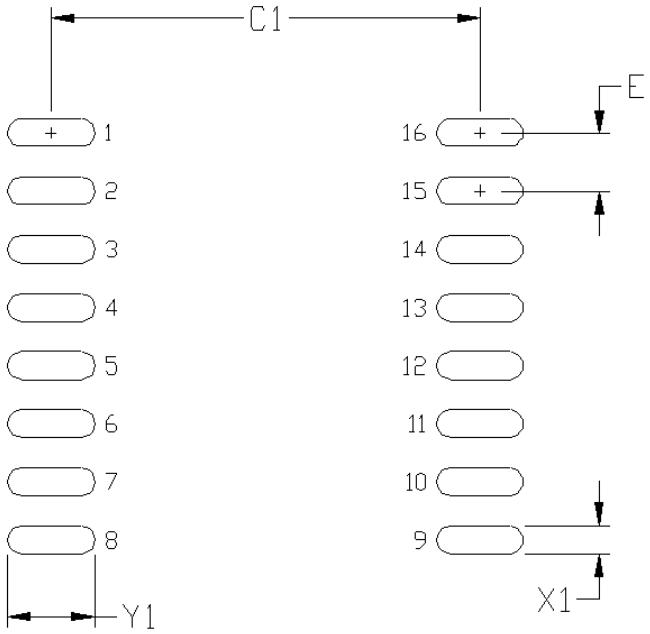


Figure 7.1. 16-Pin Wide Body SOIC PCB Land Pattern

Table 7.1. 16-Pin Wide Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

8. Package Outline (16-Pin Narrow Body SOIC)

The figure below illustrates the package details for the Si86xx in a 16-pin narrow-body SOIC package. The table below lists the values for the dimensions shown in the illustration.

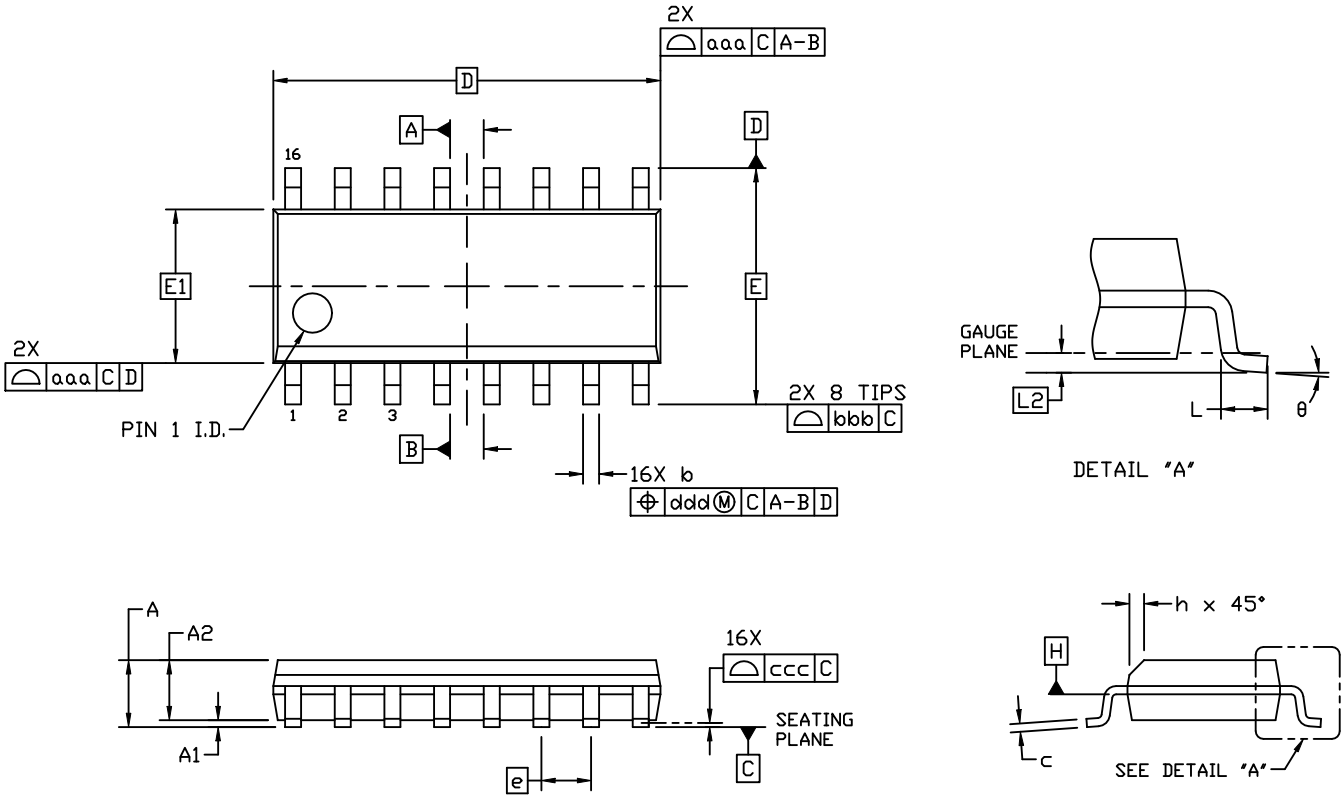


Figure 8.1. 16-Pin Narrow Body SOIC

Table 8.1. 16-Pin Narrow Body SOIC Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Land Pattern (16-Pin Narrow Body SOIC)

The figure below illustrates the recommended land pattern details for the Si86xx in a 16-pin narrow-body SOIC package. The table below lists the values for the dimensions shown in the illustration.

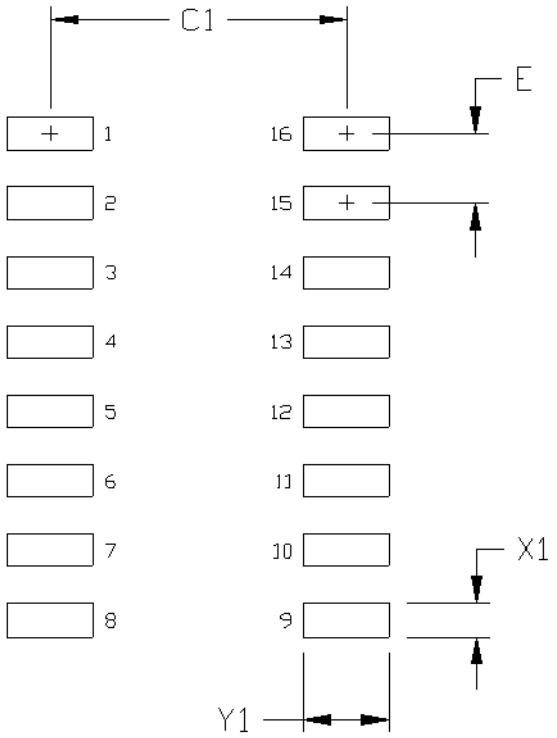


Figure 9.1. 16-Pin Narrow Body SOIC PCB Land Pattern

Table 9.1. 16-Pin Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

10. Package Outline (16-Pin QSOP)

The figure below illustrates the package details for the Si86xx in a 16-pin QSOP package. The table lists the values for the dimensions shown in the illustration.

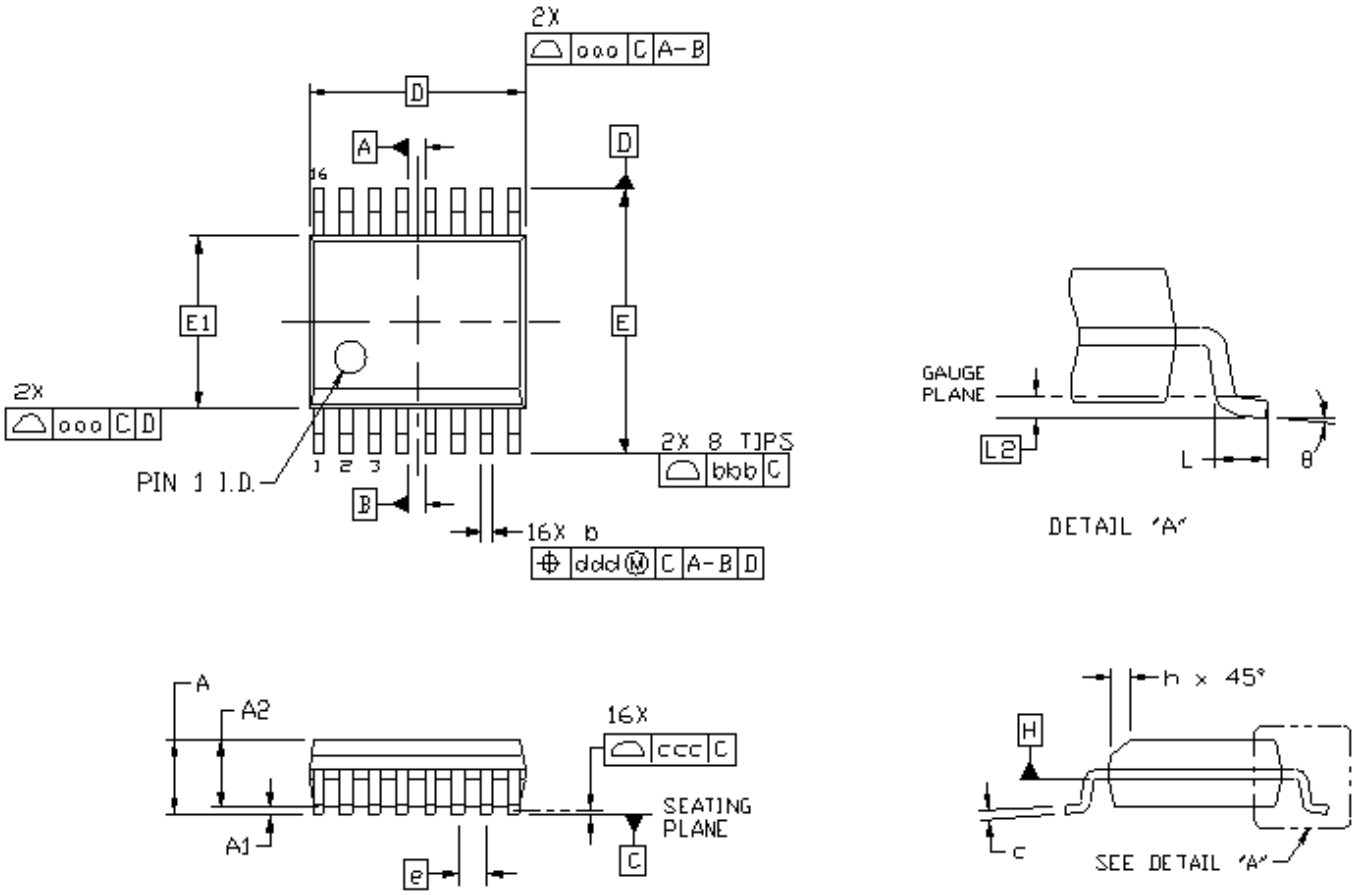


Figure 10.1. 16-Pin QSOP Package

Table 10.1. 16-Pin QSOP Package Diagram Dimensions[1, 2, 3, 4]

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.20	0.30
c	0.17	0.25
D	4.89 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	0.635 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-137, Variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. Land Pattern (16-Pin QSOP)

The figure below illustrates the recommended land pattern details for the Si86xx in a 16-pin QSOP package. The table lists the values for the dimensions shown in the illustration.

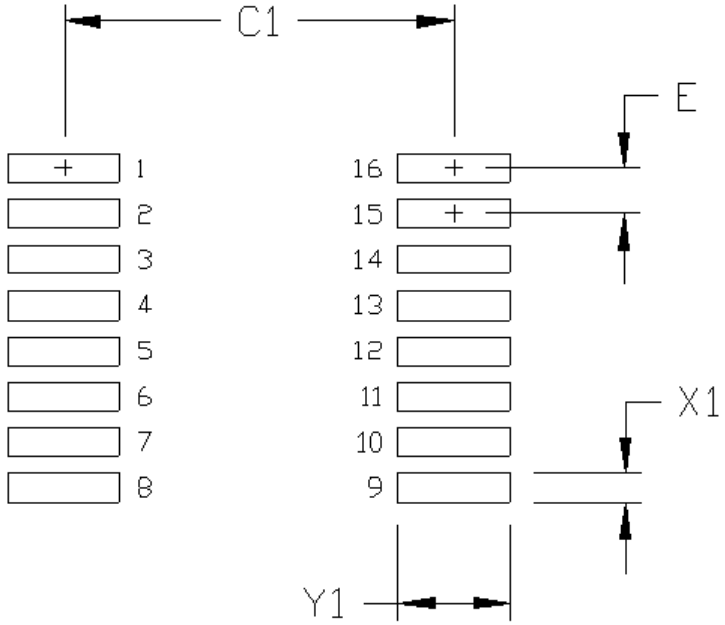


Figure 11.1. 16-Pin QSOP PCB Land Pattern

Table 11.1. 16-Pin QSOP Land Pattern Dimensions[1, 2]

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	0.635
X1	Pad Width	0.40
Y1	Pad Length	1.55

Note:

1. This Land Pattern Design is based on IPC-7351 pattern SOP63P602X173-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

12. Top Marking (16-Pin Wide Body SOIC)

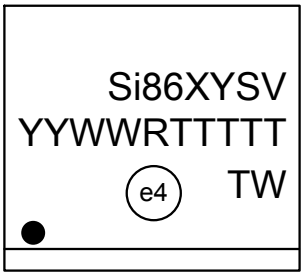


Figure 12.1. 16-Pin Wide Body SOIC Top Marking

Table 12.1. 16-Pin Wide Body SOIC Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See 1. Ordering Guide for more information.)	Si86 = Isolator product series XY = Channel Configuration X = # of data channels (6) Y = # of reverse channels (3, 2, 1, 0) S = Speed Grade A = 1 Mbps B = 150 Mbps (default output = low) E = 150 Mbps (default output = high) V = Insulation rating A = 1 kV; B = 2.5 kV; C = 3.75 kV; D = 5.0 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by assembly subcontractor. Corresponds to the year and workweek of the mold date.
	RTTTTT = Mfg Code	Manufacturing code from assembly house “R” indicates revision
Line 3 Marking:	Circle = 1.7 mm Diameter (Center-Justified)	“e4” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan as shown, TH = Thailand

13. Top Marking (16-Pin Narrow Body SOIC)

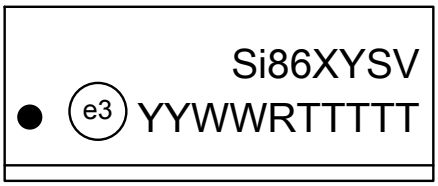


Figure 13.1. 16-Pin Narrow Body SOIC Top Marking

Table 13.1. 16-Pin Narrow Body SOIC Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See 1. Ordering Guide for more information.)	Si86 = Isolator product series XY = Channel Configuration X = # of data channels (6) Y = # of reverse channels (3, 2, 1, 0) S = Speed Grade A = 1 Mbps B = 150 Mbps (default output = low) E = 150 Mbps (default output = high) V = Insulation rating A = 1 kV; B = 2.5 kV; C = 3.75 kV
Line 2 Marking:	Circle = 1.2 mm Diameter	“e3” Pb-Free Symbol
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
	RTTTTT = Mfg Code	Manufacturing code from assembly house. “R” indicates revision.
	Circle = 1.2 mm diameter	“e3” Pb-Free Symbol.

14. Top Marking (16-Pin QSOP)

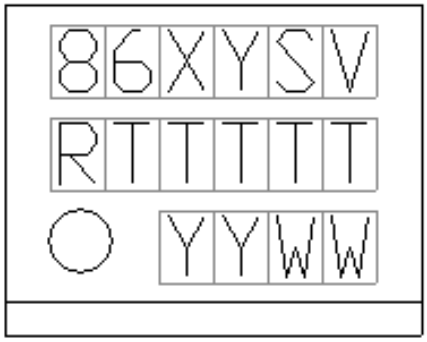


Figure 14.1. 16-Pin QSOP Top Marking

Table 14.1. 16-Pin QSOP Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See 1. Ordering Guide for more information).	86 = Isolator product series XY = Channel Configuration X = # of data channels (6) Y = # of reverse channels (3, 2, 1, 0) S = Speed Grade (max data rate) and operating mode: B = 150 Mbps (default output = low) E = 150 Mbps (default output = high) V = Insulation rating A = 1 kV; B = 2.5 kV; C = 3.75 kV
Line 2 Marking:	RTTTTT = Mfg Code	Manufacturing code from assembly house “R” indicates revision
Line 3 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.

15. Document Change List

Revision 0.1

September 15, 2010
- Initial release.

Revision 0.1 to Revision 1.0

March 31, 2011
- Added chip graphics on front page.
- Updated features list on front page.
- Moved Table 4.1 Recommended Operating Conditions on page 11 and Table 4.11 Absolute Maximum Ratings [1] on page 26.
- Updated 4. Electrical Specifications.
- Moved Table 3.1 Si866x Logic Operation on page 7.
- Moved and updated 3.5 Typical Performance Characteristics.
- Updated Table 5.1 Si866x Pin Descriptions on page 27.
- Updated 1. Ordering Guide.
- Removed references to QSOP-16 package.

Revision 1.0 to Revision 1.1

July 14, 2011
- Reordered spec tables to conform to new convention.
- Removed “pending” throughout document.

Revision 1.1 to Revision 1.2

September 14, 2011
- Reordered spec tables to conform to new convention.
- Removed “pending” throughout document.

Revision 1.2 to Revision 1.3

March 21, 2012
- Updated 1. Ordering Guide to include MSL2A.

Revision 1.3 to Revision 1.4

June 26, 2012
- Updated Table 4.11 Absolute Maximum Ratings [1] on page 26.
  - Added junction temperature spec.
- Updated 3.3.1 Supply Bypass.
- Removed “3.3.2. Pin Connections”.
- Updated 1. Ordering Guide.
  - Removed Rev A devices.
- Updated 6. Package Outline (16-Pin Wide Body SOIC).
- Updated Top Marks.
  - Added revision description.

Revision 1.4 to Revision 1.5

September 25, 2013
- Added Figure 4.2 Common Mode Transient Immunity Test Circuit on page 15.
- Added references to CQC throughout.
- Added references to 2.5 kVRMS devices throughout.
- Updated 1. Ordering Guide.

- Updated 12. Top Marking (16-Pin Wide Body SOIC).

Revision 1.5 to Revision 1.6

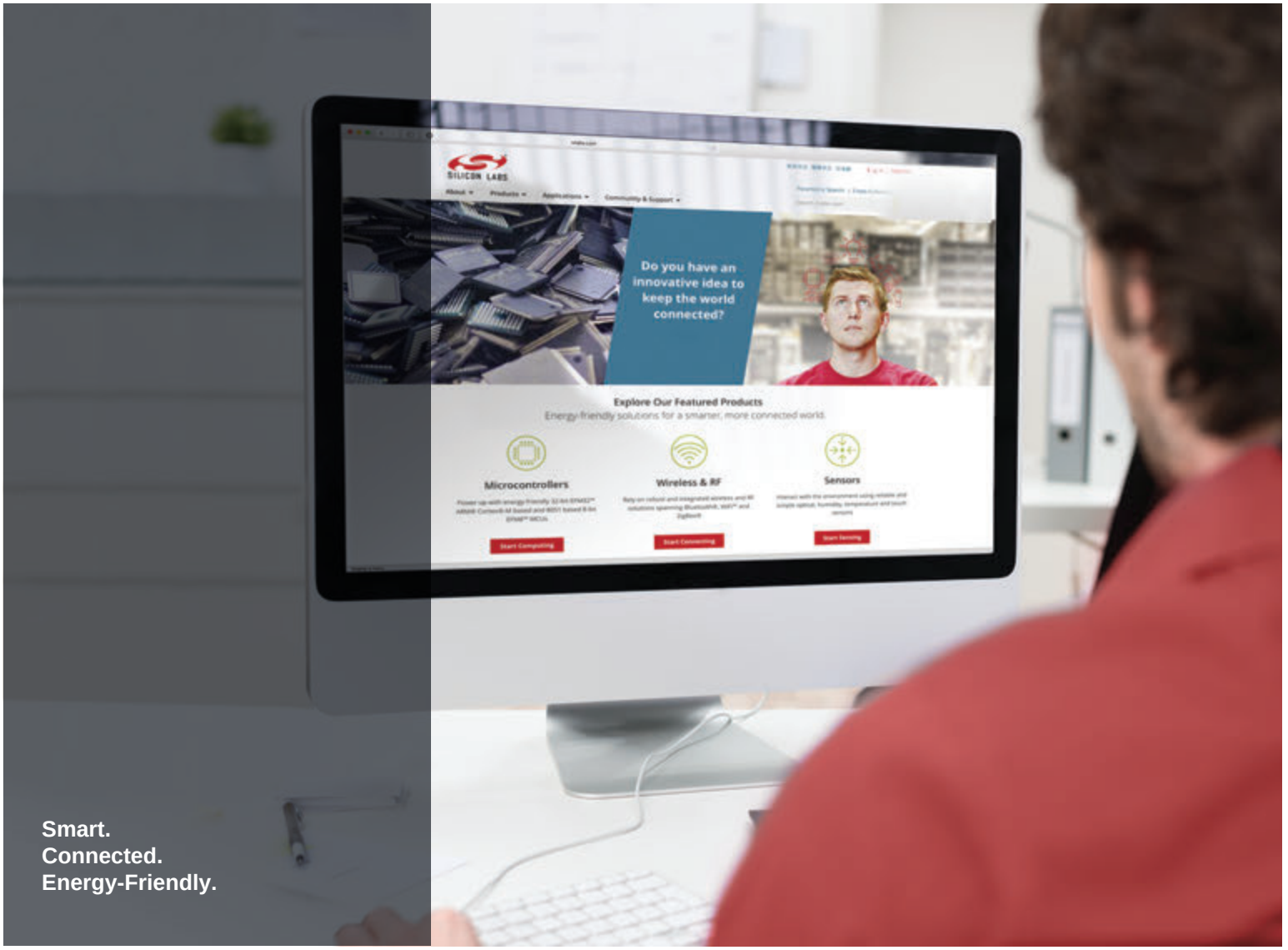
June 18, 2015

- Updated Table 4.5 Regulatory Information [1] on page 22.
  - Added CQC certificate numbers.
- Updated 1. Ordering Guide.
  - Removed references to moisture sensitivity levels.
  - Removed Note 2.
- Added note to Table 1.1 Ordering Guide for Valid OPNs [1,2, 3] on page 2 for denoting tape and reel marking.

Revision 1.6 to Revision 1.7

October 18, 2017

- Added new OPNs in Ordering Guide for IU (QSOP) and IS2 (8 mm creepage WB SOIC) package options.
- Added 62368-1 references throughout.
- Removed 61010-1 references throughout.
- Added QSOP-16 package information.



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