1.5A USB-FRIENDLY Li-Ion BATTERY CHARGER AND POWER-PATH MANAGEMENT IC

Check for Samples: bq24075-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified with the following results**
  - **Device Temperature Grade 1: -40°C to +125°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C3B**
- **Fully Compliant USB Charger**
  - **Selectable 100mA and 500mA Maximum Input Current**
  - **100mA Maximum Current Limit Ensures Compliance to USB-IF Standard**
  - **Input based Dynamic Power Management (V_{IN}-DPM) for Protection Against Poor USB Sources**
- **28V Input Rating with Overvoltage Protection**
- **Integrated Dynamic Power Path Management (DPPM) Function Simultaneously and Independently Powers the System and Charges the Battery**
- **Supports up to 1.5A Charge Current with Current Monitoring Output (ISET)**
- **Programmable Input Current Limit up to 1.5A for Wall Adapters**
- **Battery Disconnect Function with SYSOFF Input**
- **Programmable Pre-Charge and Fast-Charge Safety Timers**
- **Reverse Current, Short-Circuit and Thermal Protection**
- **NTC Thermistor Input**
- **Proprietary Start Up Sequence Limits Inrush Current**
- **Status Indication – Charging/Done, Power Good**
- **Small 3 mm × 3 mm 16 Lead QFN Package**

APPLICATIONS

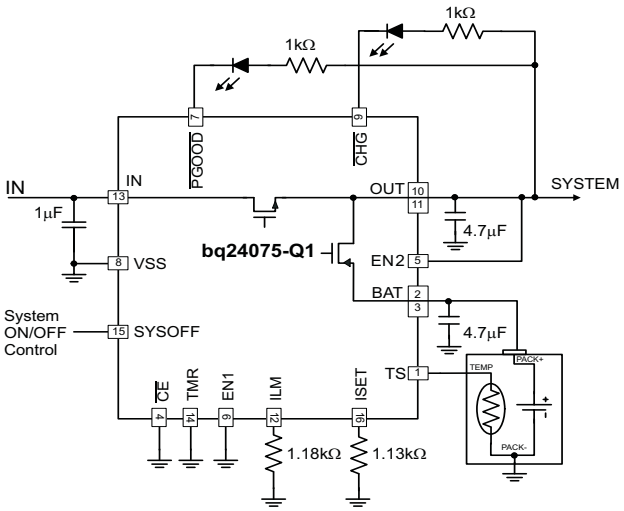
- **Automotive**

DESCRIPTION

The bq24075-Q1 device is integrated Li-ion linear charger and system power path management device targeted at space-limited portable applications. The device operate from either a USB port or AC adapter and support charge currents up to 1.5A. The input voltage range with input overvoltage protection supports unregulated adapters. The USB input current limit accuracy and start up sequence allow the bq24075-Q1 to meet USB-IF inrush current specification. Additionally, the input dynamic power management (V_{IN}-DPM) prevents the charger from crashing incorrectly configured USB sources.

The bq24075-Q1 features dynamic power path management (DPPM) that powers the system while simultaneously and independently charging the battery. The DPPM circuit reduces the charge current when the input current limit causes the system output to fall to the DPPM threshold; thus, supplying the system load at all times while monitoring the charge current separately. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination and enables the system to run with a defective or absent battery pack.

Typical Application Circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

Additionally, the regulated system input enables instant system turn-on when plugged in even with a totally discharged battery. The power-path management architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents, enabling the use of a smaller adapter.

The battery is charged in three phases: conditioning, constant current, and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if the internal temperature threshold is exceeded. The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy current and voltage regulation loops, charge status display, and charge termination. The input current limit and charge current are programmable using external resistors.

ORDERING INFORMATION

PART NUMBER (1) (2)	V_{OVP}	$V_{BAT(REG)}$	$V_{OUT(REG)}$	V_{DPPM}	OPTIONAL FUNCTION	MARKING
bq24075QRGTRQ1	6.6 V	4.2V	5.5 V	4.3 V	SYSOFF	SAM

(1) The RGT package is available in the following options:
R - taped and reeled in quantities of 3,000 devices per reel.
T - taped and reeled in quantities of 250 devices per reel.

(2) This product is RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and is suitable for use in specified lead-free soldering processes. In addition, this product uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

ABSOLUTE MAXIMUM RATINGS(1)

over the -40°C to 125°C operating free-air temperature range (unless otherwise noted)

			VALUE		UNIT
			MIN	MAX	
V_I	Input Voltage	IN (with respect to VSS)	–0.3	28	V
		BAT (with respect to VSS)	–0.3	5	V
		OUT, EN1, EN2, $\overline{CE}$, TS, ISET, $\overline{PGOOD}$, $\overline{CHG}$, ILIM, TMR, SYSOFF	–0.3	7	V
I_I	Input Current	IN		1.6	A
I_O	Output Current (Continuous)	OUT		5	A
		BAT (Discharge mode)		5	A
		BAT (Charging mode)		1.5(2)	A
	Output Sink Current	$\overline{CHG}$, $\overline{PGOOD}$		15	mA
Electrostatic Discharge (HBM) QSS 009-105 (JESD22-A114A)(3)				1.5	kV
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C
ESD Rating	Human Body Model (HBM) AEC-Q100 Classification Level H2			2	kV
	Charged Device Model (CDM) AEC-Q100 Classification Level C3B			750	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

(2) The IC operational charging life is reduced to 20,000 hours, when charging at 1.5A and 125°C. The thermal regulation feature reduces charge current if the IC's junction temperature reaches 125°C; thus without a good thermal design the maximum programmed charge current may not be reached.

(3) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

THERMAL INFORMATION

THERMAL METRIC(1)		BQ24075-Q1 RGT 16-PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	45.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	53.6	
θ_{JB}	Junction-to-board thermal resistance	18.1	
ψ_{JT}	Junction-to-top characterization parameter	1.1	
ψ_{JB}	Junction-to-board characterization parameter	18.0	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	5.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_I	IN voltage range	4.35	26	V
	IN operating voltage range	4.35	6.4	V
I_{IN}	Input current, IN pin		1.5	A
I_{OUT}	Current, OUT pin		4.5	A
I_{BAT}	Current, BAT pin (Discharging)		4.5	A
I_{CHG}	Current, BAT pin (Charging)		1.5(1)	A
R_{ILIM}	Maximum input current programming resistor	1100	8000	Ω
R_{ISET}	Fast-charge current programming resistor (2)	590	3000	Ω
R_{ITERM}	Termination current programming resistor	0	15	kΩ
R_{TMR}	Timer programming resistor	18	72	kΩ

(1) The IC operational charging life is reduced to 20,000 hours, when charging at 1.5A and 125°C. The thermal regulation feature reduces charge current if the IC's junction temperature reaches 125°C; thus without a good thermal design the maximum programmed charge current may not be reached.
(2) Use a 1% tolerance resistor for R_{ISET} to avoid issues with the R_{ISET} short test when using the maximum charge current setting.

ELECTRICAL CHARACTERISTICS

Over ambient temperature range (-40C° ≤ T_A ≤ 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
UVLO	Undervoltage lock-out	V_{IN}: 0 V → 4 V	3.2	3.3	3.4	V
V_{hys}	Hysteresis on UVLO	V_{IN}: 4 V → 0 V	200		300	mV
$V_{IN(DT)}$	Input power detection threshold	Input power detected when $V_{IN} > V_{BAT} + V_{IN(DT)}$ V_{BAT} = 3.6 V, VIN: 3.5 V → 4 V	50	80	135	mV
V_{hys}	Hysteresis on $V_{IN(DT)}$	V_{BAT} = 3.6 V, V_{IN}: 4 V → 3.5 V	20			mV
$t_{DGL(PGOOD)}$	Deglitch time, input power detected status	Time measured from V_{IN}: 0 V → 5 V 1 µs rise-time to $\overline{PGOOD}$ = LO		1.2		ms
V_{OVP}	Input overvoltage protection threshold	V_{IN}: 5 V → 7 V	6.4	6.6	6.8	V
V_{hys}	Hysteresis on OVP	V_{IN}: 7 V → 5V		110		mV
$t_{DGL(OVP)}$	Input overvoltage blanking time (OVP fault deglitch)			50		µs
t_{REC}	Input overvoltage recovery time	Time measured from V_{IN}: 11 V → 5 V with 1 µs fall-time to $\overline{PGOOD}$ = LO		1.2		ms
ILIM, ISET SHORT CIRCUIT DETECTION (CHECKED DURING STARTUP)						
I_{SC}	Current source	V_{IN} > UVLO and $V_{IN} > V_{BAT} + V_{IN(DT)}$		1.3		mA
V_{SC}		V_{IN} > UVLO and $V_{IN} > V_{BAT} + V_{IN(DT)}$		520		mV
QUIESCENT CURRENT						
$I_{BAT(PDWN)}$	Sleep current into BAT pin	$\overline{CE}$ = LO or HI, input power not detected, No load on OUT pin, T_a = 125°C			12	µA
I_{IN}	Standby current into IN pin	EN1= HI, EN2=HI, V_{IN} = 6 V, T_a= 125°C			65	µA
		EN1= HI, EN2=HI, V_{IN} = 10 V, T_a= 125°C			200	
I_{CC}	Active supply current, IN pin	$\overline{CE}$ = LO, V_{IN} = 6 V, no load on OUT pin, $V_{BAT} > V_{BAT(REG)}$, (EN1, EN2) ≠ (HI, HI)			1.5	mA
POWER PATH						
$V_{DO(IN-OUT)}$	$V_{IN} - V_{OUT}$	V_{IN} = 4.3 V, I_{IN} = 1A, V_{BAT} = 4.2V		300	475	mV
$V_{DO(BAT-OUT)}$	$V_{BAT} - V_{OUT}$	I_{OUT} = 1 A, V_{IN} = 0 V, V_{BAT} > 3 V		50	100	mV
$V_{O(REG)}$	OUT pin voltage regulation	$V_{IN} > V_{OUT} + V_{DO(IN-OUT)}$	5.4	5.5	5.65	V
I_{IN}max	Maximum input current	EN1 = LO, EN2 = LO	85	95	100	mA
		EN1 = HI, EN2 = LO	440	475	500	
		EN2 = HI, EN1 = LO		K_{ILIM}/R_{ILIM}		A
K_{ILIM}	Maximum input current factor	I_{LIM} = 500mA to 1.5A	1500	1610	1720	AΩ
		I_{LIM} = 200mA to 500mA	1300	1525	1770	
I_{IN}max	Programmable input current limit range	EN2 = HI, EN1 = LO, R_{ILIM} = 8 kΩ to 1.1 kΩ	200		1500	mA
V_{IN-DPM}	Input voltage threshold when input current is reduced	EN2 = LO, EN1 = X	4.35	4.5	4.63	V
V_{DPPM}	Output voltage threshold when charging current is reduced		4.2	4.3	4.4	V
V_{BSUP1}	Enter battery supplement mode	V_{BAT} = 3.6V, R_{ILIM} = 1.5kΩ, R_{LOAD} = 10Ω → 2Ω		$V_{OUT} \le V_{BAT}$ –40mV		V
V_{BSUP2}	Exit battery supplement mode	V_{BAT} = 3.6V, R_{ILIM} = 1.5kΩ, R_{LOAD} = 2Ω → 10Ω		$V_{OUT} \ge V_{BAT}$–20mV		V
$V_{O(SC1)}$	Output short-circuit detection threshold, power-on	$V_{IN} > V_{UVLO}$ and $V_{IN} > V_{BAT} + V_{IN(DT)}$	0.8	0.9	1	V
$V_{O(SC2)}$	Output short-circuit detection threshold, supplement mode $V_{BAT} - V_{OUT} > V_{O(SC2)}$ indicates short-circuit	$V_{IN} > V_{UVLO}$ and $V_{IN} > V_{BAT} + V_{IN(DT)}$	200	250	300	mV
$t_{DGL(SC2)}$	Deglitch time, supplement mode short circuit			250		µs
$t_{REC(SC2)}$	Recovery time, supplement mode short circuit			60		ms

ELECTRICAL CHARACTERISTICS (continued)

Over ambient temperature range (-40C° ≤ T_A ≤ 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY CHARGER						
I_{BAT}	Source current for BAT pin short-circuit detection	V_{BAT} = 1.5V	4	7.5	11	mA
$V_{BAT(SC)}$	BAT pin short-circuit detection threshold	V_{BAT} rising	1.6	1.8	2	V
$V_{BAT(REG)}$	Battery charge voltage		4.15	4.20	4.23	V
V_{LOWV}	Pre-charge to fast-charge transition threshold	V_{IN} > V_{UVLO} and V_{IN} > V_{BAT} + $V_{IN(DT)}$	2.9	3	3.1	V
$t_{DGL1(LOWV)}$	Deglitch time on pre-charge to fast-charge transition			25		ms
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to pre-charge transition			25		ms
I_{CHG}	Battery fast charge current range	$V_{BAT(REG)}$ > V_{BAT} > V_{LOWV}, V_{IN} = 5 V $\overline{CE}$ = LO, EN1 = LO, EN2 = HI	300		1500	mA
	Battery fast charge current	$\overline{CE}$ = LO, EN1= LO, EN2 = HI, V_{BAT} > V_{LOWV}, V_{IN} = 5 V, I_{IN}max > I_{CHG}, no load on OUT pin, thermal loop and DPPM loop not active	K_{ISET}/R_{ISET}			A
K_{ISET}	Fast charge current factor		797	890	975	AΩ
I_{PRECHG}	Pre-charge current		K_{PRECHG}/R_{ISET}			A
K_{PRECHG}	Pre-charge current factor		55	88	110	AΩ
I_{TERM}	Termination comparator detection threshold (internally set)	$\overline{CE}$ = LO, (EN1, EN2) ≠ (LO, LO), V_{BAT} > V_{RCH}, t < t_{MAXCH}, V_{IN} = 5 V, DPPM loop and thermal loop not active	0.09×I_{CHG}	0.1×I_{CHG}	0.11×I_{CHG}	A
		$\overline{CE}$ = LO, (EN1, EN2) = (LO, LO), V_{BAT} > V_{RCH}, t < t_{MAXCH}, V_{IN} = 5 V, DPPM loop and thermal loop not active	0.027×I_{CHG}	0.033×I_{CHG}	0.040×I_{CHG}	
$t_{DGL(TERM)}$	Deglitch time, termination detected			25		ms
V_{RCH}	Recharge detection threshold	V_{IN} > V_{UVLO} and V_{IN} > V_{BAT} + $V_{IN(DT)}$	$V_{BAT(REG)}$ –140mV	$V_{BAT(REG)}$ –100mV	$V_{BAT(REG)}$ –55mV	V
$t_{DGL(RCH)}$	Deglitch time, recharge threshold detected			62.5		ms
$t_{DGL(NO-IN)}$	Delay time, input power loss to OUT LDO turn-off	V_{BAT} = 3.6 V. Time measured from V_{IN}: 5 V → 3 V 1 µs fall-time		20		ms
$I_{BAT(DET)}$	Sink current for battery detection	V_{BAT} = 2.5V	5	7.5	10	mA
t_{DET}	Battery detection timer	BAT high or low		250		ms
BATTERY CHARGING TIMERS						
t_{PRECHG}	Pre-charge safety timer value	TMR = floating	1440	1800	2160	s
t_{MAXCHG}	Charge safety timer value	TMR = floating	14400	18000	21600	s
t_{PRECHG}	Pre-charge safety timer value	18 kΩ < R_{TMR} < 72 kΩ	R_{TMR} × K_{TMR}			s
t_{MAXCHG}	Charge safety timer value	18 kΩ < R_{TMR} < 72 kΩ	10×R_{TMR} ×K_{TMR}			s
K_{TMR}	Timer factor		36	48	60	s/kΩ
BATTERY-PACK NTC MONITOR(1)						
I_{NTC}	NTC bias current	V_{IN} > UVLO and V_{IN} > V_{BAT} + $V_{IN(DT)}$	72	75	80	µA
V_{HOT}	High temperature trip point	Battery charging, V_{TS} Falling	270	300	330	mV
$V_{HYS(HOT)}$	Hysteresis on high trip point	Battery charging, V_{TS} Rising from V_{HOT}		30		mV
V_{COLD}	Low temperature trip point	Battery charging, V_{TS} Rising	2000	2100	2200	mV
$V_{HYS(COLD)}$	Hysteresis on low trip point	Battery charging, V_{TS} Falling from V_{COLD}		300		mV
$t_{DGL(TS)}$	Deglitch time, pack temperature fault detection	TS fault detected to charger disable		50		ms
THERMAL REGULATION						
$T_{J(REG)}$	Temperature regulation limit			125		°C
$T_{J(OFF)}$	Thermal shutdown temperature	T_J Rising		155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C

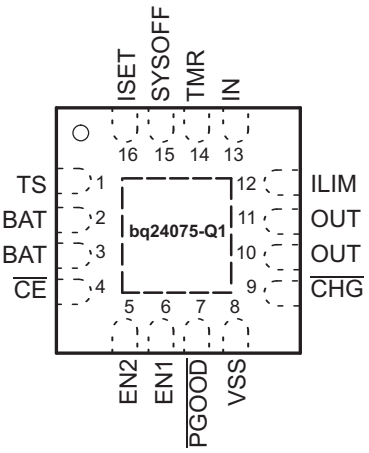
(1) These numbers set trip points of 0°C and 50°C while charging, with 3°C hysteresis on the trip points, with a Vishay Type 2 curve NTC with an R25 of 10 kΩ.

ELECTRICAL CHARACTERISTICS (continued)

Over ambient temperature range (-40C° ≤ T_A ≤ 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC LEVELS ON EN1, EN2, $\overline{CE}$, SYSOFF						
V_{IL}	Logic LOW input voltage		0		0.4	V
V_{IH}	Logic HIGH input voltage		1.4		6	V
I_{IL}	Input sink current	V_{IL}= 0V			1	µA
I_{IH}	Input source current	V_{IH}= 1.4V			10	µA
LOGIC LEVELS ON $\overline{PGOOD}$, $\overline{CHG}$						
V_{OL}	Output LOW voltage	I_{SINK} = 5 mA			0.4	V

RGT PACKAGE
(Top View)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
TS	1	I	External NTC Thermistor Input. Connect the TS input to the NTC thermistor in the battery pack. TS monitors a 10kΩ NTC thermistor. For applications that do not utilize the TS function, connect a 10kΩ fixed resistor from TS to VSS to maintain a valid voltage level on TS.
BAT	2, 3	I/O	Charger Power Stage Output and Battery Voltage Sense Input. Connect BAT to the positive terminal of the battery. Bypass BAT to VSS with a 4.7 µF to 47 µF ceramic capacitor.
$\overline{CE}$	4	I	Charge Enable Active-Low Input. Connect $\overline{CE}$ to a high logic level to place the battery charger in standby mode. In standby mode, OUT is active and battery supplement mode is still available. Connect $\overline{CE}$ to a low logic level to enable the battery charger. $\overline{CE}$ is internally pulled down with ~285 kΩ. Do not leave $\overline{CE}$ unconnected to ensure proper operation.
EN2	5	I	Input Current Limit Configuration Inputs. Use EN1 and EN2 control the maximum input current and enable USB compliance. See Table 2 for the description of the operation states. EN1 and EN2 are internally pulled down with ≠285 kΩ. Do not leave EN1 or EN2 unconnected to ensure proper operation.
EN1	6	I	
$\overline{PGOOD}$	7	O	Open-drain Power Good Status Indication Output. $\overline{PGOOD}$ pulls to VSS when a valid input source is detected. $\overline{PGOOD}$ is high-impedance when the input power is not within specified limits. Connect $\overline{PGOOD}$ to the desired logic voltage rail using a 1kΩ-100kΩ resistor, or use with an LED for visual indication.
VSS	8	–	Ground. Connect to the thermal pad and to the ground rail of the circuit.
$\overline{CHG}$	9	O	Open-Drain Charging Status Indication Output. $\overline{CHG}$ pulls to VSS when the battery is charging. $\overline{CHG}$ is high impedance when charging is complete and when charger is disabled. Connect $\overline{CHG}$ to the desired logic voltage rail using a 1kΩ-100kΩ resistor, or use with an LED for visual indication.
OUT	10, 11	O	System Supply Output. OUT provides a regulated output when the input is below the OVP threshold and above the regulation voltage. When the input is out of the operation range, OUT is connected to V_{BAT} except when SYSOFF is high. Connect OUT to the system load. Bypass OUT to VSS with a 4.7 µF to 47 µF ceramic capacitor.
ILIM	12	I	Adjustable Current Limit Programming Input. Connect a 1100 Ω to 8 kΩ resistor from ILIM to VSS to program the maximum input current (EN2=1, EN1=0). The input current includes the system load and the battery charge current. Leaving ILIM unconnected disables all charging.

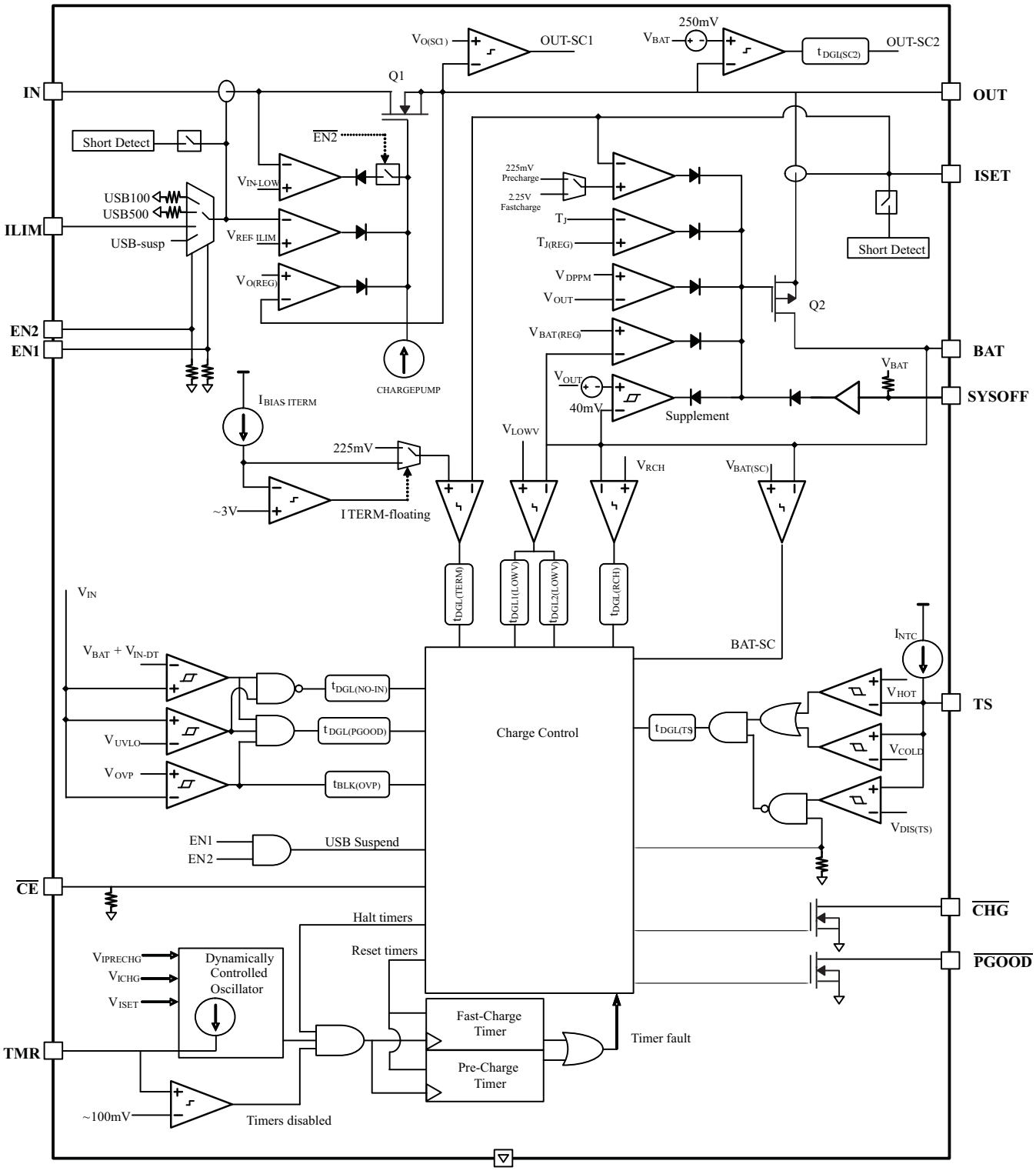
PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
IN	13	I	Input Power Connection. Connect IN to the external DC supply (AC adapter or USB port). The input operating range is 4.35V to 6.6V . The input can accept voltages up to 26V without damage but operation is suspended. Connect bypass capacitor 1 µF to 10 µF to VSS.
TMR	14	I	Timer Programming Input. TMR controls the pre-charge and fast-charge safety timers. Connect TMR to VSS to disable all safety timers. Connect a 18 kΩ to 72 kΩ resistor between TMR and VSS to program the timers a desired length. Leave TMR unconnected to set the timers to the default values.
SYSOFF	15	I	System Enable Input. Connect SYSOFF high to turn off the FET connecting the battery to the system output. When an adapter is connected, charging is also disabled. Connect SYSOFF low for normal operation. SYSOFF is internally pulled up to V_{BAT} through a large resistor (~5 MΩ). Do not leave SYSOFF unconnected to ensure proper operation.
ISET	16	I/O	Fast Charge Current Programming Input. Connect a 590 Ω to 3 kΩ resistor from ISET to VSS to program the fast charge current level. Charging is disabled if ISET is left unconnected. While charging, the voltage at ISET reflects the actual charging current and can be used to monitor charge current. See the CHARGE CURRENT TRANSLATOR section for more details.
Thermal Pad		–	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

Table 1. EN1/EN2 Settings

EN2	EN1	Maximum input current into IN pin
0	0	100 mA. USB100 mode
0	1	500 mA. USB500 mode
1	0	Set by an external resistor from ILIM to VSS
1	1	Standby (USB suspend mode)

SIMPLIFIED BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

V_{IN} = 6V, EN1=1, EN2=0, T_A = 25°C, unless otherwise noted.

ADAPTER PLUG-IN BATTERY CONNECTED R_{LOAD} = 10Ω

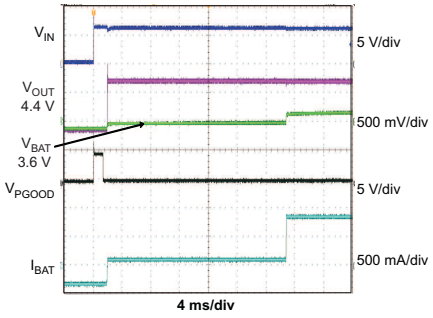


Figure 1.

BATTERY DETECTION BATTERY INSERTED

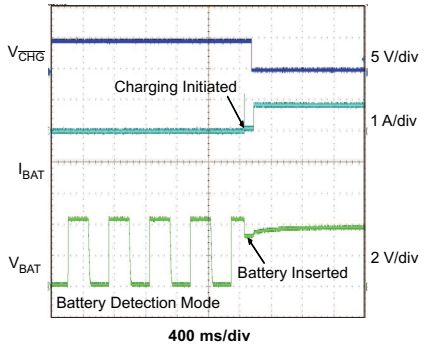


Figure 2.

BATTERY DETECTION BATTERY REMOVED

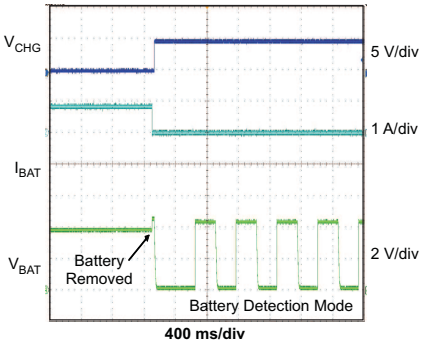


Figure 3.

ENTERING AND EXITING DPPM MODE R_{LOAD} = 20Ω to 9Ω

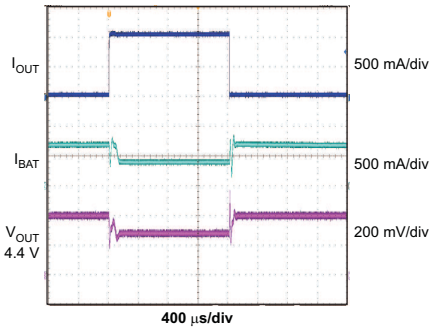


Figure 4.

CHARGER ON/OF USING $\overline{CE}$

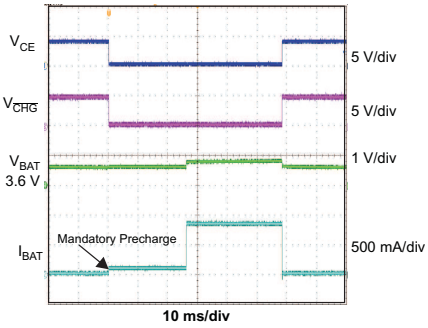


Figure 5.

OVP FAULT V_{IN} = 6V to 15V R_{LOAD} = 10Ω

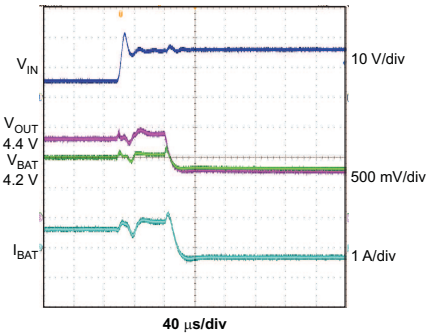


Figure 6.

SYSTEM ON/OFF WITH INPUT CONNECTED V_{IN} = 6V bq24075

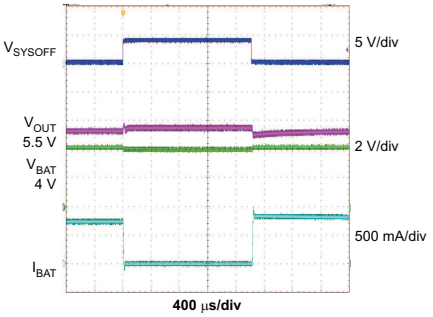


Figure 7.

SYSTEM ON/OFF WITH INPUT NOT CONNECTED V_{IN} = 0V bq24075

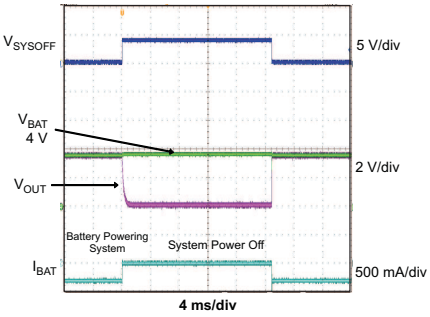


Figure 8.

THERMAL REGULATION

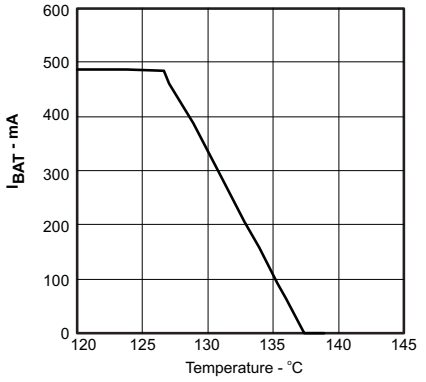


Figure 9.

TYPICAL CHARACTERISTICS (continued)

V_{IN} = 6V, EN1=1, EN2=0, T_A = 25°C, unless otherwise noted.

DROPOUT VOLTAGE vs TEMPERATURE

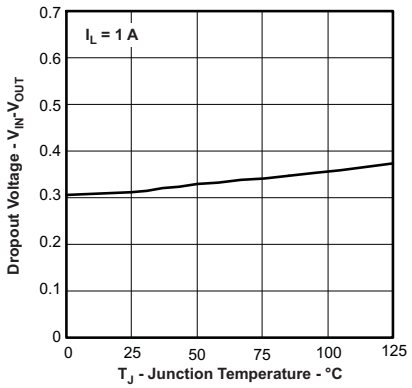


Figure 10.

DROPOUT VOLTAGE vs TEMPERATURE NO INPUT SUPPLY

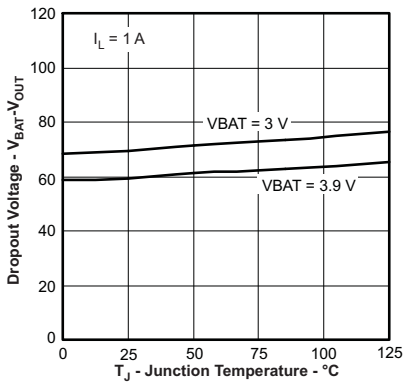


Figure 11.

bq24075 OUTPUT REGULATION VOLTAGE vs TEMPERATURE

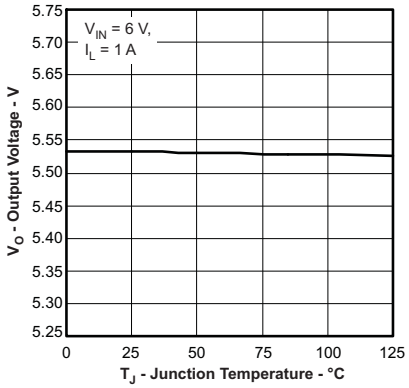


Figure 12.

BAT REGULATION VOLTAGE vs TEMPERATURE

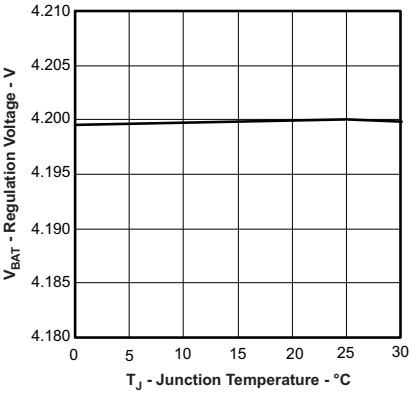


Figure 13.

OVERVOLTAGE PROTECTION THRESHOLD vs TEMPERATURE

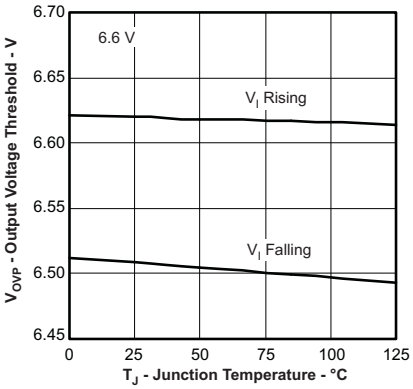


Figure 14.

FASTCHARGE CURRENT vs BATTERY VOLTAGE

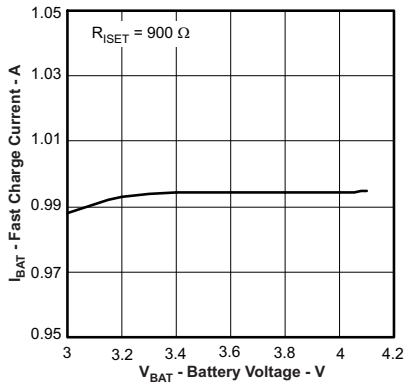


Figure 15.

TYPICAL CHARACTERISTICS (continued)

V_{IN} = 6V, EN1=1, EN2=0, T_A = 25°C, unless otherwise noted.

FASTCHARGE CURRENT vs BATTERY VOLTAGE

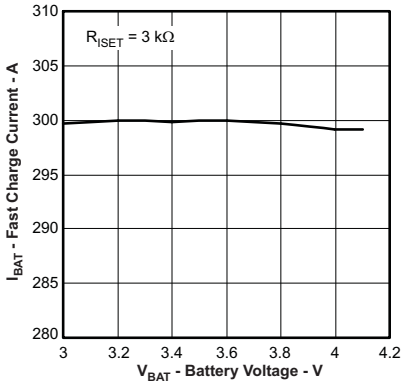


Figure 16.

PRECHARGE CURRENT vs BATTERY VOLTAGE

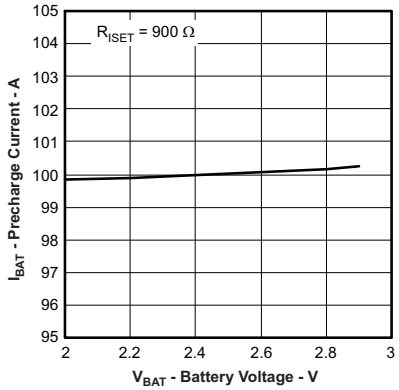


Figure 17.

PRECHARGE CURRENT vs BATTERY VOLTAGE

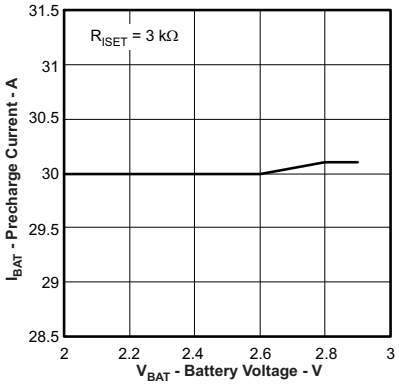


Figure 18.

APPLICATION CIRCUITS

V_{IN} = UVLO to V_{OVP}, $I_{FASTCHG}$ = 800mA, $I_{IN(MAX)}$ = 1.3A, Battery Temperature Charge Range = 0°C to 50°C, 6.25 hour Fastcharge Safety Timer

V_{IN} = UVLO to V_{OVP}, $I_{FASTCHG}$ = 800mA, $I_{IN(MAX)}$ = 1.3A, I_{TERM} = 110mA, Battery Temperature Charge Range = 0°C to 50°C, Safety Timers disabled

V_{IN} = UVLO to V_{OVP}, $I_{FASTCHG}$ = 800mA, $I_{IN(MAX)}$ = 1.3A, Battery Temperature Charge Range = 0°C to 50°C, 6.25 hour Fastcharge Safety Timer

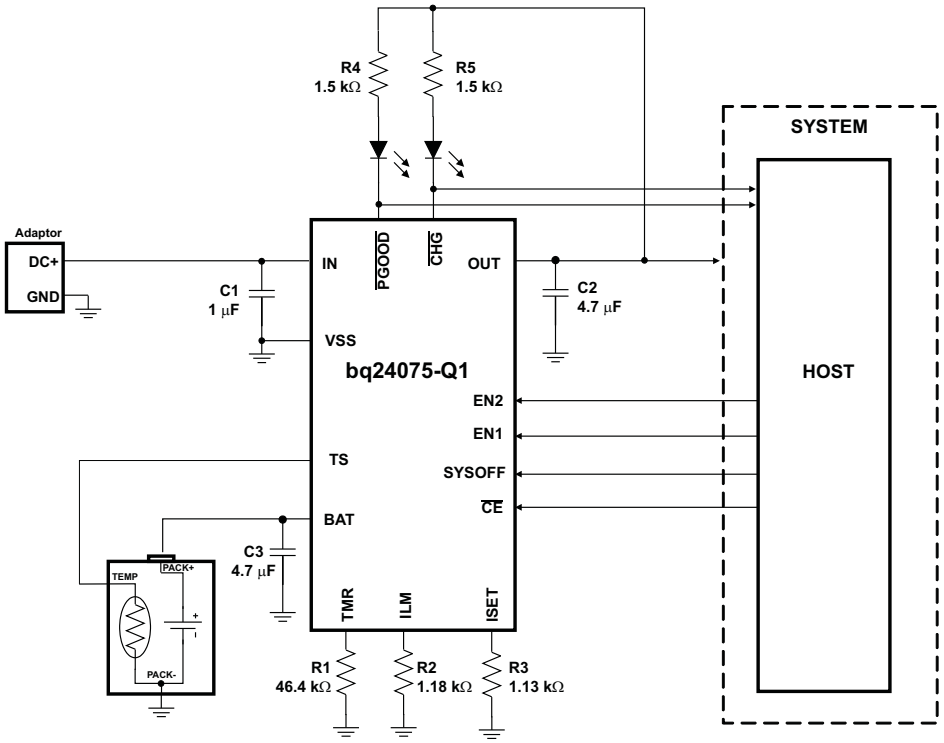


Figure 19. Using bq24075 to Disconnect the Battery from the System

EXPLANATION OF DEGLITCH TIMES AND COMPARATOR HYSTERESIS

Figures not to scale

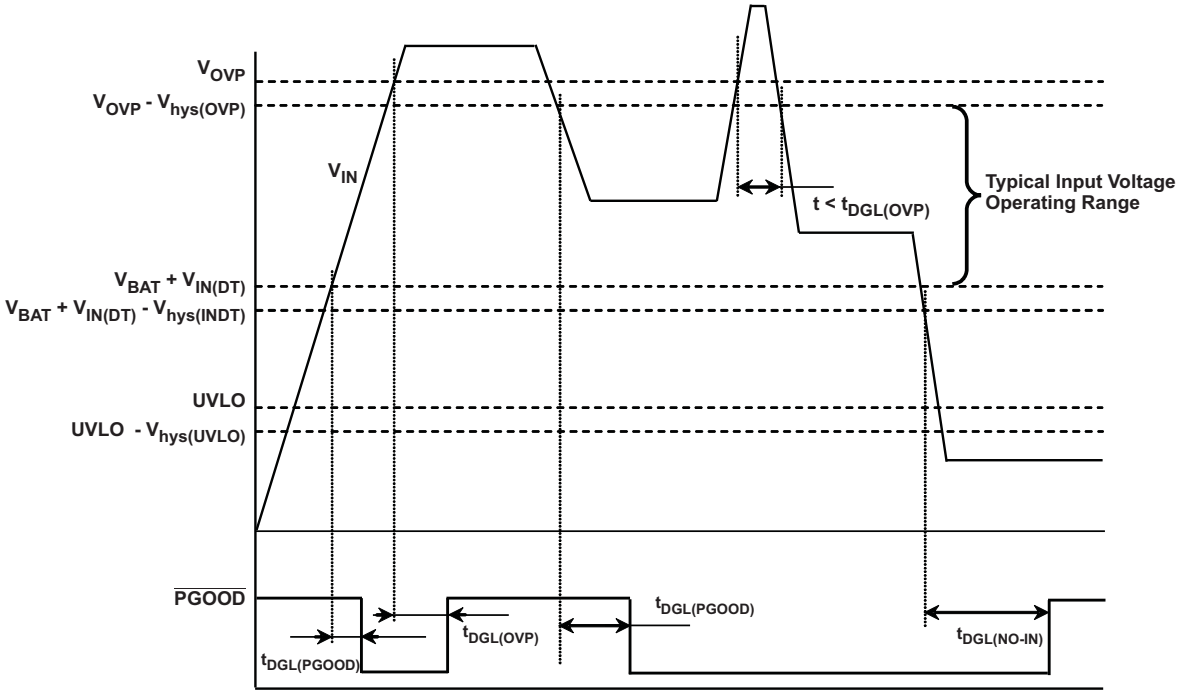


Figure 20. Power-Up, Power-Down, Power Good Indication

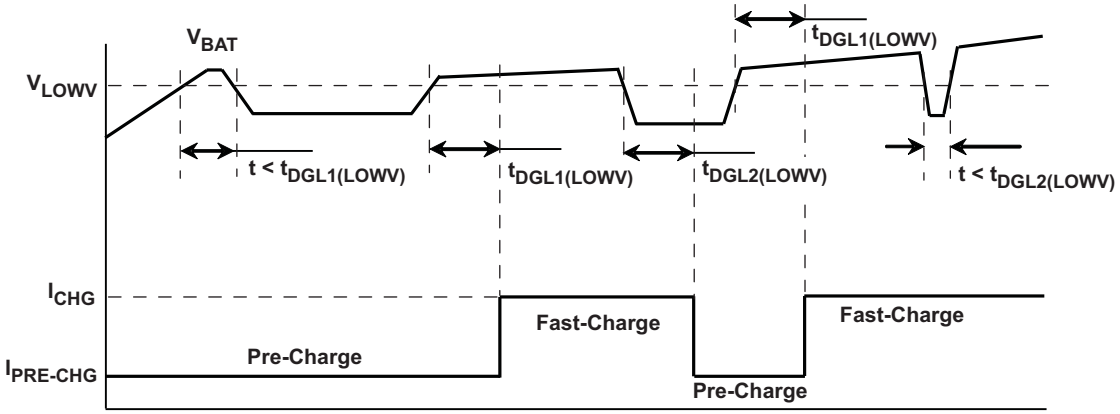


Figure 21. Pre- to Fast-Charge, Fast- to Pre-Charge Transition – $t_{DGL1(LOWV)}$, $t_{DGL2(LOWV)}$

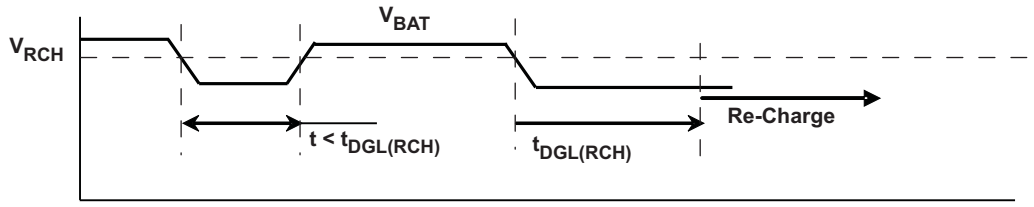


Figure 22. Recharge – $t_{DGL(RCH)}$

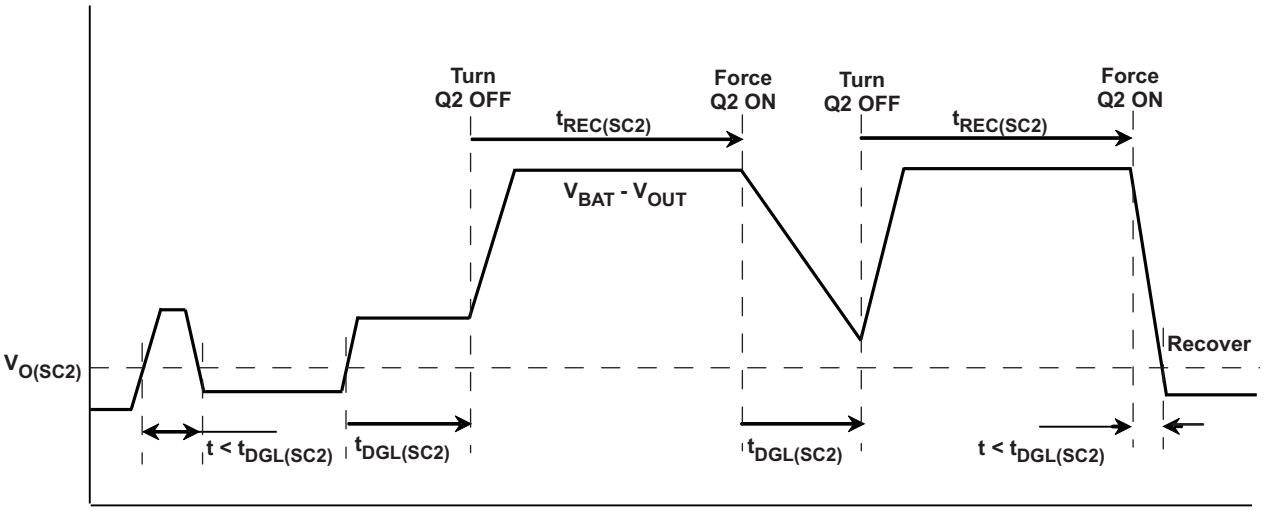


Figure 23. OUT Short-Circuit – Supplement Mode

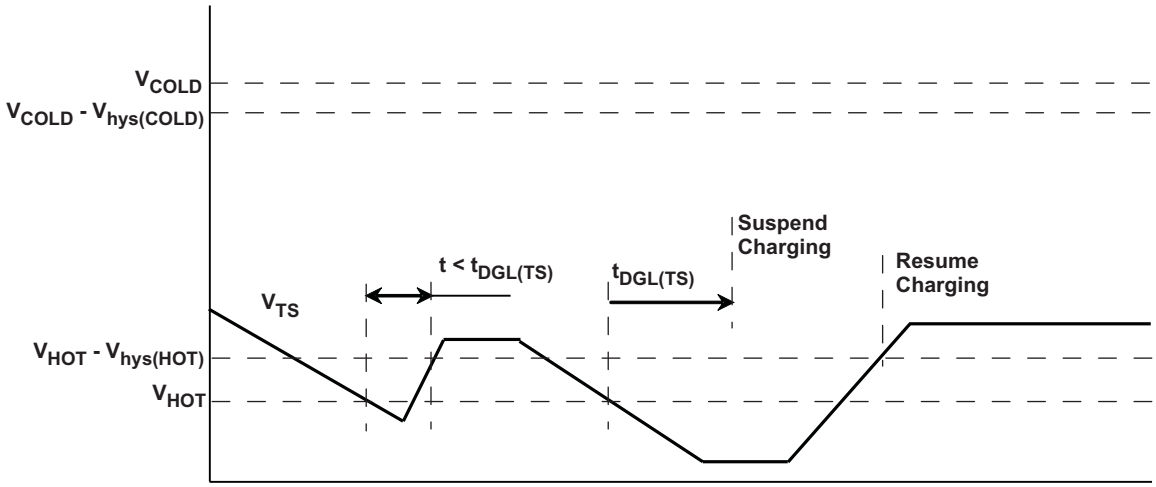


Figure 24. Battery Pack Temperature Sensing – TS Pin. Battery Temperature Increasing

DETAILED FUNCTIONAL DESCRIPTION

The bq24075-Q1 device is integrated Li-Ion linear charger and system power path management device targeted at space-limited portable applications. The device powers the system while simultaneously and independently charging the battery. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination and enables the system to run with a defective or absent battery pack. It also allows instant system turn-on even with a totally discharged battery. The input power source for charging the battery and running the system can be an AC adapter or a USB port. The device features Dynamic Power Path Management (DPPM), which shares the source current between the system and battery charging, and automatically reduces the charging current if the system load increases. When charging from a USB port, the input dynamic power management (V_{IN}-DPM) circuit reduces the input current if the input voltage falls below a threshold, preventing the USB port from crashing. The power-path architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents.

UNDERVOLTAGE LOCKOUT (UVLO)

The bq24075-Q1 family remains in power down mode when the input voltage at the IN pin is below the undervoltage threshold (UVLO).

During the power down mode the host commands at the control inputs ($\overline{CE}$, EN1 and EN2) are ignored. The Q1 FET connected between IN and OUT pins is off, and the status outputs $\overline{CHG}$ and $\overline{PGOOD}$ are high impedance. The Q2 FET that connects BAT to OUT is ON. (If SYSOFF is high, Q2 is off). During power down mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

POWER ON

When V_{IN} exceeds the UVLO threshold, the bq24075-Q1 powers up. While V_{IN} is below V_{BAT} + $V_{IN(DT)}$, the host commands at the control inputs ($\overline{CE}$, EN1 and EN2) are ignored. The Q1 FET connected between IN and OUT pins is off, and the status outputs $\overline{CHG}$ and $\overline{PGOOD}$ are high impedance. The Q2 FET that connects BAT to OUT is ON. (If SYSOFF is high, Q2 is off). During this mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

Once V_{IN} rises above V_{BAT} + $V_{IN(DT)}$, $\overline{PGOOD}$ is driven low to indicate the valid power status and the $\overline{CE}$, EN1, and EN2 inputs are read. The device enters standby mode if (EN1 = EN2 = HI) or if an input overvoltage condition occurs. In standby mode, Q1 is OFF and Q2 is ON so OUT is connected to the battery input. (If SYSOFF is high, FET Q2 is off). During this mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

When the input voltage at IN is within the valid range: V_{IN} > UVLO ***AND*** V_{IN} > V_{BAT} + $V_{IN(DT)}$ ***AND*** V_{IN} < V_{OVP}, and the EN1 and EN2 pins indicate that the USB suspend mode is not enabled [($\overline{EN1}$, EN2) ≠ (HI, HI)] all internal timers and other circuit blocks are activated. The device then checks for short-circuits at the ISET and ILIM pins. If no short conditions exists, the device switches on the input FET Q1 with a 100mA current limit to checks for a short circuit at OUT. When V_{OUT} is above V_{SC}, the FET Q1 switches to the current limit threshold set by EN1, EN2 and R_{ILIM} and the device enters into the normal operation. During normal operation, the system is powered by the input source (Q1 is regulating), and the device continuously monitors the status of $\overline{CE}$, EN1 and EN2 as well as the input voltage conditions.

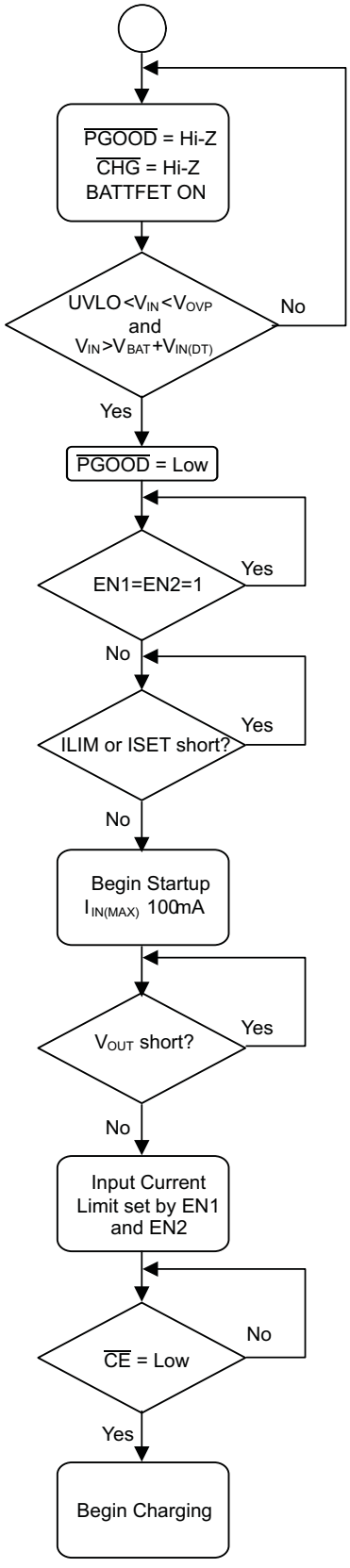


Figure 25. Startup Flow Diagram

OVERVOLTAGE PROTECTION (OVP)

The bq24075-Q1 accepts inputs up to 28V without damage. Additionally, an overvoltage protection (OVP) circuit is implemented that shuts off the internal LDO and discontinues charging when $V_{IN} > V_{OVP}$ for a period long than $t_{DGL(OVP)}$. When in OVP, the system output (OUT) is connected to the battery and PGOOD is high impedance. Once the OVP condition is removed, a new power on sequence starts (See the POWER ON section). The safety timers are reset and a new charge cycle will be indicated by the CHG output.

DYNAMIC POWER-PATH MANAGEMENT

The bq24075-Q1 features an OUT output that powers the external load connected to the battery. This output is active whenever a source is connected to IN or BAT. The following sections discuss the behavior of OUT with a source connected to IN to charge the battery and a battery source only.

INPUT SOURCE CONNECTED (ADAPTER or USB)

With a source connected, the dynamic power-path management (DPPM) circuitry of the bq24075-Q1 monitors the input current continuously. The OUT output for the bq24075-Q1 is regulated to a fixed voltage ($V_{O(REG)}$). The current into IN is shared between charging the battery and powering the system load at OUT. The bq24075-Q1 has internal selectable current limits of 100mA (USB100) and 500mA (USB500) for charging from USB ports, as well as a resistor-programmable input current limit.

The bq24075-Q1 is USB IF compliant for the inrush current testing. The USB spec allows up to 10µF to be hard started, which establishes 50µC as the maximum inrush charge value when exceeding 100mA. The input current limit for the bq24075-Q1 prevents the input current from exceeding this limit, even with system capacitances greater than 10µF. Note that the input capacitance to the device must be selected small enough to prevent a violation (<10µF), as this current is not limited. Figure 26 demonstrates the startup of the bq24075-Q1 and compares it to the USB-IF specification.

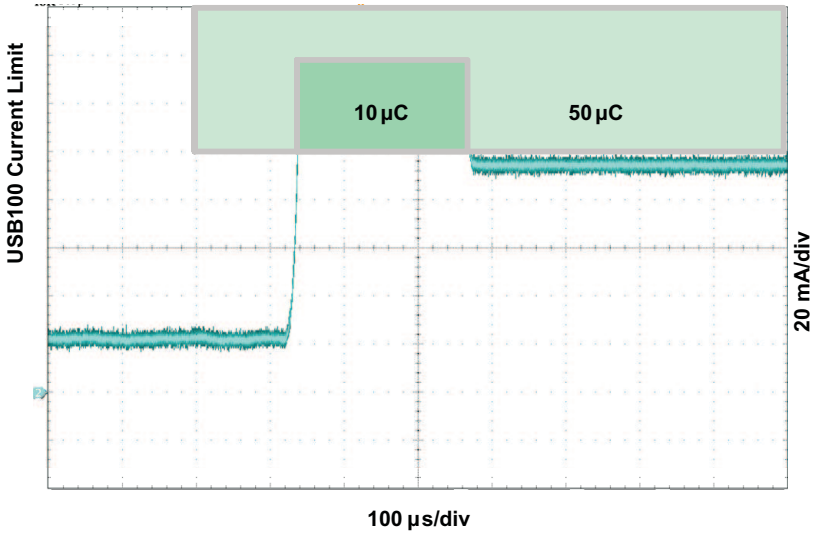


Figure 26. USB-IF Inrush Current Test

The input current limit selection is controlled by the state of the EN1 and EN2 pins as shown in Table 1. When using the resistor-programmable current limit, the input current limit is set by the value of the resistor connected from the ILIM pin to VSS, and is given by the equation:

$$I_{IN\text{-}MAX} = K_{ILIM}/R_{ILIM} \quad (1)$$

The input current limit is adjustable up to 1.5A. The valid resistor range is 1.1 kΩ to 8 kΩ.

When the IN source is connected, priority is given to the system load. The DPPM and Battery Supplement modes are used to maintain the system load. These modes are explained in detail in the following sections.

Input DPM Mode (V_{IN}-DPM)

The bq24075-Q1 uses the V_{IN}-DPM mode for operation from current-limited USB ports. When EN1 and EN2 are configured for USB100 (EN2=0, EN1=0) or USB500 (EN2=0, EN2=1) modes, the input voltage is monitored. If V_{IN} falls to V_{IN-DPM}, the input current limit is reduced to prevent the input voltage from falling further. This prevents the bq24075-Q1 from crashing poorly designed or incorrectly configured USB sources. Figure 27 shows the V_{IN}-DPM behavior to a current limited source. In this figure, the input source has a 400mA current limit and the device is in USB500 mode (EN1=1, EN2=0).

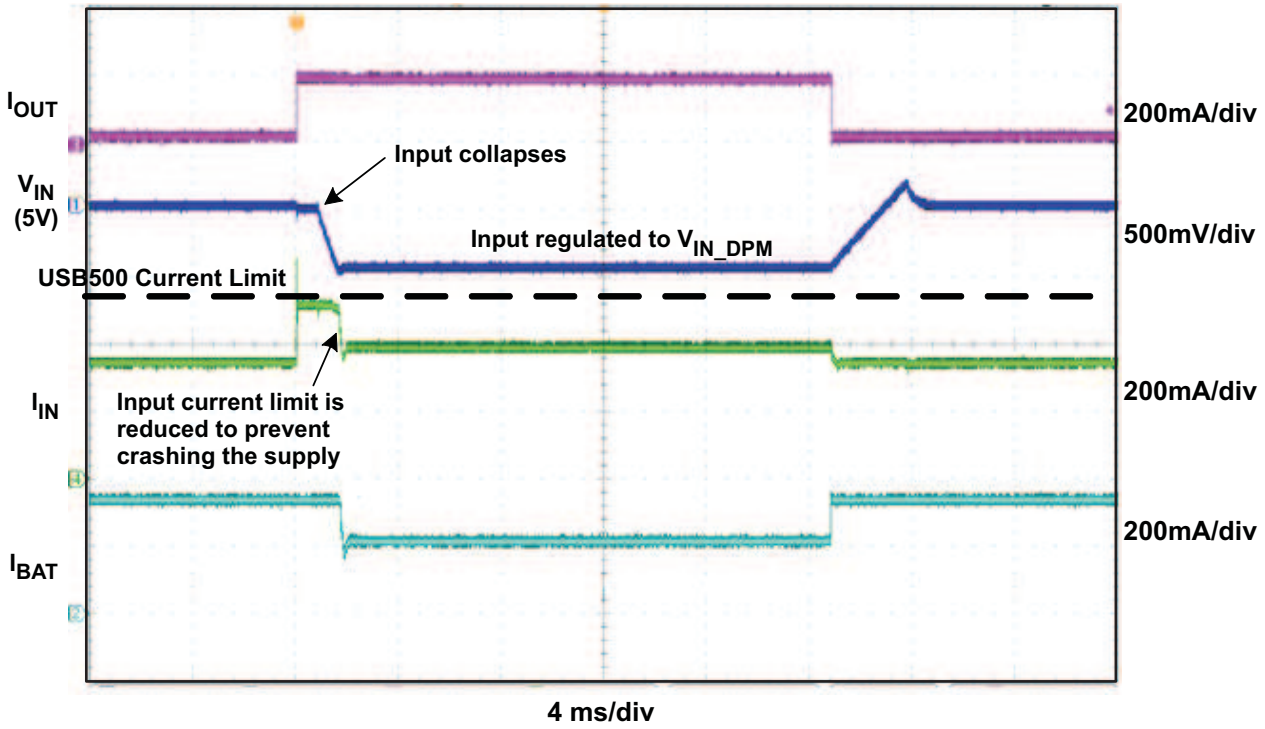


Figure 27. V_{IN}-DPM Waveform

DPPM Mode

When the sum of the charging and system load currents exceeds the maximum input current (programmed with EN1, EN2 and ILIM pins), the voltage at OUT decreases. Once the voltage on the OUT pin falls to V_{DPPM}, the bq24075-Q1 enters DPPM mode. In this mode, the charging current is reduced as the OUT current increases in order to maintain the system output. Battery termination is disabled while in DPPM mode.

Battery Supplement Mode

While in DPPM mode, if the charging current falls to zero and the system load current increases beyond the programmed input current limit, the voltage at OUT reduces further. When the OUT voltage drops below the V_{BSUP1} threshold, the battery supplements the system load. The battery stops supplementing the system load when the voltage at OUT rises above the V_{BSUP2} threshold.

During supplement mode, the battery supplement current is not regulated (BAT-FET is fully on), however there is a short circuit protection circuit built in. If during battery supplement mode, the voltage at OUT drops $V_{O(SC2)}$ below the BAT voltage, the OUT output is turned off if the overload exists after $t_{DGL(SC2)}$. The short circuit recovery timer then starts counting. After $t_{REC(SC2)}$, OUT turns on and attempts to restart. If the short circuit remains, OUT is turned off and the counter restarts. Battery termination is disabled while in supplement mode.

INPUT SOURCE NOT CONNECTED

When no source is connected to the IN input, OUT is powered strictly from the battery. During this mode the current into OUT is not regulated, similar to *Battery Supplement Mode*, however the short circuit circuitry is active. If the OUT voltage falls below the BAT voltage by 250mV for longer than $t_{DGL(SC2)}$, OUT is turned off. The short circuit recovery timer then starts counting. After $t_{REC(SC2)}$, OUT turns on and attempts to restart. If the short circuit remains, OUT is turned off and the counter restarts. This ON/OFF cycle continues until the overload condition is removed.

BATTERY CHARGING

Set $\overline{CE}$ low to initiate battery charging. First, the device checks for a short-circuit on the BAT pin by sourcing $I_{BAT(SC)}$ to the battery and monitoring the voltage. When the BAT voltage exceeds $V_{BAT(SC)}$, the battery charging continues. The battery is charged in three phases: conditioning pre-charge, constant current fast charge (current regulation) and a constant voltage tapering (voltage regulation). In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

Figure 28 illustrates a normal Li-Ion charge cycle using the bq24075-Q1:

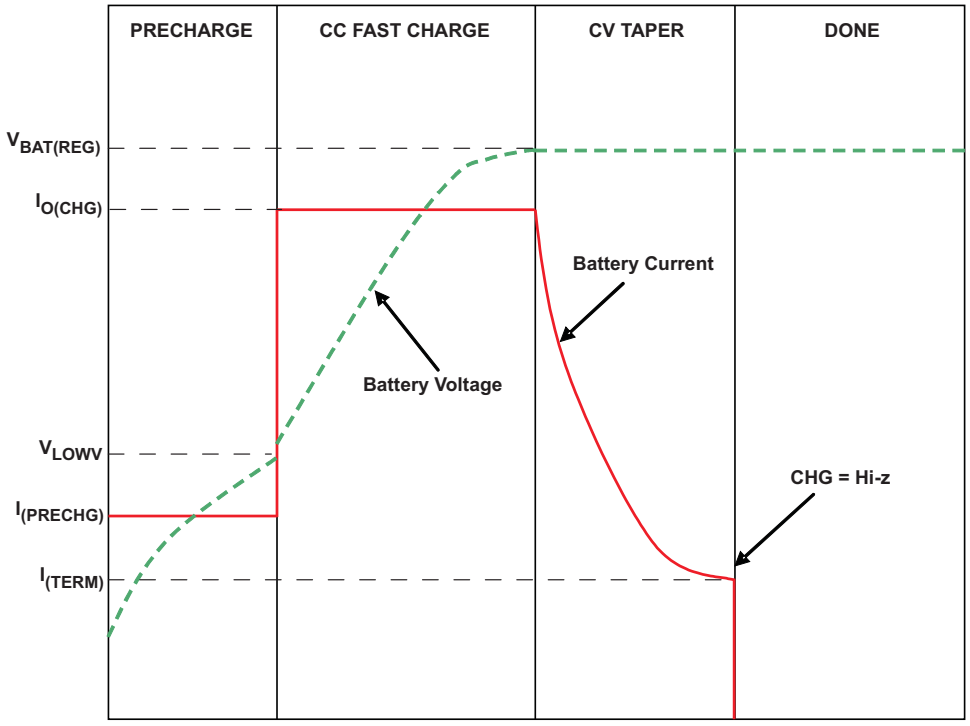


Figure 28. Typical Charge Cycle

In the pre-charge phase, the battery is charged at with the pre-charge current (I_{PRECHG}). Once the battery voltage crosses the V_{LOWV} threshold, the battery is charged with the fast-charge current (I_{CHG}). As the battery voltage reaches $V_{BAT(REG)}$, the battery is held at a constant voltage of $V_{BAT(REG)}$ and the charge current tapers off as the battery approaches full charge. When the battery current reaches I_{TERM}, the $\overline{CHG}$ pin indicates *charging done* by going high-impedance.

Note that termination detection is disabled whenever the charge rate is reduced because of the actions of the thermal loop, the DPPM loop or the $V_{IN(LOW)}$ loop.

The value of the fast-charge current is set by the resistor connected from the ISET pin to VSS, and is given by the equation

$$I_{CHG} = K_{ISET}/R_{ISET}$$

The charge current limit is adjustable up to 1.5A. The valid resistor range is 590Ω to 3 kΩ. Note that if I_{CHG} is programmed as greater than the input current limit, the battery will not charge at the rate of I_{CHG}, but at the slower rate of $I_{IN(MAX)}$ (minus the load current on the OUT pin, if any). In this case, the charger timers will be proportionately slowed down.

CHARGE CURRENT TRANSLATOR

When the charger is enabled, internal circuits generate a current proportional to the charge current at the ISET input. The current out of ISET is 1/400 (±10%) of the charge current. This current, when applied to the external charge current programming resistor, R_{ISET}, generates an analog voltage that can be monitored by an external host to calculate the current sourced from BAT.

$$V_{ISET} = I_{CHARGE} / 400 \times R_{ISET} \quad (1)$$

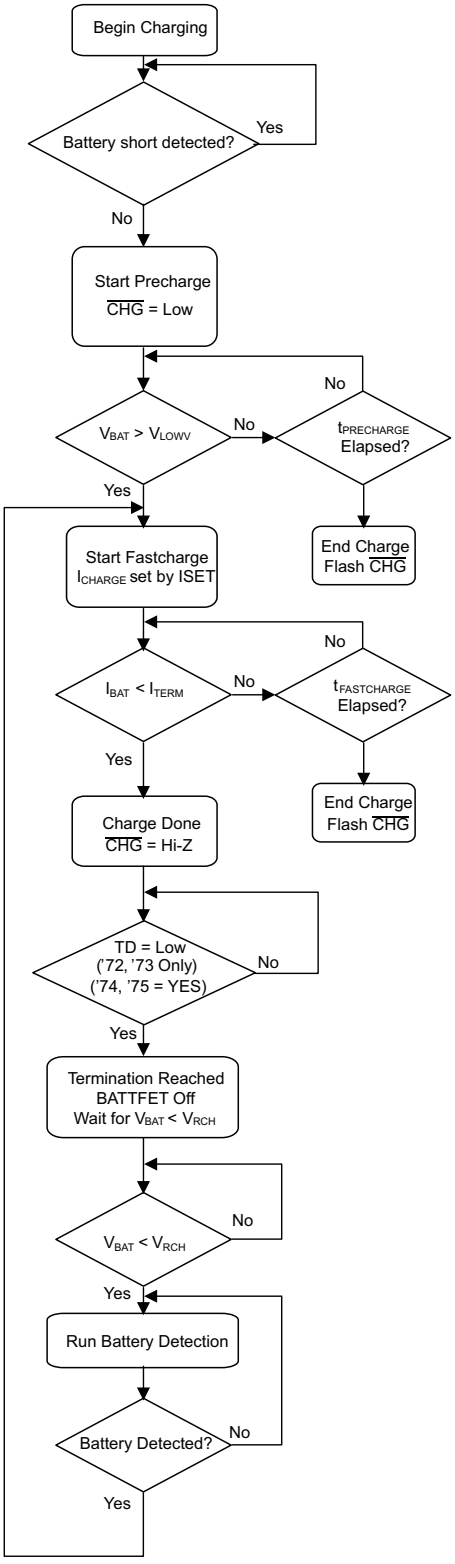


Figure 29. Battery Charging Flow Diagram

BATTERY DETECTION AND RECHARGE

The bq24075-Q1 automatically detects if a battery is connected or removed. Once a charge cycle is complete, the battery voltage is monitored. When the battery voltage falls below V_{RCH}, the battery detection routine is run. During battery detection, current ($I_{BAT(DET)}$) is pulled from the battery for a duration t_{DET} to see if the voltage on BAT falls below V_{LOWV}. If not, charging begins. If it does, then it indicates that the battery is missing or the protector is open. Next, the precharge current is applied for t_{DET} to close the protector if possible. If $V_{BAT} < V_{RCH}$, then the protector closed and charging is initiated. If $V_{BAT} > V_{RCH}$, then the battery is determined to be missing and the detection routine continues.

BATTERY DISCONNECT (SYSOFF Input)

The bq24075 feature a SYSOFF input that allows the user to turn the FET Q2 off and disconnect the battery from the OUT pin. This is useful for disconnecting the system load from the battery, factory programming where the battery is not installed or for host side impedance track fuel gauging, such as bq27500, where the battery open circuit voltage level must be detected before the battery charges or discharges. The /CHG output remains low when SYSOFF is high. Connect SYSOFF to VSS, to turn Q2 on for normal operation. SYSOFF is internally pulled to VBAT through ~5 MΩ resistor.

DYNAMIC CHARGE TIMERS (TMR Input)

The bq24075-Q1 device contains internal safety timers for the pre-charge and fast-charge phases to prevent potential damage to the battery and the system. The timers begin at the start of the respective charge cycles. The timer values are programmed by connecting a resistor from TMR to VSS. The resistor value is calculated using the following equation:

$$t_{PRECHG} = K_{TMR} \times R_{TMR}$$

$$t_{MAXCHG} = 10 \times K_{TMR} \times R_{TMR}$$

Leave TMR unconnected to select the internal default timers. Disable the timers by connecting TMR to VSS.

Note that timers are suspended when the device is in thermal shutdown, and the timers are slowed proportionally to the charge current when the device enters thermal regulation.

During the fast charge phase, several events increase the timer durations.

1. The system load current activates the DPPM loop which reduces the available charging current
2. The input current is reduced because the input voltage has fallen to $V_{IN(LOW)}$
3. The device has entered thermal regulation because the IC junction temperature has exceeded $T_{J(REG)}$

During each of these events, the internal timers are slowed down proportionately to the reduction in charging current. For example, if the charging current is reduced by half for two minutes, the timer clock is reduced to half the frequency and the counter counts half as fast resulting in only one minute of "counting" time.

If the pre charge timer expires before the battery voltage reaches V_{LOWV}, the bq24075-Q1 indicates a fault condition. Additionally, if the battery current does not fall to I_{TERM} before the fast charge timer expires, a fault is indicated. The $\overline{CHG}$ output flashes at approximately 2 Hz to indicate a fault condition. The fault condition is cleared by toggling $\overline{CE}$ or the input power, entering/ exiting USB suspend mode, or an OVP event.

STATUS INDICATORS ($\overline{PGOOD}$, $\overline{CHG}$)

The bq24075-Q1 contains two open-drain outputs that signal its status. The $\overline{PGOOD}$ output signals when a valid input source is connected. $\overline{PGOOD}$ is low when $(V_{BAT} + V_{IN(DT)}) < V_{IN} < V_{OVP}$. When the input voltage is outside of this range, $\overline{PGOOD}$ is high impedance.

The charge cycle after power-up, CE going low, or exiting OVP is indicated with the $\overline{CHG}$ pin on (low - LED on), whereas all refresh (subsequent) charges will result in the $\overline{CHG}$ pin off (open - LED off). In addition, the $\overline{CHG}$ signals timer faults by flashing at approximately 2 Hz.

Table 2. $\overline{PGOOD}$ STATUS INDICATOR

Input State	$\overline{PGOOD}$ Output
$V_{IN} < V_{UVLO}$	Hi impedance
$V_{UVLO} < V_{IN} < V_{IN(DT)}$	Hi impedance
$V_{IN(DT)} < V_{IN} < V_{OVP}$	Low

Table 2. $\overline{\text{PGOOD}}$ STATUS INDICATOR (continued)

Input State	$\overline{\text{PGOOD}}$ Output
$V_{IN} > V_{OVP}$	Hi impedance

Table 3. $\overline{\text{CHG}}$ STATUS INDICATOR

Charge State	$\overline{\text{CHG}}$ Output
Charging	Low (for first charge cycle)
Charging suspended by thermal loop	
Safety timers expired	Flashing at 2Hz
Charging done	Hi impedance
Recharging after termination	
IC disabled or no valid input power	
Battery absent	

THERMAL REGULATION AND THERMAL SHUTDOWN

The bq24075-Q1 contain a thermal regulation loop that monitors the die temperature. If the temperature exceeds $T_{J(REG)}$, the device automatically reduces the charging current to prevent the die temperature from increasing further. In some cases, the die temperature continues to rise despite the operation of the thermal loop, particularly under high VIN and heavy OUT system load conditions. Under these conditions, if the die temperature increases to $T_{J(OFF)}$, the input FET Q1 is turned OFF. FET Q2 is turned ON to ensure that the battery still powers the load on OUT. Once the device die temperature cools by $T_{J(OFF-HYS)}$, the input FET Q1 is turned on and the device returns to thermal regulation. Continuous overtemperature conditions result in a "hiccup" mode. During thermal regulation, the safety timers are slowed down proportionately to the reduction in current limit.

Note that this feature monitors the die temperature of the bq24075-Q1. This is not synonymous with ambient temperature. Self heating exists due to the power dissipated in the IC because of the linear nature of the battery charging algorithm and the LDO associated with OUT. A modified charge cycle with the thermal loop active is shown in Figure 30. Battery termination is disabled during thermal regulation.

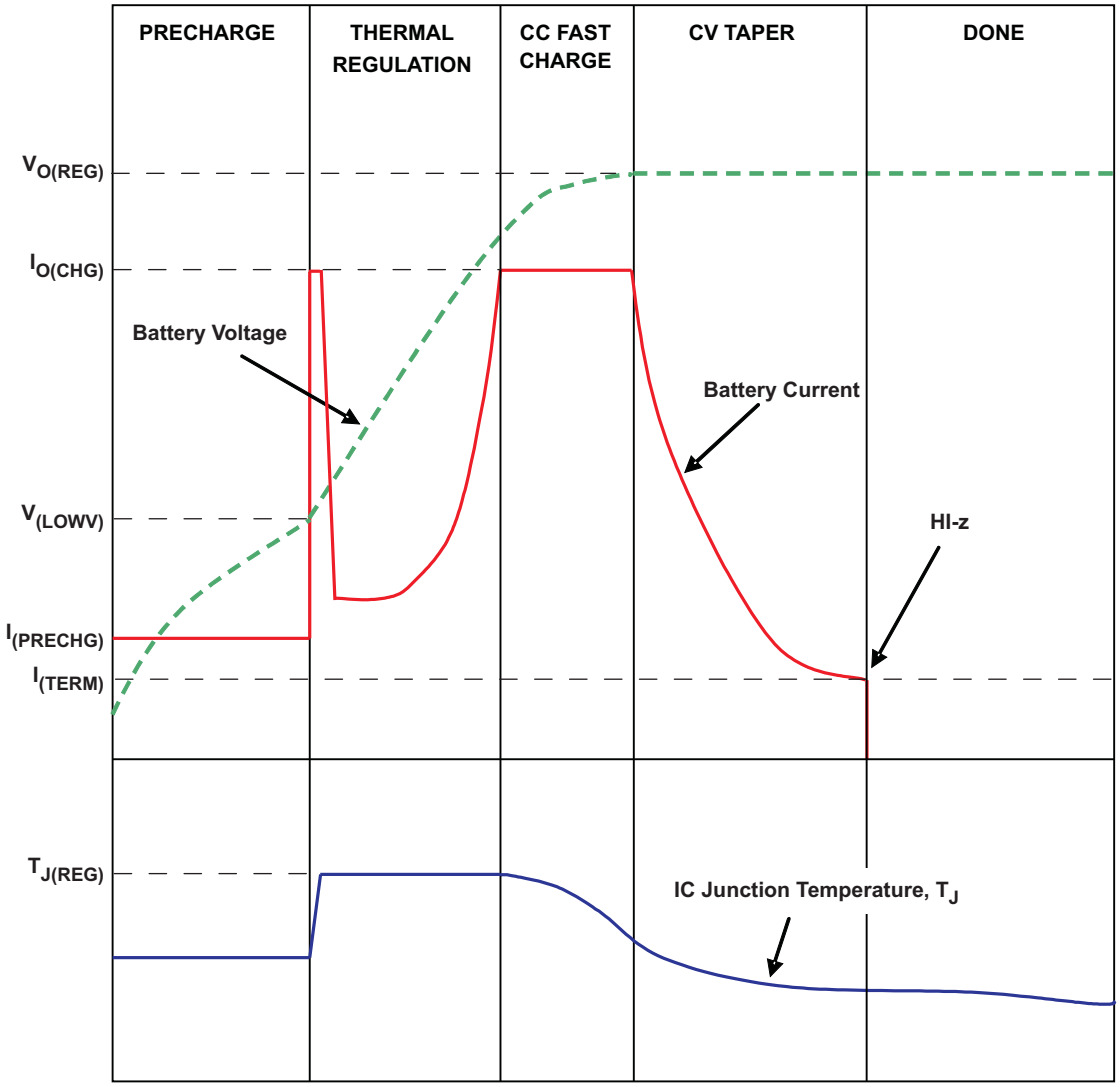


Figure 30. Charge Cycle Modified by Thermal Loop

BATTERY PACK TEMPERATURE MONITORING

The bq24075-Q1 features an external battery pack temperature monitoring input. The TS input connects to the NTC thermistor in the battery pack to monitor battery temperature and prevent dangerous over-temperature conditions. During charging, I_{NTC} is sourced to TS and the voltage at TS is continuously monitored. If, at any time, the voltage at TS is outside of the operating range (V_{COLD} to V_{HOT}), charging is suspended. The timers maintain their values but suspend counting. When the voltage measured at TS returns to within the operation window, charging is resumed and the timers continue counting. When charging is suspended due to a battery pack temperature fault, the $\overline{CHG}$ pin remains low and continues to indicate *charging*.

For applications that do not require the TS monitoring function, connect a 10kΩ resistor from TS to VSS to set the TS voltage at a valid level and maintain charging.

The allowed temperature range for 103AT-2 type thermistor is 0°C to 50°C. However, the user may increase the range by adding two external resistors. See Figure 31 for the circuit details. The values for Rs and Rp are calculated using the following equations:

$$Rs = \frac{-(R_{TH} + R_{TC}) \pm \sqrt{\left((R_{TH}+R_{TC})^2 - 4\left\{R_{TH} \times R_{TC} + \frac{V_H \times V_C}{(V_H - V_C) \times I_{TS}} \times (R_{TC} - R_{TH})\right\}\right)}}{2} \quad (2)$$

$$Rp = \frac{V_H \times (R_{TH} + R_S)}{I_{TS} \times (R_{TH} + R_S) - V_H} \quad (3)$$

Where:

R_{TH}: Thermistor Hot Trip Value found in thermistor data sheet
R_{TC}: Thermistor Cold Trip Value found in thermistor data sheet
V_H: IC's Hot Trip Threshold = 0.3V nominal
V_C: IC's Cold Trip Threshold = 2.1V nominal
I_{TS}: IC's Output Current Bias = 75µA nominal
NTC Thermsitor Semitec 103AT-4

Rs and Rp 1% values were chosen closest to calculated values

Cold Temp Resistance and Trip Threshold; Ω (°C)	Hot Temp Resistance and Trip Threshold; Ω (°C)	External Bias Resistor, Rs (Ω)	External Bias Resistor, Rp (Ω)
28000 (–0.6)	4000 (51)	0	∞
28480 (–1)	3536 (55)	487	845000
28480 (–1)	3021 (60)	1000	549000
33890 (–5)	4026 (51)	76.8	158000
33890 (–5)	3536 (55)	576	150000
33890 (–5)	3021 (60)	1100	140000

RHOT and RCOLD are the thermistor resistance at the desired hot and cold temperatures, respectively. **Note that the temperature window cannot be tightened more than using only the thermistor connected to TS, it can only be extended.**

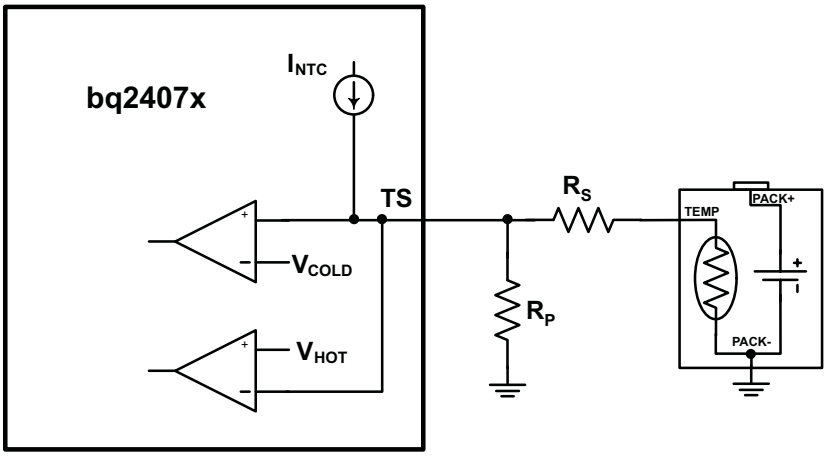


Figure 31. Extended TS Pin Thresholds

APPLICATIONS INFORMATION

bq24075-Q1 CHARGER DESIGN EXAMPLE

See Figure 19 for Schematics of the Design Example.

Requirements

- Supply voltage = 5V
- Fast charge current of approximately 800 mA; ISET - pin 16
- Input Current Limit =1.3A; ILIM - pin 12
- Termination Current Threshold = 110mA
- Safety timer duration, Fast-Charge = 6.25 hours; TMR – pin 14
- TS – Battery Temperature Sense = 10kΩ NTC (103AT-2)

Calculations

Program the Fast Charge Current (ISET):

$R_{ISET} = K_{ISET} / I_{CHG}$
K_{ISET} = 890 AΩ from the electrical characteristics table.
R_{ISET} = 890AΩ/0.8A = 1.1125 kΩ

Select the closest standard value, which for this case is 1.13kΩ. Connect this resistor between ISET (pin 16) and V_{SS}.

Program the Input Current Limit (ILIM)

$R_{ILIM} = K_{ILIM} / I_{I\_MAX}$
K_{ILIM} = 1550 AΩ from the electrical characteristics table.
R_{ISET} = 1550AΩ / 1.3A = 1.192 kΩ

Select the closest standard value, which for this case is 1.18 kΩ. Connect this resistor between ILIM (pin 12) and V_{SS}.

Program 6.25-hour Fast-Charge Safety Timer (TMR)

$R_{TMR} = t_{MAXCHG} / (10 \times K_{TMR})$
K_{TMR} = 48 s/kΩ from the electrical characteristics table.
R_{TMR} = (6.25 hr × 3600 s/hr) / (10 × 48 s/kΩ) = 46.8kΩ

Select the closest standard value, which for this case is 46.4 kΩ. Connect this resistor between TMR (pin 2) and V_{SS}.

TS Function

Use a 10kΩ NTC thermistor in the battery pack (103AT-2). For applications that do not require the TS monitoring function, connect a 10kΩ resistor from TS to VSS to set the TS voltage at a valid level and maintain charging.

$\overline{\text{CHG}}$ and $\overline{\text{PGOOD}}$

LED Status: connect a 1.5kΩ resistor in series with a LED between OUT and $\overline{\text{CHG}}$ to indicate charging status. Connect a 1.5kΩ resistor in series with a LED between OUT and $\overline{\text{PGOOD}}$ to indicate when a valid input source is connected.

Processor Monitoring Status: connect a pullup resistor (on the order of 100 kΩ) between the processor's power rail and $\overline{\text{CHG}}$ and $\overline{\text{PGOOD}}$

System ON/OFF (SYSOFF)

Connect SYSOFF high to disconnect the battery from the system load. Connect SYSOFF low for normal operation

SELECTING IN, OUT AND BAT pin CAPACITORS

In most applications, all that is needed is a high-frequency decoupling capacitor (ceramic) on the power pin, input, output and battery pins. Using the values shown on the application diagram, is recommended. After evaluation of these voltage signals with real system operational conditions, one can determine if capacitance values can be adjusted toward the minimum recommended values (DC load application) or higher values for fast high amplitude pulsed load applications. Note if designed high input voltage sources (bad adaptors or wrong adaptors), the capacitor needs to be rated appropriately. Ceramic capacitors are tested to 2x their rated values so a 16V capacitor may be adequate for a 30V transient (verify tested rating with capacitor manufacturer).

THERMAL PACKAGE

The bq24075 is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). The power pad should be directly connected to the V_{SS} pin. Full PCB design guidelines for this package are provided in the application note entitled: QFN/SON PCB Attachment Application Note (SLUA271). The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$\theta_{JA} = (T_J - T) / P$

Where:

T_J = chip junction temperature

T = ambient temperature

P = device power dissipation

Factors that can influence the measurement and calculation of θ_{JA} include:

1. Whether or not the device is board mounted
2. Trace size, composition, thickness, and geometry
3. Orientation of the device (horizontal or vertical)
4. Volume of the ambient air surrounding the device under test and airflow
5. Whether other surfaces are in close proximity to the device being tested

Due to the charge profile of Li-Ion batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. Typically after fast charge begins the pack voltage increases to ≠3.4V within the first 2 minutes. The thermal time constant of the assembly typically takes a few minutes to heat up so when doing maximum power dissipation calculations, 3.4V is a good minimum voltage to use. This is verified, with the system and a fully discharged battery, by plotting temperature on the bottom of the PCB under the IC (pad should have multiple vias), the charge current and the battery voltage as a function of time. The fast charge current will start to taper off if the part goes into thermal regulation.

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged :

$$P = [V_{(IN)} - V_{(OUT)}] \times I_{(OUT)} + [V_{(OUT)} - V_{(BAT)}] \times I_{(BAT)} \quad (3)$$

The thermal loop feature reduces the charge current to limit excessive IC junction temperature. It is recommended that the design not run in thermal regulation for typical operating conditions (nominal input voltage and nominal ambient temperatures) and use the feature for non typical situations such as hot environments or higher than normal input source voltage. With that said, the IC will still perform as described, if the thermal loop is always active.

Half-Wave Adaptors

Some adapters implement a half rectifier topology, which causes the adapter output voltage to fall below the battery voltage during part of the cycle. To enable operation with adapters under those conditions, the bq24075-Q1 family keeps the charger on for at least 20 msec (typical) after the input power puts the part in sleep mode. This feature enables use of external adapters using 50 Hz networks. The input must not drop below the UVLO voltage for the charger to work properly. Thus, the battery voltage should be above the UVLO to help prevent the input from dropping out. Additional input capacitance may be needed.

Sleep Mode

When the input is between UVLO and $V_{IN(DT)}$, the device enters sleep mode. After entering sleep mode for >20mS the internal FET connection between the IN and OUT pin is disabled and pulling the input to ground will not discharge the battery, other than the leakage on the BAT pin. If one has a full 1000mAHr battery and the leakage is 10µA, then it would take 1000mAHr/10µA = 100000 hours (11.4 years) to discharge the battery. The battery's self discharge is typically 5 times higher than this.

Layout Tips

- To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the bq24075-Q1, with short trace runs to both IN, OUT and GND (thermal pad).
- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces
- The bq24075-Q1 family is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. Full PCB design guidelines for this package are provided in the application note entitled: QFN/SON PCB Attachment Application Note (SLUA271).

REVISION HISTORY

Changes from Original (February 2012) to Revision A	Page
• Changed the device status From: Product Preview To: Production	1

Changes from Revision A (March 2012) to Revision B	Page
• Changed the Device HBM ESD and Device CDM ESD items in the Features List	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ24075QRGTRQ1	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	SAM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF BQ24075-Q1 :

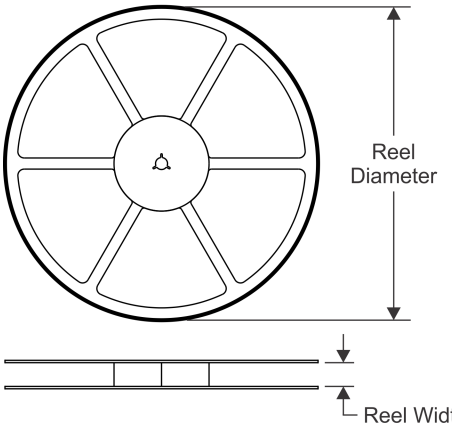
- Catalog: BQ24075

NOTE: Qualified Version Definitions:

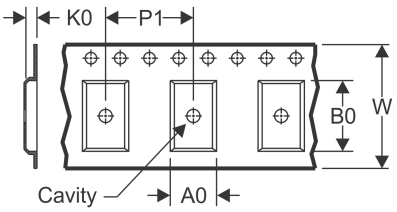
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

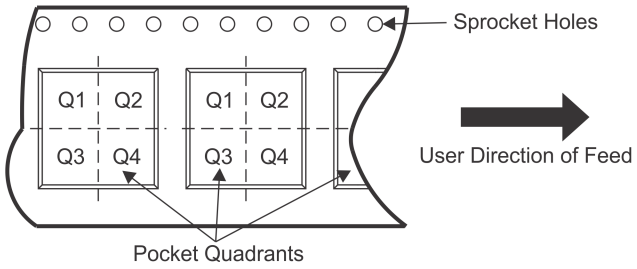


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

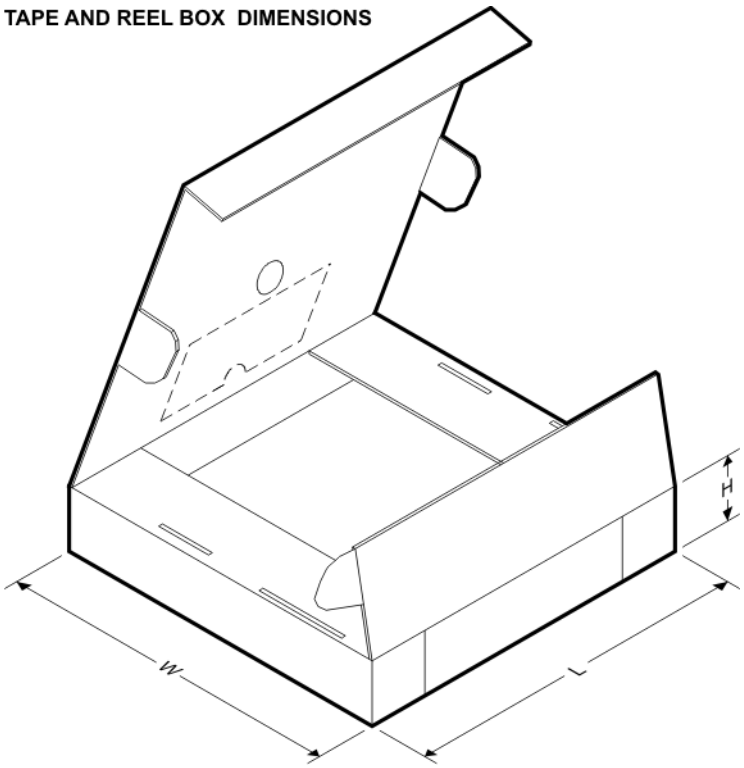
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24075QRGTRQ1	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

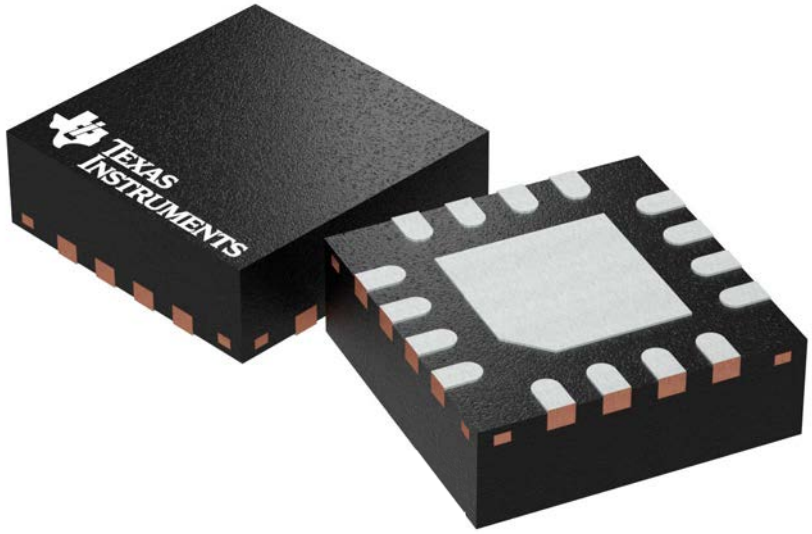


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24075QRGTRQ1	QFN	RGT	16	3000	367.0	367.0	35.0

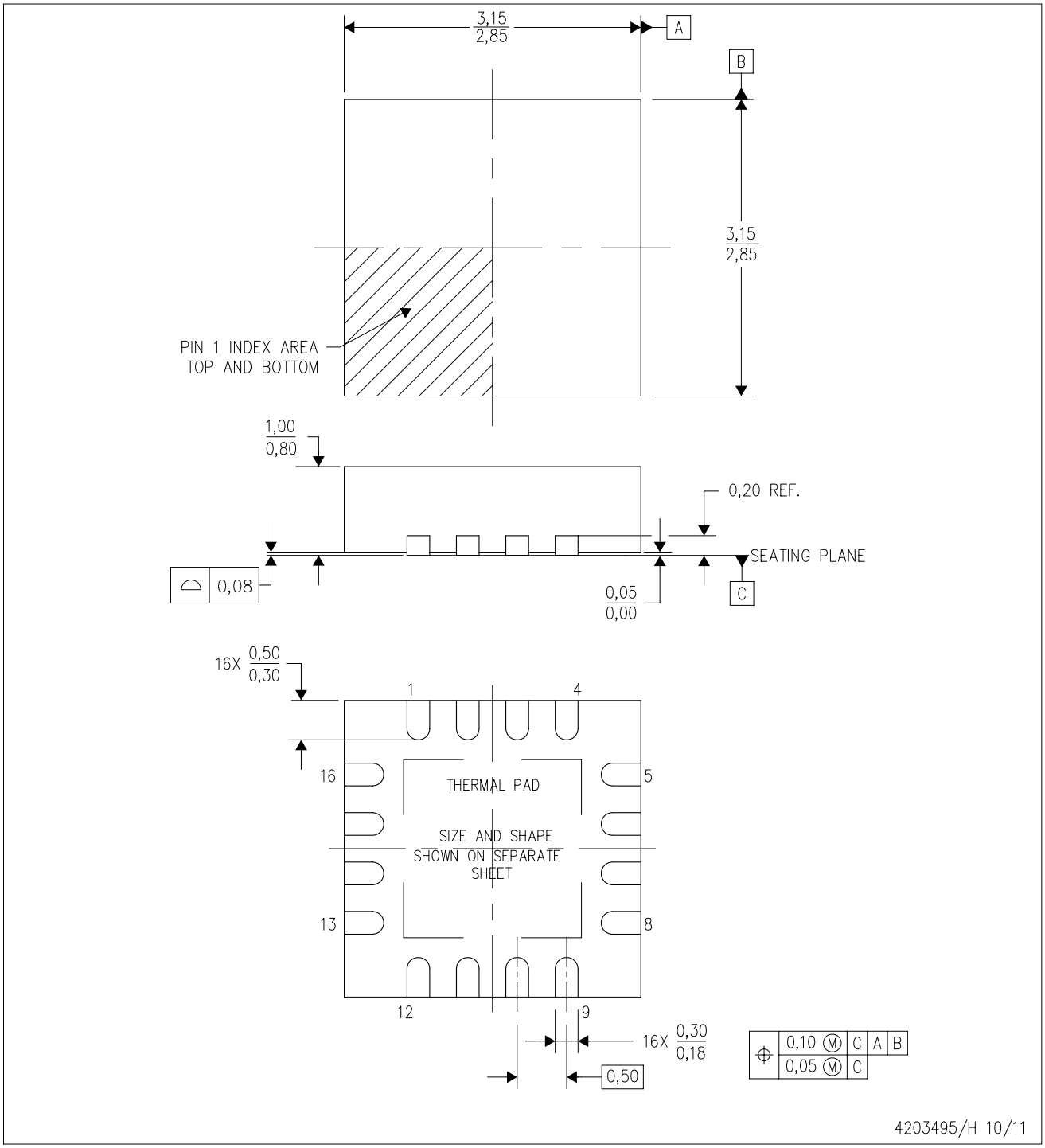
RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

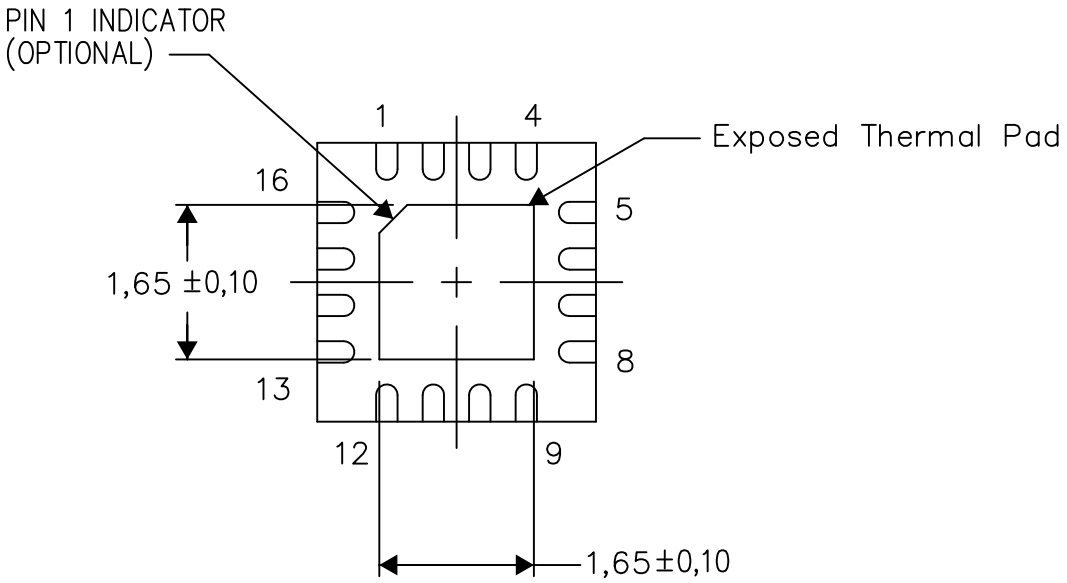
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206349–7/Z 08/15

NOTE: All linear dimensions are in millimeters

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265