TEXAS INSTRUMENTS

CSD95472Q5MC

SLPS599 – FEBRUARY 2016

CSD95472Q5MC Synchronous Buck NexFET™ Smart Power Stage

1 Features

- 60-A Continuous Operating Current Capability
- 94.4% System Efficiency at 1.2 V / 30 A
- Low Power Loss of 2.3 W at 30 A
- High-Frequency Operation (up to 1.25 MHz)
- Diode Emulation Mode With FCCM
- Temperature-Compensated Bidirectional Current Sense
- Analog Temperature Output (600 mV at 0°C)
- Fault Monitoring
  - High-Side Short, Overcurrent, and Overtemperature Protection
- 3.3-V and 5-V PWM Signal Compatible
- Tri-State PWM Input
- Integrated Bootstrap Diode
- Optimized Deadtime for Shoot-Through Protection
- High-Density SON 5 × 6 mm Footprint
- Ultralow Inductance Package
- System-Optimized PCB Footprint
- DualCool™ Packaging
- RoHS Compliant – Lead-Free Terminal Plating
- Halogen Free

2 Applications

- Multiphase Synchronous Buck Converters
  - High-Frequency Applications
  - High-Current, Low Duty Cycle Applications
- POL DC-DC Converters
- Memory and Graphic Cards

3 Description

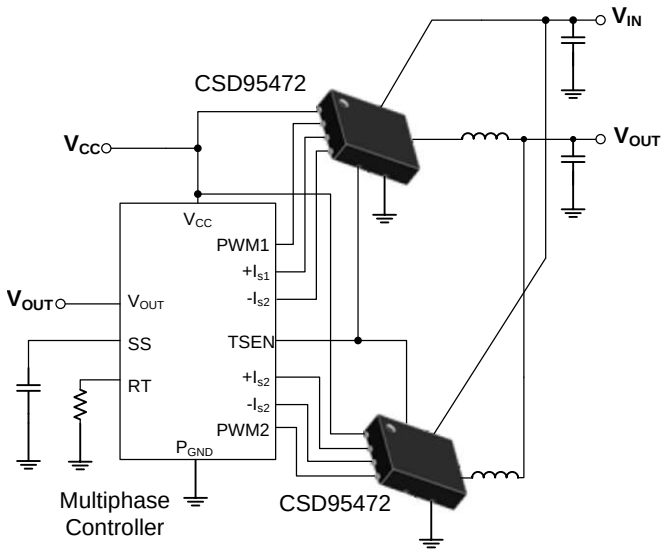
The CSD95472Q5MC NexFET™ smart power stage is a highly optimized design for use in a high-power, high-density synchronous buck converter. This product integrates the driver IC and Power MOSFETs to complete the power stage switching function. This combination produces high-current, high-efficiency, and high-speed switching capability in a small 5 mm × 6 mm outline package. It also integrates the accurate current sensing and temperature sensing functionality to simplify system design and improve accuracy. In addition, the PCB footprint has been optimized to help reduce design time and simplify the completion of the overall system design.

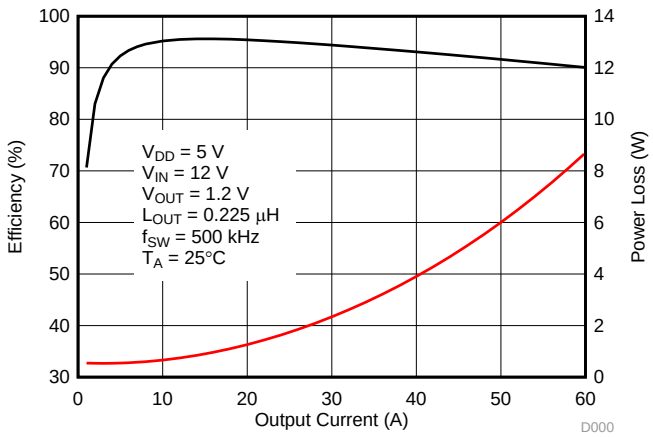
Device Information(1)

DEVICE	MEDIA	QTY	PACKAGE	SHIP
CSD95472Q5MC	13-Inch Reel	2500	SON 5 × 6 mm DualCool Package	Tape and Reel
CSD95472Q5MCT	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Diagram





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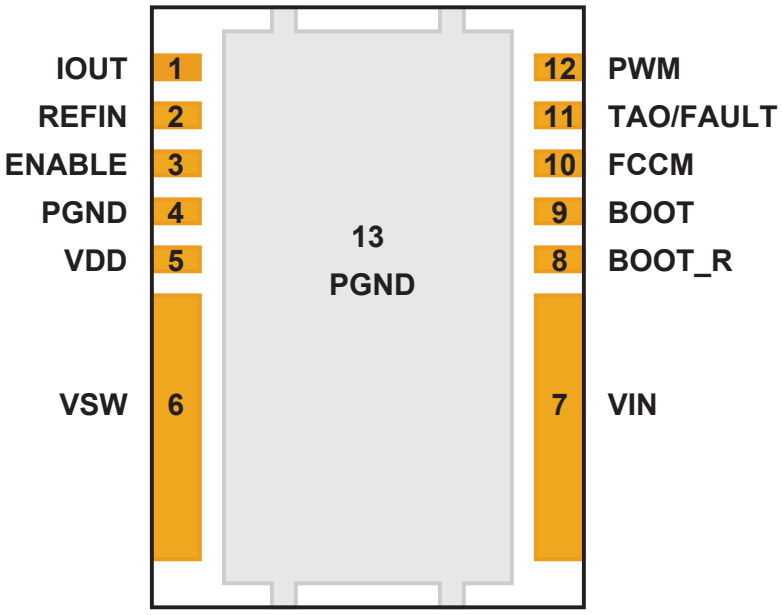
4 Revision History

DATE	REVISION	NOTES
February 2016	*	Initial release.

5 Pin Configuration and Functions

Top View



Pin Functions

PIN		DESCRIPTION
NUMBER	NAME	
1	IOUT	Output of current sensing amplifier. V(IOUT) – V(REFIN) is proportional to the phase current.
2	REFIN	External reference voltage input for current sensing amplifier.
3	ENABLE	Enables device operation. If ENABLE = logic HIGH, turns on device. If ENABLE = logic LOW, the device is turned off and both MOSFET gates are actively pulled low. An internal 100 kΩ pulldown resistor will pull the ENABLE pin LOW if left floating.
4	P_{GND}	Power ground, connected directly to pin 13.
5	V_{DD}	Supply voltage to gate driver and internal circuitry.
6	V_{SW}	Phase node connecting the HS MOSFET source and LS MOSFET drain – pin connection to the output inductor.
7	V_{IN}	Input voltage pin. Connect input capacitors close to this pin.
8	BOOT_R	Return path for HS gate driver, connected to V_{SW} internally.
9	BOOT	Bootstrap capacitor connection. Connect a minimum of 0.1 µF 16 V X7R ceramic capacitor from BOOT to BOOT_R pins. The bootstrap capacitor provides the charge to turn on the control FET. The bootstrap diode is integrated.
10	FCCM	This pin enables the diode emulation function. When this pin is held LOW, diode emulation mode is enabled for sync FET. When FCCM is HIGH, the device is operated in forced continuous conduction mode. An internal 5 µA current source will pull the FCCM pin to 3.3 V if left floating.
11	TAO/ FAULT	Temperature Analog Output. Reports a voltage proportional to the die temperature. An ORing diode is integrated in the IC. When used in multiphase application, a single wire can be used to connect the TAO pins of all the ICs. Only the highest temperature will be reported. TAO will be pulled up to 3.3 V if thermal shutdown occurs. TAO should be bypassed to P_{GND} with a 1 nF 16 V X7R ceramic capacitor.
12	PWM	Pulse width modulated tri-state input from external controller. Logic LOW sets control FET gate low and sync FET gate high. Logic HIGH sets control FET gate high and sync FET gate low. Open or High Z sets both MOSFET gates low if greater than the tri-state shutdown hold-off time (t_{3HT}).
13	P_{GND}	Power ground.

6 Specifications

6.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
	V_{IN} to P_{GND}	–0.3	20	V
	V_{IN} to V_{SW}	–0.3	20	V
	V_{IN} to V_{SW} (10 ns)		23	V
	V_{SW} to P_{GND}	–0.3	20	V
	V_{SW} to P_{GND} (10 ns)	–7	23	V
	V_{DD} to P_{GND}	–0.3	7	V
	ENABLE, PWM, FCCM, TAO, IOUT, REFIN to P_{GND}(2)	–0.3	V_{DD} + 0.3 V	V
	BOOT to BOOT_R(2)	–0.3	V_{DD} + 0.3 V	V
P_D	Power dissipation		12	W
T_J	Operating junction	–55	150	°C
T_{stg}	Storage temperature	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Should not exceed 7 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM)	±2000	V
		Charged device model (CDM)	±500	

6.3 Recommended Operating Conditions

T_A = 25° (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Gate drive voltage		4.5	5.5	V
V_{IN}	Input supply voltage(1)			16	V
V_{OUT}	Output voltage			5.5	V
I_{OUT}	Continuous output current	V_{IN} = 12 V, V_{DD} = 5 V, V_{OUT} = 1.2 V, f_{SW} = 500 kHz, L_{OUT} = 0.225 µH(2)		60	A
I_{OUT-PK}	Peak output current(3)			90	A
f_{SW}	Switching frequency	C_{BST} = 0.1 µF (min)		1250	kHz
	On time duty cycle	f_{SW} = 1 MHz		85%	
	Minimum PWM on time		40		ns
	Operating temperature		–40	125	°C

(1) Operating at high V_{IN} can create excessive AC voltage overshoots on the switch node (V_{SW}) during MOSFET switching transients. For reliable operation, the switch node (V_{SW}) to ground voltage must remain at or below the *Absolute Maximum Ratings*.
(2) Measurement made with six 10 µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins.
(3) System conditions as defined in Note 1. Peak Output Current is applied for t_p = 50 µs.

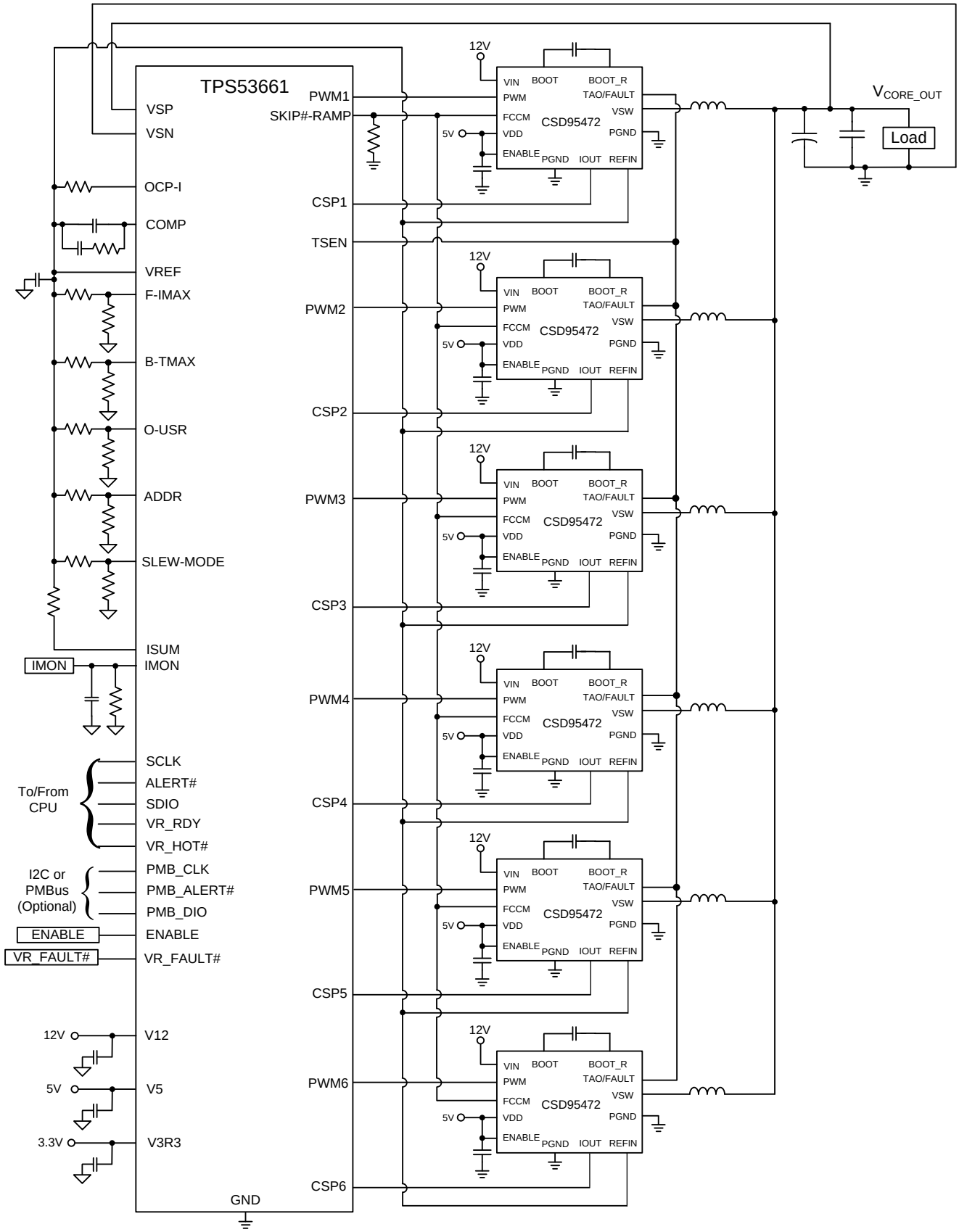
6.4 Thermal Information

T_A = 25°C (unless otherwise noted)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC(top)}$	Junction-to-case (top of package) thermal resistance (1)			5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance(2)			1.5	

(1) $R_{\theta JC(top)}$ is determined with the device mounted on a 1 inch² (6.45 cm²), 2-oz (0.071 mm thick) Cu pad on a 1.5 inches x 1.5 inches, 0.06-inch (1.52-mm) thick FR4 board.
(2) $R_{\theta JB}$ value based on hottest board temperature within 1 mm of the package.

7 Application Schematic



8 Device and Documentation Support

8.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.2 Trademarks

NexFET, DualCool, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

8.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.4 Glossary

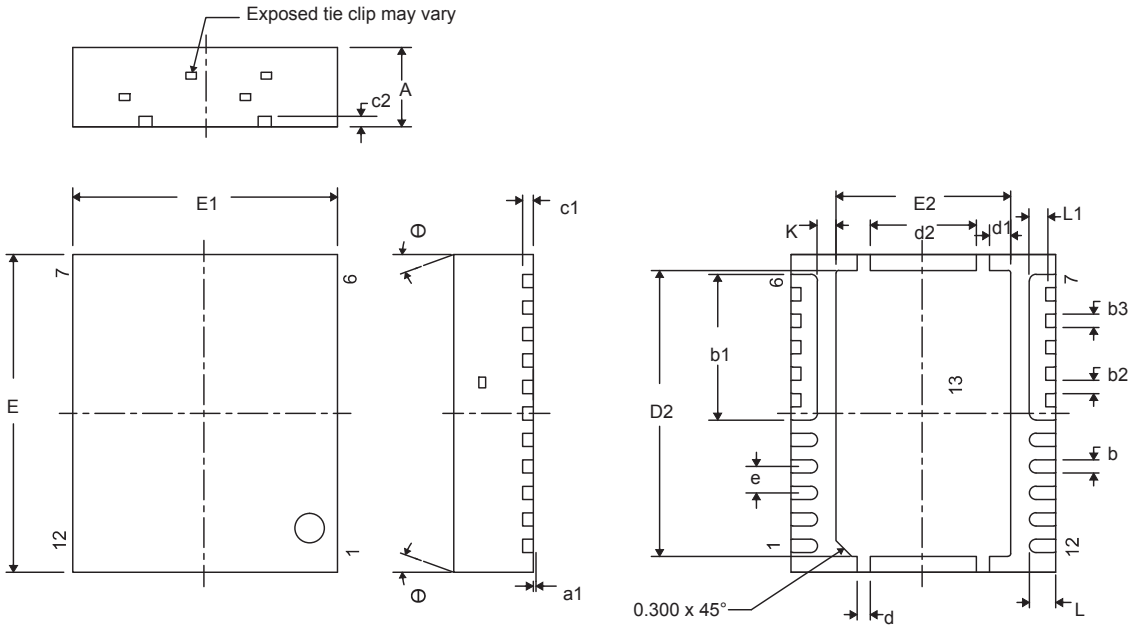
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

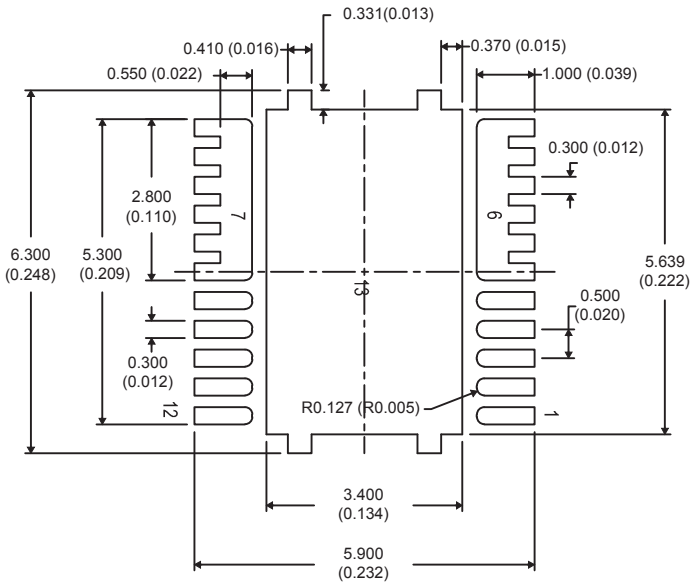
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

9.1 Mechanical Drawing



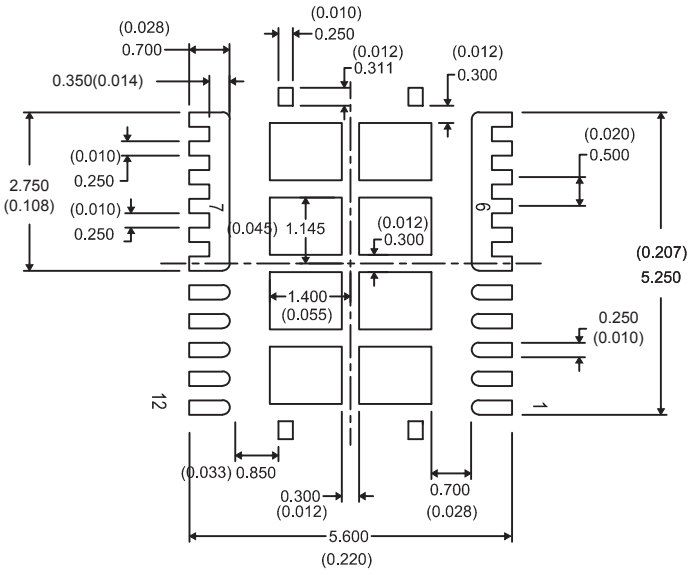
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.050	0.037	0.039	0.041
a1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.200	0.250	0.320	0.008	0.010	0.013
b1		2.750 TYP			0.108 TYP	
b2	0.200	0.250	0.320	0.008	0.010	0.013
b3		0.250 TYP			0.010 TYP	
c1	0.150	0.200	0.250	0.006	0.008	0.010
c2	0.200	0.250	0.300	0.008	0.010	0.012
D2	5.300	5.400	5.500	0.209	0.213	0.217
d	0.200	0.250	0.300	0.008	0.010	0.012
d1	0.350	0.400	0.450	0.014	0.016	0.018
d2	1.900	2.000	2.100	0.075	0.079	0.083
E	5.900	6.000	6.100	0.232	0.236	0.240
E1	4.900	5.000	5.100	0.193	0.197	0.201
E2	3.200	3.300	3.400	0.126	0.130	0.134
e		0.500 TYP			0.020 TYP	
K		0.350 TYP			0.014 TYP	
L	0.400	0.500	0.600	0.016	0.020	0.024
L1	0.210	0.310	0.410	0.008	0.012	0.016
θ	0.00	—	—	0.00	—	—

9.2 Recommended PCB Land Pattern



1. Dimensions are in mm (inches).

9.3 Recommended Stencil Opening



1. Dimensions are in mm (inches).
2. Stencil thickness is 100 µm.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD95472Q5MC	ACTIVE	VSON-CLIP	DMC	12	2500	Pb-Free (RoHS Exempt)	CU SN	Level-2-260C-1 YEAR	-55 to 150	95472MC	Samples
CSD95472Q5MCT	ACTIVE	VSON-CLIP	DMC	12	250	Pb-Free (RoHS Exempt)	CU SN	Level-2-260C-1 YEAR	-55 to 150	95472MC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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