DRV8846 Dual H-Bridge Stepper Motor Driver

1 Features

- PWM Microstepping Motor Driver
  - Built-In Microstepping Indexer
  - Up to 1/32 Microstepping
  - Step/Direction Control
- Multiple Decay Modes
  - Adaptive Decay
  - Mixed Decay
  - Slow Decay
  - Fast Decay
- Configurable Off-Time PWM Chopping
  - 10-, 20-, or 30-µs Off-Time
- Adaptive Blanking Time for Smooth Stepping
- 4- to 18-V Operating Supply Voltage Range
- 1-A Continuous/RMS Output Current per H-Bridge (at 25°C)
- Low-Current Sleep Mode
- 3-Bit Torque DAC to Scale Motor Current
- Thermally Enhanced Surface Mount Package
- Protection Features
  - VM Undervoltage Lockout (UVLO)
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
  - Fault Condition Indication Pin (nFAULT)

2 Applications

- Printers
- Scanners
- Video Security Cameras
- Projectors

3 Description

The DRV8846 provides a highly-integrated stepper motor driver for cameras, printers, projectors, and other automated equipment applications. The device has two H-bridges and a microstepping indexer and is intended to drive a bipolar stepper motor. The output block of each H-bridge driver consists of N-channel and P-channel power MOSFETs configured as full H-bridges to drive the motor windings. The DRV8846 is capable of driving up to 1-A full scale output current (with proper heatsinking and T_A = 25°C).

A simple STEP/DIR interface allows easy interfacing to controller circuits. Pins allow configuration of the motor in full-step up to 1/32-step modes. Decay mode is configurable so that adaptive decay, slow decay, fast decay, and mixed decay can be used. The PWM current chopping off-time can also be selected. A low-power sleep mode is provided which shuts down internal circuitry to achieve very-low quiescent current draw. This sleep mode can be set using a dedicated nSLEEP pin.

Internal protection functions are provided for UVLO, overcurrent protection, short circuit protection, and overtemperature. Fault conditions are indicated via a nFAULT pin.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8846	QFN (24)	4.00 × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

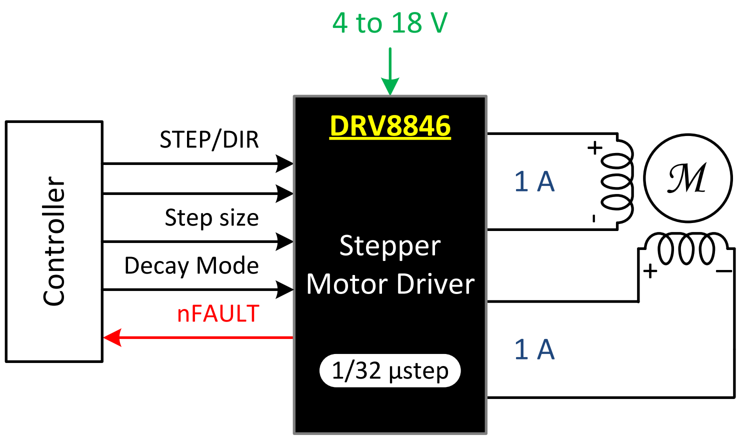


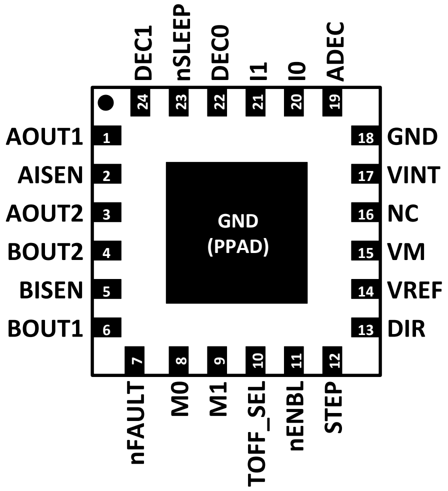
Table of Contents

5 Revision History

DATE	REVISION	NOTES
June 2014	*	Initial release.

6 Pin Configuration and Functions

RGE (VQFN) Package
24 Pins
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION	
NAME	NO.			
ADEC	19	I	Adaptive decay enable	Logic low sets decay modes by DEC0 and DEC1 pins; logic high – adaptive decay operation is enabled; must be set prior to coming out of sleep; internal pulldown
AISEN	2	O	Winding A sense	Connect to current sense resistor for bridge A, or GND if current regulation is not required
AOUT1	1	O	Winding A output	
AOUT2	3			
BISEN	5	O	Winding B sense	Connect to current sense resistor for bridge B, or GND if current regulation is not required
BOUT1	6	O	Winding B output	
BOUT2	4			
DEC0	22	I	Decay mode setting pins	Sets the decay mode; see description section; tri-level pin
DEC1	24	I		
DIR	13	I	Direction input	Logic level sets the direction of stepping; internal pulldown
GND	18, PPAD	PWR	Device ground	Both the GND pin and device PowerPAD™ must be connected to ground
I0	20	I	Torque DAC current scalar	Scales the current from 100% to 12.5% in 12.5% steps; tri-level pin
I1	21	I		
MO	8	I	Microstepping mode setting pins	Controls step mode (full, half, up to 1/32-step) and single- or dual-edge clocking; tri-level pin
M1	9	I		
NC	16	—	No connect	Unused pin not connected internally
nENBL	11	I	Enable driver output	Logic low to enable device outputs and internal indexer; logic high to disable; internal pulldown
nFAULT	7	OD	Fault indication pin	Pulled logic low with fault condition; open-drain output requires external pullup
nSLEEP	23	I	Sleep mode input	Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown
STEP	12	I	Step input	A rising edge (or rising and falling depending on step mode) advances the indexer one step; internal pulldown
TOFF_SEL	10	I	Decay mode off time set	Sets the off-time during current chopping; tri-level pin

Pin Functions (continued)

PIN		I/O	DESCRIPTION	
NAME	NO.			
VINT	17	—	Internal regulator	Internal supply voltage; bypass to GND with 2.2-μF, 6.3-V capacitor
VM	15	PWR	Power supply	Connect to motor power supply; bypass to GND with a 0.1- and 10-μF (minimum) ceramic capacitor rated for VM
VREF	14	I	Full-scale current reference input	Voltage on this pin sets the full scale chopping current; short to VINT if not supplying an external reference voltage

Table 1. External Components

Component	Pin 1	Pin 2	Recommended
C_{VM}	VM	GND	10-μF (minimum) ceramic capacitor rated for VM
C_{VM}	VM	GND	0.1-μF ceramic capacitor rated for VM
C_{VINT}	VINT	GND	6.3-V, 2.2-μF ceramic capacitor
R_{nFAULT}	VCC (1)	nFAULT	>5 kΩ
R_{AISEN}	AISEN	GND	Sense resistor, see applications section for sizing
R_{BISEN}	BISEN	GND	Sense resistor, see applications section for sizing

(1) VCC is not a pin on the DRV8846, but a VCC supply voltage pullup is required for open-drain output nFAULT; nFAULT may be pulled up to VINT through a resistor R_{nFAULT}

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature referenced with respect to GND (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply voltage (VM)		–0.3	20	V
Power supply voltage ramp rate (VM)		0	2	V/µs
Internal regulator voltage (VINT)		–0.3	3.6	V
Analog input pin voltage (VREF)		–0.3	3.6	V
Control pin voltage (nENABLE, STEP, DIR, I0, I1, M0, M1, DEC0, DEC1, TOFF_SEL, nSLEEP, nFAULT, ADEC)		–0.3	7.0	V
Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)		–0.3	VM + 0.6	V
Continuous shunt amplifier input pin voltage (AISEN, BISEN)(2)		–0.6	0.6	V
Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2, AISEN, BISEN)		Internally limited		A
T_J	Operating junction temperature	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transients of ±1 V for less than 25 ns are acceptable.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–4	4	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–1.5	1.5	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VM	Power supply voltage range(1)	4	18	V
VREF	Reference rms voltage range(2)	1	3.3	V
f_{PWM}	Applied STEP signal	0	250	kHz
I_{VINT}	VINT external load current		1	mA
I_{rms}	Motor rms current per H-bridge(3)	0	1	A
T_A	Operating ambient temperature	–40	85	°C

(1) Note that $R_{DS(ON)}$ increases and maximum output current is reduced at VM supply voltages below 5 V
(2) Operational at VREF between 0 to 1 V, but accuracy is degraded
(3) Power dissipation and thermal limits must be observed

7.4 Thermal Information

THERMAL METRIC(1)		DRV8846	UNIT
		QFN	
		24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	12.5	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	12.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, VINT)						
VM	VM operating voltage		4		18	V
I_{VM}	VM operating supply current	VM = 12 V, excluding winding current, nSLEEP = 1, nENBL = 0 or 1	3.5	4.5	5.5	mA
I_{VMQ}	VM sleep mode supply current	VM = 12 V, nSLEEP = 0, nENBL = 0 or 1	0.5	1.2	3	μA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep mode			1	ms
t_{WAKE}	Wake time	nSLEEP = 1 to output transition			1	ms
t_{ON}	Power-on time	VM > V_{UVLO} rising to output transition			1	ms
VINT	VINT voltage	VM > 4 V, I_{OUT} = 0 A to 1 mA	3.13	3.3	3.47	V
LOGIC-LEVEL INPUTS (STEP, DIR, nENBL, nSLEEP, ADEC)						
V_{IL}	Input logic low voltage		0		0.7	V
V_{IH}	Input logic high voltage		1.6		5.5	V
V_{HYS}	Input logic hysteresis		100			mV
I_{IL}	Input logic low current	VIN = 0 V	–1		1	μA
I_{IH}	Input logic high current	VIN = 5 V	1		30	μA
R_{PD}	Pulldown resistance	nENBL, STEP, DIR, ADEC		200		kΩ
		nSLEEP		500		
t_{DEG}	Input deglitch time			200		ns
t_{PROP}	Propagation delay	STEP edge to current change		600		ns
TRI-LEVEL INPUTS (I0, I1, M0, M1, DEC0, DEC1, TOFF_SEL)						
V_{IL}	Tri-level input logic low voltage		0		0.7	V
V_{IZ}	Tri-level input Hi-Z voltage			1.1		V
V_{IH}	Tri-level input logic high voltage		1.6		5.5	V
V_{HYS}	Tri-level input hysteresis		100			mV
I_{IL}	Tri-level input logic low current	V_{IN} = 0 V	–30		–1	μA
I_{IH}	Tri-level input logic high current	V_{IN} = 5 V	1		30	μA
R_{PD}	Tri-level pulldown resistance	To GND		170		kΩ
R_{PU}	Tri-level pullup resistance	To VINT		340		kΩ
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic high leakage	V_O = 3.3 V	–1		1	μA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ON)}$	High-side FET on resistance	VM = 12 V, I = 0.5 A, T_J = 25°C		550		Ω
		VM = 12 V, I = 0.5 A, T_J = 85°C(1)		660		
$R_{DS(ON)}$	Low-side FET on resistance	VM = 12 V, I = 0.5 A, T_J = 25°C		350		Ω
		VM = 12 V, I = 0.5 A, T_J = 85°C(1)		420		
I_{OFF}	Off-state leakage current	VM = 5 V, T_J = 25°C	–1		1	μA
t_{RISE}	Output rise time			60		ns
t_{FALL}	Output fall time			60		ns
t_{DEAD}	Output dead time	Internal dead time		200		ns
PWM CURRENT CONTROL (VREF, AISEN, BISEN)						
I_{REF}	Externally applied VREF input current	VREF = 1 to 3.3 V			1	μA
V_{TRIP}	xISEN trip voltage	For 100% current step with VREF = 3.3 V		500		mV
A_{ISENSE}	Current sense amplifer gain	Reference only		6.6		V/V

---

(1) Not tested in production; limits are based on characterization data

Electrical Characteristics (continued)

T_A = 25°C, over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OFF}	Current control constant off time	TOFF_SEL = GND		20		µs
		TOFF_SEL = Hi-Z		10		
		TOFF_SEL = VINT		30		
PROTECTION CIRCUITS						
V_{UVLO}	VM undervoltage lockout	VM falling; UVLO report			2.9	V
		VM rising; UVLO recovery			3	
I_{OCP}	Overcurrent protection trip level		2			A
t_{OCP}	Overcurrent deglitch time			2.8		µs
t_{RETRY}	Overcurrent protection period			1.6		ms
T_{TSD}	Thermal shutdown temperature	Die temperature T_J	150	160	180	°C
T_{HYS}	Thermal shutdown hysteresis	Die temperature T_J		50		°C

7.6 Timing Requirements

T_A = 25°C, over recommended operating conditions unless otherwise noted

NO.	PARAMETER		MIN	MAX	UNIT
1	f_{STEP}	Step frequency		250	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	1.9		µs
3	$t_{WL(STEP)}$	Pulse duration, STEP low	1.9		µs
4	$t_{SU(STEP)}$	Setup time, DIR or Mx to STEP rising	200		ns
5	$t_{H(STEP)}$	Hold time, DIR or Mx to STEP rising	200		ns

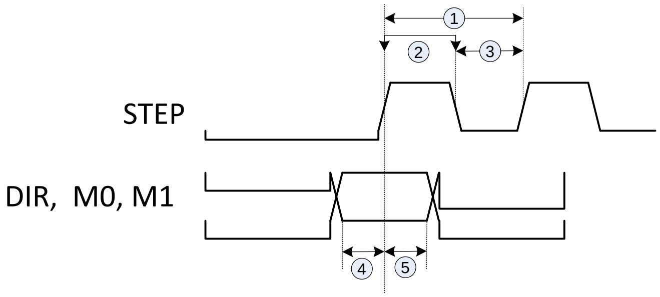


Figure 1. Timing Diagram

7.7 Typical Characteristics

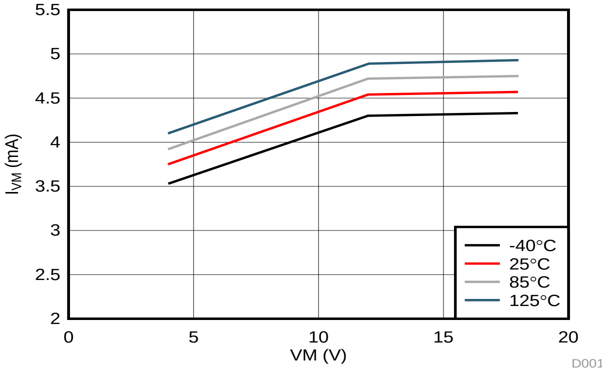


Figure 2. I_{VM} vs VM

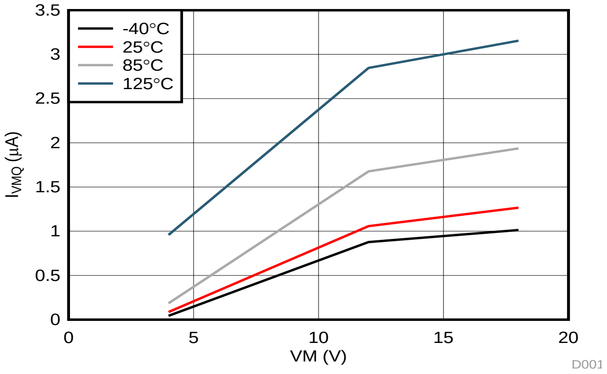


Figure 3. I_{VMQ} vs VM

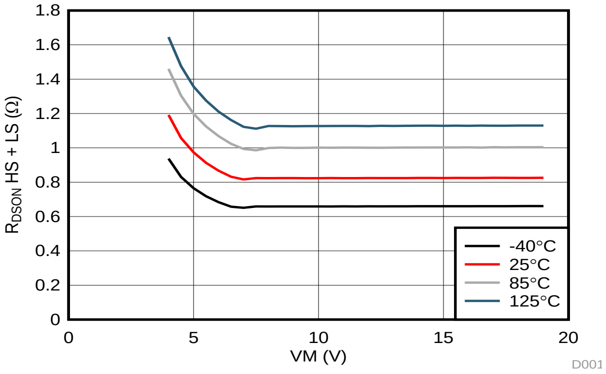


Figure 4. R_{DSON} vs VM

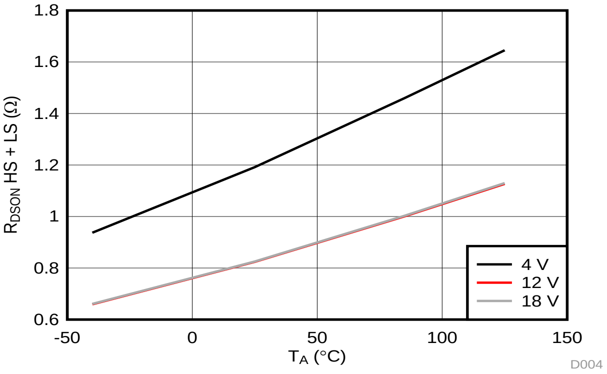


Figure 5. R_{DSON} vs Temperature

8 Detailed Description

8.1 Overview

The DRV8846 is an integrated motor driver solution for bipolar stepper motors. The device integrates 2 H-bridges that use NMOS low-side drivers and PMOS high-side drivers, current sense regulation circuitry, and a microstepping indexer. The DRV8846 can be powered with a supply range between 4 to 18 V and is capable of providing an output current to 1.4-A full scale or 1-A rms.

A simple STEP/DIR interface allows easy interfacing to the controller circuit. The internal indexer is able to execute high-accuracy microstepping without requiring the processor to control the current level.

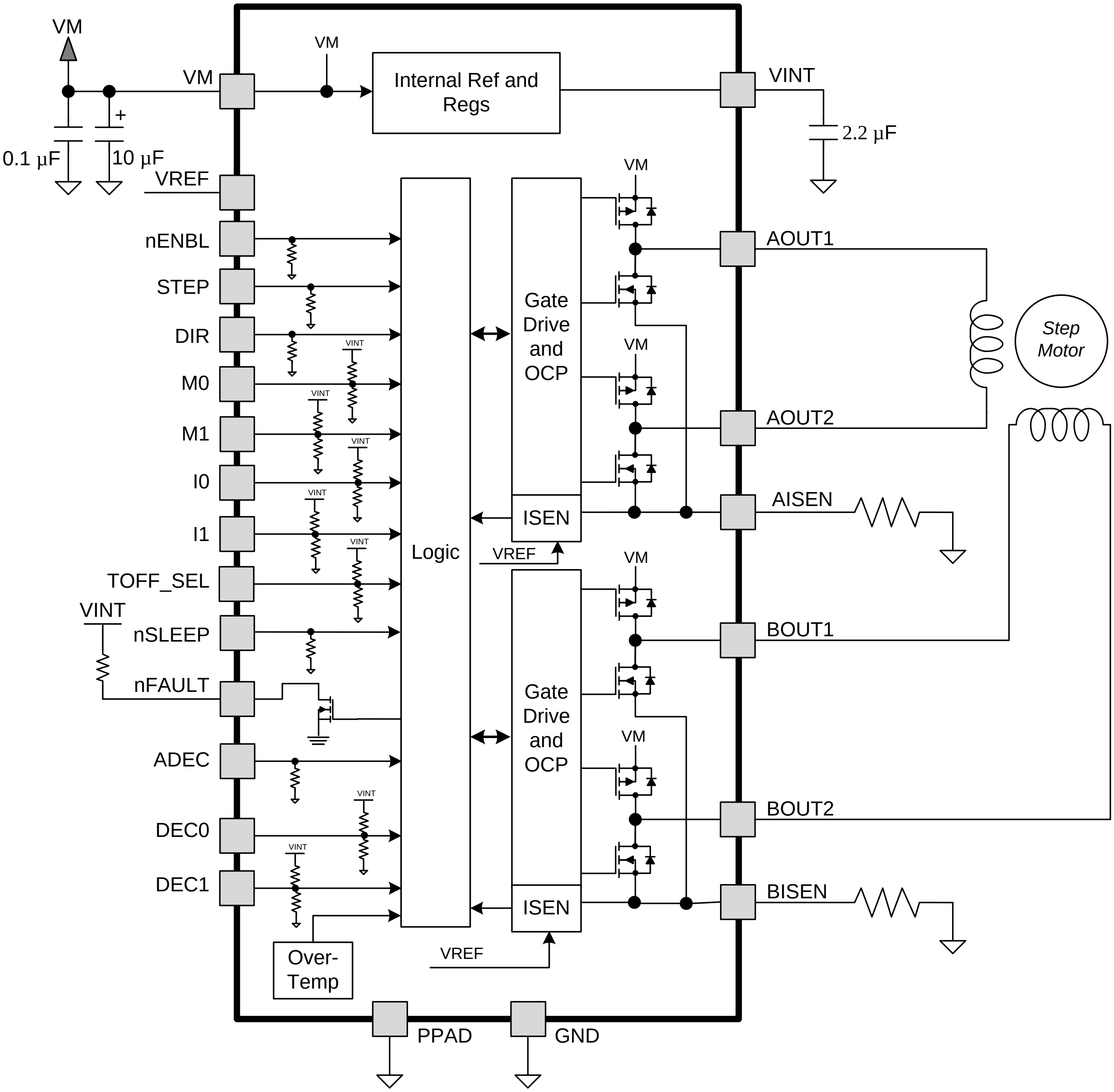
The PWM off-time, t_{OFF} can be adjusted to 10, 20, or 30 µs.

The DRV8846 has an adaptive decay feature that automatically adjusts the decay setting to minimize current ripple while still reacting quickly to step changes. This feature allows the DRV8846 to quickly be integrated into a system.

A torque DAC feature allows the controller to scale the output current without needing to scale the analog reference voltage input VREF. The torque DAC is accessed using digital input pins. This allows the controller to save power by decreasing the current consumption when not required.

A low-power sleep mode is included, which allows the system to save power when not driving the motor.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 PWM Motor Drivers

DRV8846 contains two identical H-bridge motor drivers with current-control PWM circuitry. Figure 6 shows a block diagram of the circuitry.

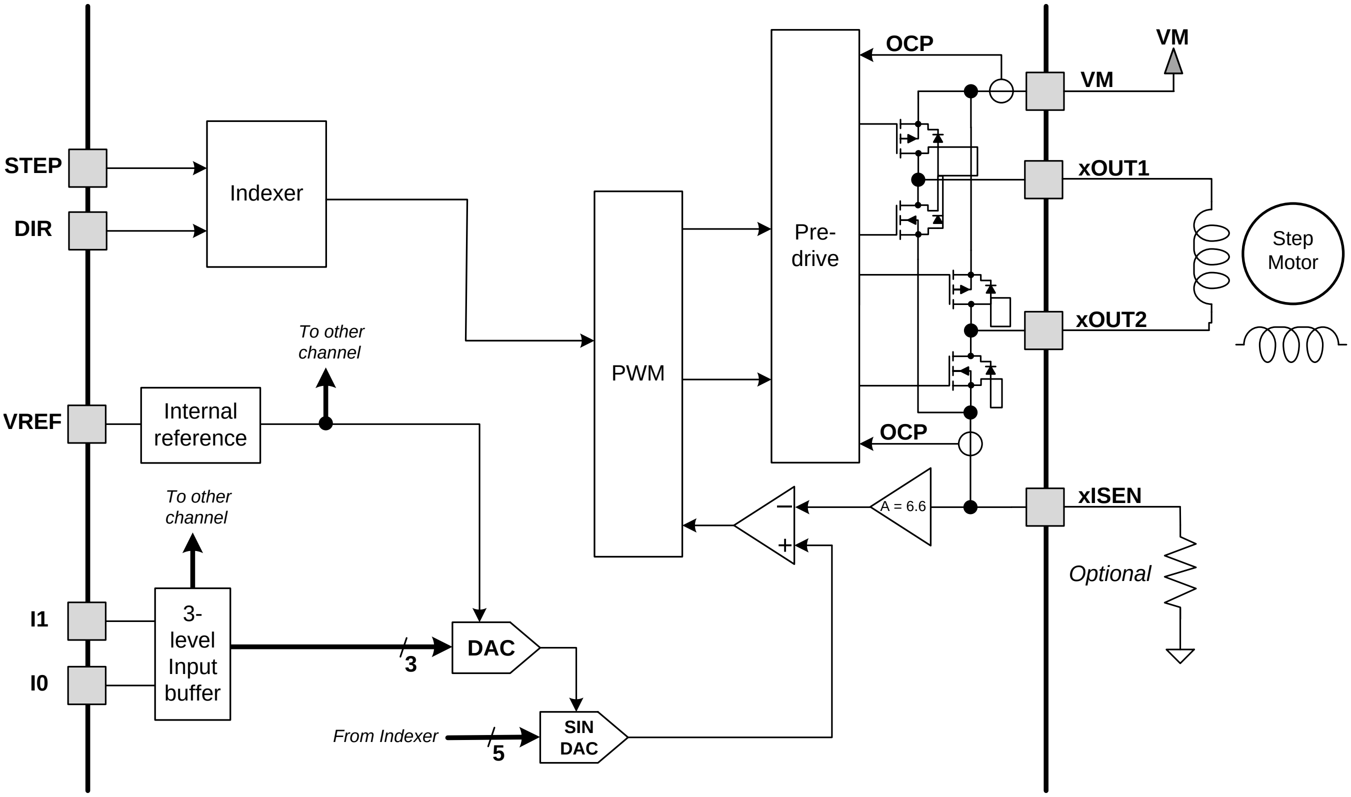


Figure 6. PWM Motor Driver Circuitry

8.3.2 Micro-Stepping Indexer

To allow a simple step and direction interface to control stepper motors, the DRV8846 contains a microstepping indexer. The indexer controls the state of the H-bridges automatically. When the correct transition is applied at the STEP input, the indexer moves to the next step, according to the direction set by the DIR pin. In 1/8, 1/16, and 1/32 step modes, both the rising and falling edges of the STEP input may be used to advance the indexer, depending on the M0 / M1 setting.

The nENBL pin disables the output stage in indexer mode. When nENBL = 0, the indexer inputs are still active and respond to the STEP and DIR input pins; only the output stage is disabled.

The indexer logic in the DRV8846 allows a number of different stepping configurations. The M0 and M1 pins configure the stepping format (see Table 2).

Table 2. Step Mode Settings

M1	M0	STEP MODE
0	0	Full step (2-phase excitation), rising-edge only
0	Z	1/2 step (1-2 phase excitation), rising-edge only
0	1	1/4 step (W1-2 phase excitation), rising-edge only
Z	0	8 microsteps/step, rising-edge only
Z	Z	8 microsteps/step, rising and falling edges
Z	1	16 microsteps/step, rising-edge only
1	0	16 microsteps/step, rising and falling edges
1	Z	32 microsteps/step, rising-edge only
1	1	32 microsteps/step, rising and falling edges

Note that the M0 and M1 pins are tri-level inputs. These pins can be driven logic low, logic high, or high-impedance (Z), like the I0 and I1 pins described previously.

For 1/8, 1/16, and 1/32-step modes, selections are available to advance the indexer only on the rising edge of the STEP input, or on both the rising and falling edges.

The step mode may be changed on-the-fly while the motor is moving. The indexer advances to the next valid state for the new M0 / M1 setting at the next rising edge of STEP.

The home state is 45°. The indexer enters the home state after power-up, after exiting UVLO, or after exiting sleep mode (see the yellow-shaded cells in Table 3 also indicated with a table note).

Table 3 shows the relative current and step directions for different step mode settings. At each rising edge of the STEP input, the indexer travels to the next state in the table. The direction is shown with the DIR pin high; if the DIR pin is low, the sequence is reversed. Positive current is defined as xOUT1 = positive with respect to xOUT2.

Table 3. Relative Current and Step Directions

1/32 STEP	1/16 STEP	1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 70%	WINDING CURRENT A	WINDING CURRENT B	ELECTRICAL ANGLE
1	1	1	1	1		100%	0%	0
2						100%	5%	3
3	2					100%	10%	6
4						99%	15%	8
5	3	2				98%	20%	11
6						97%	24%	14
7	4					96%	29%	17
8						94%	34%	20
9	5	3	2			92%	38%	23
10						90%	43%	25
11	6					88%	47%	28
12						86%	51%	31
13	7	4				83%	56%	34
14						80%	60%	37
15	8					77%	63%	39
16						74%	67%	42
17(1)	9(1)	5(1)	3(1)	2(1)	1(1)	71%	71%	45
18						67%	74%	48
19	10					63%	77%	51
20						60%	80%	53
21	11	6				56%	83%	56
22						51%	86%	59

(1) The indexer enters the home state after power-up, after exiting UVLO, or after exiting sleep mode.

Table 3. Relative Current and Step Directions (continued)

1/32 STEP	1/16 STEP	1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 70%	WINDING CURRENT A	WINDING CURRENT B	ELECTRICAL ANGLE
23	12					47%	88%	62
24						43%	90%	65
25	13	7	4			38%	92%	68
26						34%	94%	70
27	14					29%	96%	73
28						24%	97%	76
29	15	8				20%	98%	79
30						15%	99%	82
31	16					10%	100%	84
32						5%	100%	87
33	17	9	5	3		0%	100%	90
34						–5%	100%	93
35	18					–10%	100%	96
36						–15%	99%	98
37	19	10				–20%	98%	101
38						–24%	97%	104
39	20					–29%	96%	107
40						–34%	94%	110
41	21	11	6			–38%	92%	113
42						–43%	90%	115
43	22					–47%	88%	118
44						–51%	86%	121
45	23	12				–56%	83%	124
46						–60%	80%	127
47	24					–63%	77%	129
48						–67%	74%	132
49	25	13	7	4	2	–71%	71%	135
50						–74%	67%	138
51	26					–77%	63%	141
52						–80%	60%	143
53	27	14				–83%	56%	146
54						–86%	51%	149
55	28					–88%	47%	152
56						–90%	43%	155
57	29	15	8			–92%	38%	158
58						–94%	34%	160
59	30					–96%	29%	163
60						–97%	24%	166
61	31	16				–98%	20%	169
62						–99%	15%	172
63	32					–100%	10%	174
64						–100%	5%	177
65	33	17	9	5		–100%	0%	180
66						–100%	–5%	183
67	34					–100%	–10%	186
68						–99%	–15%	188
69	35	18				–98%	–20%	191

Table 3. Relative Current and Step Directions (continued)

1/32 STEP	1/16 STEP	1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 70%	WINDING CURRENT A	WINDING CURRENT B	ELECTRICAL ANGLE
70						–97%	–24%	194
71	36					–96%	–29%	197
72						–94%	–34%	200
73	37	19	10			–92%	–38%	203
74						–90%	–43%	205
75	38					–88%	–47%	208
76						–86%	–51%	211
77	39	20				–83%	–56%	214
78						–80%	–60%	217
79	40					–77%	–63%	219
80						–74%	–67%	222
81	41	21	11	6	3	–71%	–71%	225
82						–67%	–74%	228
83	42					–63%	–77%	231
84						–60%	–80%	233
85	43	22				–56%	–83%	236
86						–51%	–86%	239
87	44					–47%	–88%	242
88						–43%	–90%	245
89	45	23	12			–38%	–92%	248
90						–34%	–94%	250
91	46					–29%	–96%	253
92						–24%	–97%	256
93	47	24				–20%	–98%	259
94						–15%	–99%	262
95	48					–10%	–100%	264
96						–5%	–100%	267
97	49	25	13	7		0%	–100%	270
98						5%	–100%	273
99	50					10%	–100%	276
100						15%	–99%	278
101	51	26				20%	–98%	281
102						24%	–97%	284
103	52					29%	–96%	287
104						34%	–94%	290
105	53	27	14			38%	–92%	293
106						43%	–90%	295
107	54					47%	–88%	298
108						51%	–86%	301
109	55	28				56%	–83%	304
110						60%	–80%	307
111	56					63%	–77%	309
112						67%	–74%	312
113	57	29	15	8	4	71%	–71%	315
114						74%	–67%	318
115	58					77%	–63%	321
116						80%	–60%	323

Table 3. Relative Current and Step Directions (continued)

1/32 STEP	1/16 STEP	1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 70%	WINDING CURRENT A	WINDING CURRENT B	ELECTRICAL ANGLE
117	59	30				83%	–56%	326
118						86%	–51%	329
119	60					88%	–47%	332
120						90%	–43%	335
121	61	31	16			92%	–38%	338
122						94%	–34%	340
123	62					96%	–29%	343
124						97%	–24%	346
125	63	32				98%	–20%	349
126						99%	–15%	352
127	64					100%	–10%	354
128						100%	–5%	357

8.3.3 Current Regulation

The current through the motor windings is regulated by an adjustable fixed-off-time PWM current regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. After the current reaches the current chopping threshold, the bridge enters a decay mode for a fixed period of time to decrease the current, which is configurable between 10 to 30 µs through the tri-level input TOFF_SEL. After the time expires, the bridge is re-enabled, starting another PWM cycle.

Table 4. Fixed Off-Time Selection

TOFF_SEL	TOFF Duration
0	20 µs
Z	10 µs
1	30 µs

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISEN pin, with a reference voltage. The reference voltage can be supplied by an internal reference of 3.3 V (which requires VINT to be connected to VREF), or externally supplied to the VREF pin. The reference voltage is then scaled first by the 3-bit torque DAC, then by the output of a sine lookup table that is applied to a sine-weighted DAC (sine DAC). The voltage is attenuated by a factor of 6.6.

The full-scale (100%) chopping current is calculated as follows:

$$I_{FS} = \frac{\mathrm{VREF}}{6.6 \times R_{ISENSE}} \times \mathrm{TORQUE}$$

where

- I_{FS} is the full scale regulated current
- VREF is the voltage on the VREF pin
- R_{ISENSE} is the resistance of the sense resistor
- TORQUE is the scaling percentage from the torque DAC. (1)

Example: Using VREF is 3.3 V, torque DAC = 100%, and a 500-mΩ sense resistor, the full-scale chopping current is 3.3 V / (6.6 × 500 mΩ) × 100% = 1 A.

The current for both motor windings is scaled depending on the I0 and I1 pins, which drive a 3-bit linear DAC, as in Table 5.

Table 5. Torque DAC Settings

I1	I0	CURRENT SCALING (TORQUE)
0	0	100%
0	Z	87.5%
0	1	75%
Z	0	62.5%
Z	Z	50%
Z	1	37.5%
1	0	25%
1	Z	12.5%
1	1	0% (outputs disabled)

Table 6 gives the xISEN trip voltage at a given DAC code and I[1:0] setting.

Table 6. Torque DAC xISENS Trip Levels (VREF = 3.3 V)

Sine DAC Code	Torque DAC I[1:0] Setting							
	00 - 100%	0Z - 87.5%	01 - 75%	Z0 - 62.5%	ZZ - 50%	Z1 - 37.5%	10 - 25%	1Z - 12.5%
31	500 mV	438 mV	375 mV	313 mV	250 mV	188 mV	125 mV	63 mV
30	500 mV	438 mV	375 mV	313 mV	250 mV	188 mV	125 mV	63 mV
29	495 mV	433 mV	371 mV	309 mV	248 mV	186 mV	124 mV	62 mV
28	490 mV	429 mV	368 mV	306 mV	245 mV	184 mV	123 mV	61 mV
27	485 mV	424 mV	364 mV	303 mV	243 mV	182 mV	121 mV	61 mV
26	480 mV	420 mV	360 mV	300 mV	240 mV	180 mV	120 mV	60 mV
25	470 mV	411 mV	353 mV	294 mV	235 mV	176 mV	118 mV	59 mV
24	460 mV	403 mV	345 mV	288 mV	230 mV	173 mV	115 mV	58 mV
23	450 mV	394 mV	338 mV	281 mV	225 mV	169 mV	113 mV	56 mV
22	440 mV	385 mV	330 mV	275 mV	220 mV	165 mV	110 mV	55 mV
21	430 mV	376 mV	323 mV	269 mV	215 mV	161 mV	108 mV	54 mV
20	415 mV	363 mV	311 mV	259 mV	208 mV	156 mV	104 mV	52 mV
19	400 mV	350 mV	300 mV	250 mV	200 mV	150 mV	100 mV	50 mV
18	385 mV	337 mV	289 mV	241 mV	193 mV	144 mV	96 mV	48 mV
17	370 mV	324 mV	278 mV	231 mV	185 mV	139 mV	93 mV	46 mV
16	355 mV	311 mV	266 mV	222 mV	178 mV	133 mV	89 mV	44 mV
15	335 mV	293 mV	251 mV	209 mV	168 mV	126 mV	84 mV	42 mV
14	315 mV	276 mV	236 mV	197 mV	158 mV	118 mV	79 mV	39 mV
13	300 mV	263 mV	225 mV	188 mV	150 mV	113 mV	75 mV	38 mV
12	280 mV	245 mV	210 mV	175 mV	140 mV	105 mV	70 mV	35 mV
11	255 mV	223 mV	191 mV	159 mV	128 mV	96 mV	64 mV	32 mV
10	235 mV	206 mV	176 mV	147 mV	118 mV	88 mV	59 mV	29 mV
9	215 mV	188 mV	161 mV	134 mV	108 mV	81 mV	54 mV	27 mV
8	190 mV	166 mV	143 mV	119 mV	95 mV	71 mV	48 mV	24 mV
7	170 mV	149 mV	128 mV	106 mV	85 mV	64 mV	43 mV	21 mV
6	145 mV	127 mV	109 mV	91 mV	73 mV	54 mV	36 mV	18 mV
5	120 mV	105 mV	90 mV	75 mV	60 mV	45 mV	30 mV	15 mV
4	100 mV	88 mV	75 mV	63 mV	50 mV	38 mV	25 mV	13 mV
3	75 mV	66 mV	56 mV	47 mV	38 mV	28 mV	19 mV	9 mV
2	50 mV	44 mV	38 mV	31 mV	25 mV	19 mV	13 mV	6 mV
1	25 mV	22 mV	19 mV	16 mV	13 mV	9 mV	6 mV	3 mV
0	0 mV	0 mV	0 mV	0 mV	0 mV	0 mV	0 mV	0 mV

8.3.4 Decay Mode

After the chopping current threshold is reached, the drive current is interrupted, but due to the inductive nature of the motor, current must continue to flow for some period of time (called recirculation current). To handle this recirculation current, the H-bridge can operate in two different states, fast decay or slow decay (or a mixture of fast and slow decay).

In fast-decay mode, after the PWM chopping current level is reached, the H-bridge reverses state to allow winding current to flow through the opposing FETs. As the winding current approaches 0, the bridge is disabled to prevent any reverse current flow. For fast-decay mode, see number 2 in Figure 7.

In slow-decay mode, winding current is recirculated by enabling both of the low-side FETs in the bridge. For slow-decay mode, see number 3 in Figure 7.

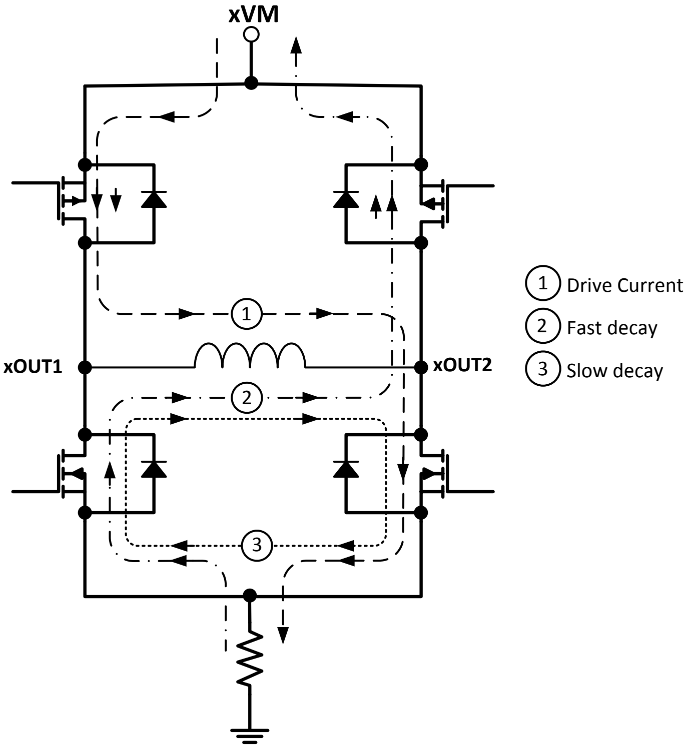


Figure 7. Decay Modes

The DRV8846 supports fast, slow, mixed, and adaptive decay modes. With stepper motors, the decay mode is chosen for a given stepper motor and operating conditions to minimize mechanical noise and vibration.

In mixed decay mode, the current recirculation begins as fast decay, but at a fixed period of time (determined by the state of the DEC1 and DEC0 pins shown in Table 7) the current recirculation switches to slow decay mode for the remainder of the fixed PWM period. Note that the DEC1 and DEC0 pins are tri-level inputs; these pins can be driven logic low, logic high, or high-impedance (Z).

Figure 8 shows the current waveforms in slow, fast, and 25% and 1 t_{BLANK} mixed decay modes.

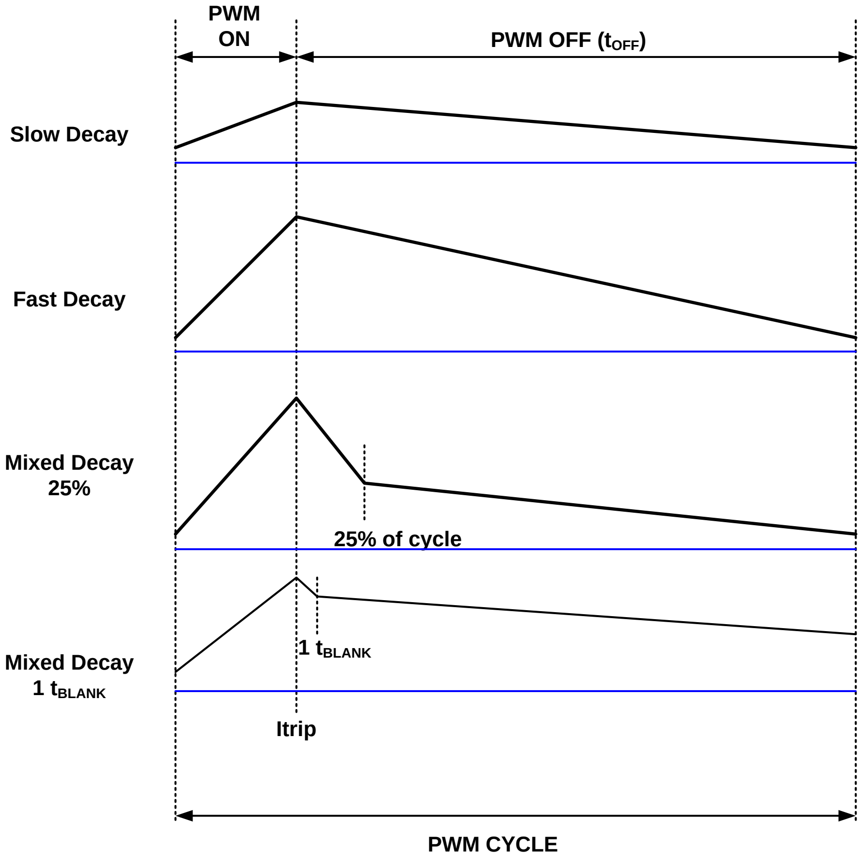


Figure 8. Decay Behavior

Table 7. Decay Pins Configuration

DEC1	DEC0	Decay Mode (Increasing Current)	Decay Mode (Decreasing Current)
0	0	Slow decay	Slow decay
0	Z	Slow decay	Mixed decay: 25% fast
0	1	Slow decay	Mixed decay: 1 t_{BLANK}
Z	0	Mixed decay: 1 t_{BLANK}	Mixed decay: 1 t_{BLANK}
Z	Z	Mixed decay: 50% fast	Mixed decay: 50% fast
Z	1	Mixed decay: 25% fast	Mixed decay: 25% fast
1	0	Slow decay	Mixed decay: 50% fast
1	Z	Slow decay	Mixed decay: 12.5% fast
1	1	Slow decay	Fast decay

Figure 9 shows increasing and decreasing current. When current is decreasing, the decay mode used is fast, slow, or mixed as commanded by the DEC1 and DEC0 pins. Three DEC pin selections allow for mixed decay during increasing current.

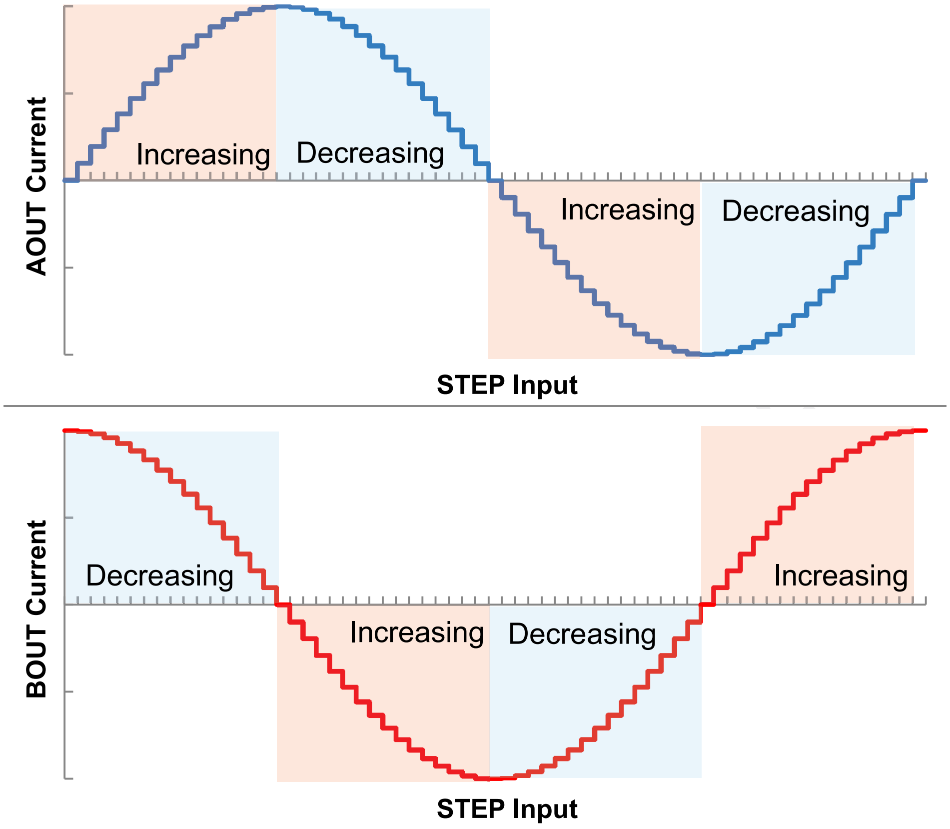


Figure 9. Increasing and Decreasing Current

Adaptive decay mode simplifies the decay mode selection by dynamically changing to adjust for current level, step change, supply variation, BEMF, and load. To enable adaptive decay mode, pull the ADEC pin to logic high and pull DEC0 and DEC1 pins to logic high. The state of the ADEC pin is only evaluated when exiting sleep mode.

Adaptive decay adjusts the time spent in fast decay to minimize current ripple and quickly adjust to current-step changes. If the drive time is longer than the minimum (t_{BLANK}), in order to reach the current trip point, the decay mode applied is slow decay (see Figure 10).

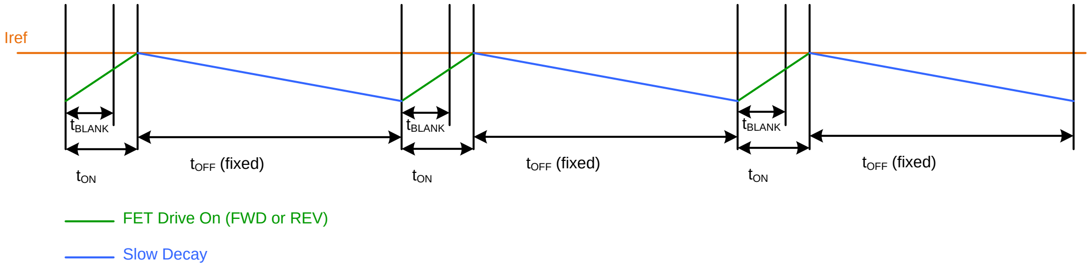


Figure 10. Adaptive Decay – Slow Decay Operation

When the minimum drive time (t_{BLANK}) provides more current than the regulation point, fast decay of 1- t_{BLANK} is applied. If the second drive period also provides more current than the regulation point, fast decay of 2 t_{BLANK} is applied. If a third (or more) consecutive period provides more current than the regulation point, fast decay using 25% of t_{OFF} time is applied. When the minimum drive time is insufficient to reach the current regulation level, slow decay is applied until the current exceeds the current reference level (see Figure 11).

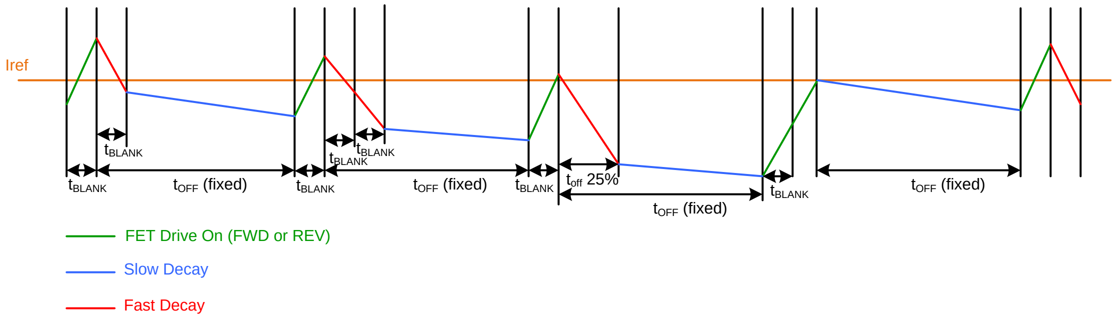


Figure 11. Adaptive Decay – Mixed Decay Operation

Figure 12 shows a case for adaptive decay where a step occurs. The system starts with 1 t_{BLANK} of fast decay and works up to 25% of t_{OFF} time for fast decay until the current is regulated again.

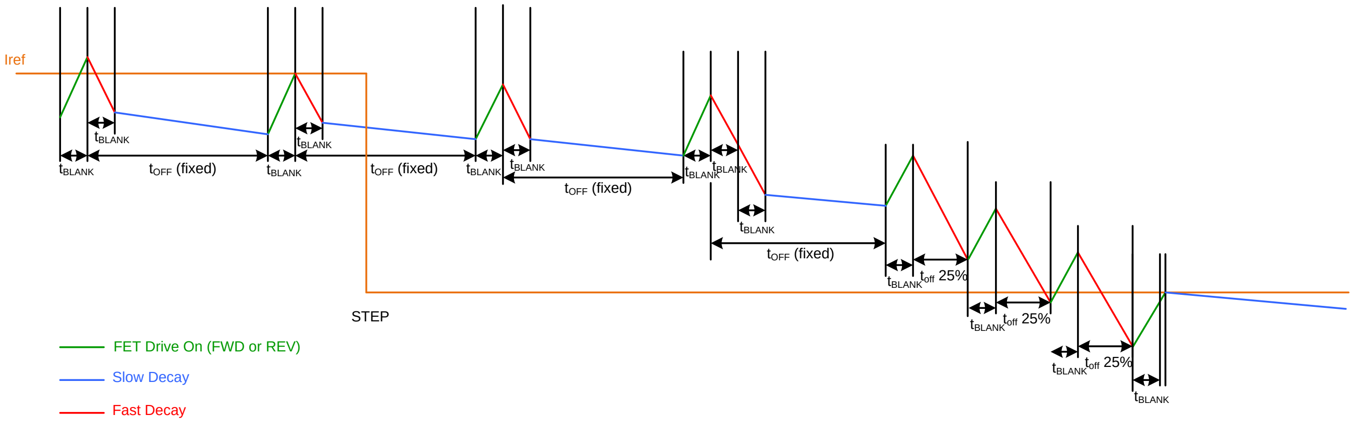


Figure 12. Adaptive Decay – Step Operation

8.3.5 Blanking Time

After the current is enabled in an H-bridge, the voltage on the xISEN pin is ignored for a period of time before enabling the current sense circuitry. Note that the blanking time also sets the minimum drive time of the PWM.

The time, t_{BLANK}, is determined by the sine DAC code and the torque DAC setting. The timing information for t_{BLANK} is given in Table 8.

Table 8. t_{BLANK} Settings

Sine DAC Code	**Torque DAC I[1:0] Setting**							
	00 - 100%	**0Z - 87.5%**	**01 - 75%**	**Z0 - 62.5%**	**ZZ - 50%**	**Z1 - 37.5%**	**10 - 25%**	**1Z - 12.5%**
31	1.80 µs	1.80 µs	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	0.90 µs
30	1.80 µs	1.80 µs	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	0.90 µs
29	1.80 µs	1.80 µs	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	0.90 µs
28	1.80 µs	1.80 µs	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	0.90 µs
27	1.80 µs	1.80 µs	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	0.90 µs
26	1.80 µs	1.80 µs	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	0.90 µs
25	1.80 µs	1.80 µs	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	0.90 µs
24	1.80 µs	1.80 µs	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	0.90 µs
23	1.80 µs	1.80 µs	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	0.90 µs
22	1.80 µs	1.80 µs	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	0.90 µs
21	1.80 µs	1.80 µs	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	0.90 µs
20	1.80 µs	1.80 µs	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	0.90 µs
19	1.80 µs	1.80 µs	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	0.90 µs
18	1.80 µs	1.80 µs	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	0.90 µs
17	1.80 µs	1.80 µs	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	0.90 µs
16	1.80 µs	1.80 µs	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	0.90 µs
15	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	1.20 µs	0.90 µs	0.90 µs
14	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	1.20 µs	0.90 µs	0.90 µs
13	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	1.20 µs	0.90 µs	0.90 µs
12	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	1.20 µs	0.90 µs	0.90 µs
11	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	1.20 µs	0.90 µs	0.90 µs
10	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	1.20 µs	0.90 µs	0.90 µs
9	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	1.20 µs	0.90 µs	0.90 µs
8	1.50 µs	1.50 µs	1.50 µs	1.20 µs	1.20 µs	1.20 µs	0.90 µs	0.90 µs
7	1.20 µs	1.20 µs	1.20 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs
6	1.20 µs	1.20 µs	1.20 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs
5	1.20 µs	1.20 µs	1.20 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs
4	1.20 µs	1.20 µs	1.20 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs
3	0.90 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs
2	0.90 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs
1	0.90 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs
0	0.90 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs	0.90 µs

8.3.6 Protection Circuits

The DRV8846 is fully protected against undervoltage, overcurrent, and overtemperature events.

8.3.6.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive. If this analog current limit persists for longer than the OCP deglitch time t_{OCP}, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. The device remains disabled until the retry time, t_{RETRY}, occurs. The OCP is independent for each H-bridge.

Overcurrent conditions are detected independently on both high-side and low-side devices; that is, a short to ground, supply, or across the motor winding all result in an OCP event. Note that OCP does not use the current sense circuitry used for PWM current control, so OCP functions without the presence of the xISEN resistors.

8.3.6.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. After the die temperature falls to a safe level, operation automatically resumes. The nFAULT pin is released after operation has resumed.

8.3.6.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the UVLO falling threshold voltage, V_{UVLO}, all circuitry in the device is disabled, and all internal logic is reset. Operation resumes when VM rises above the UVLO rising threshold. The nFAULT pin is driven low during an undervoltage condition and is released after operation has resumed.

Table 9. Fault Behavior

Fault	Error Report	H-Bridge	Internal Circuits	Recovery
VM UVLO	nFAULT unlatched	Disabled	Shut down	System and fault clears on recovery
OCP	nFAULT unlatched	Disabled	Operating	System and fault clears on recovery and motor is driven after time, t_{RETRY}
TSD	nFAULT unlatched	Disabled	Operating	System and fault clears on recovery

8.4 Device Functional Modes

The DRV8846 device is active unless the nSLEEP pin is driven low. In sleep mode, the VINT regulator is disabled and the H-bridge FETs are disabled (Hi-Z). The time t_{SLEEP} must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The DRV8846 is brought out of sleep mode by bringing the nSLEEP pin high. The time t_{WAKE} must elapse, after nSLEEP is brought high, before the outputs change state.

If the nENBL pin is brought high, the H-bridge outputs are disabled, but the internal logic is still active. An appropriate edge on STEP (depending on the step mode) advances the indexer, but the outputs do not change state until nENBL is driven low.

When VM falls below the VM UVLO threshold, V_{UVLO}, the output driver, internal logic, and VINT regulator are reset.

Table 10. Operating Modes

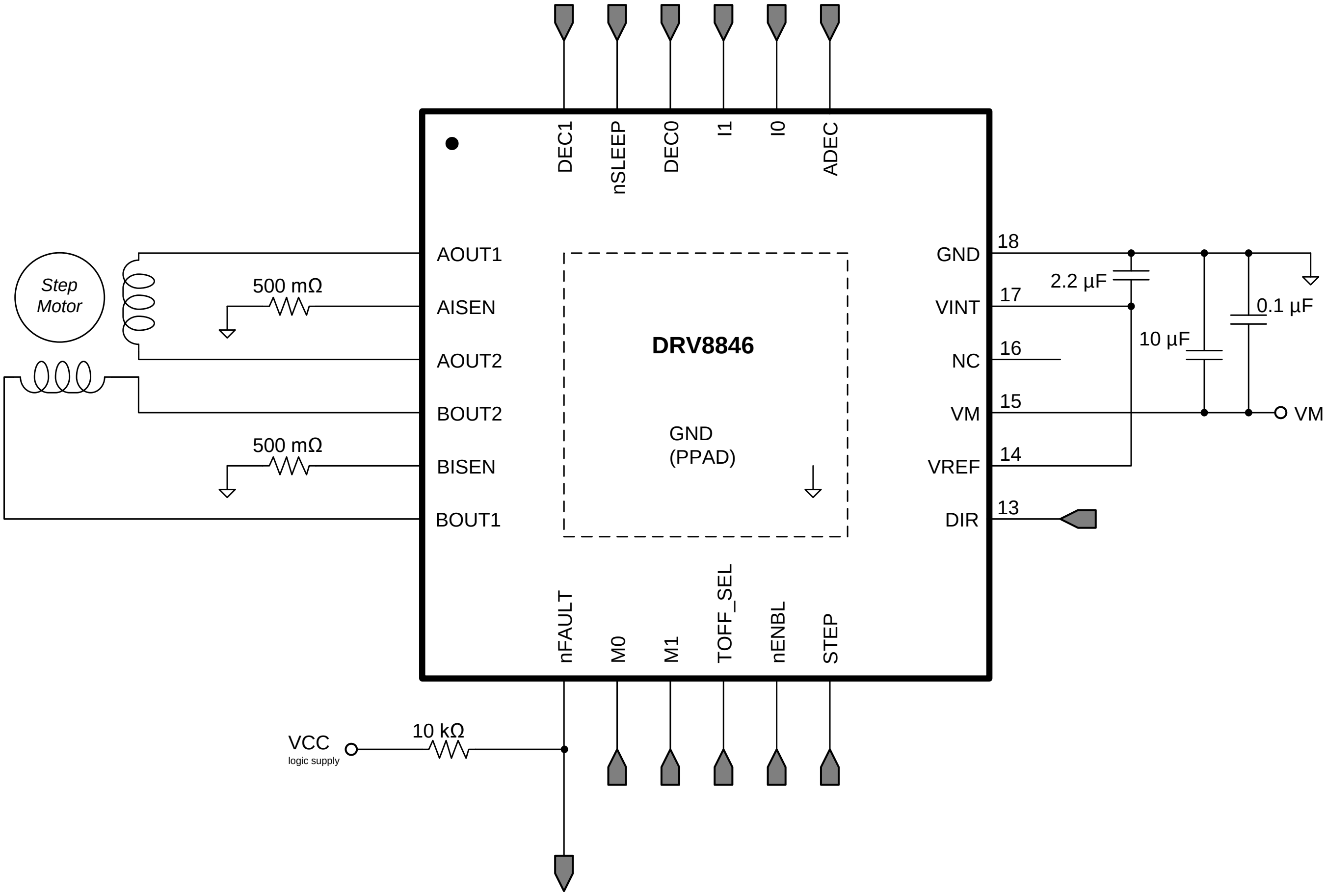
Mode	Condition	H-Bridge	VINT	Indexer
Operating	4 V < VM < 18 V nSLEEP pin = 1 nENBL = 0	Operating	Operating	Operating
Disabled	4 V < VM < 18 V nSLEEP pin = 1 nENBL = 1	Disabled	Operating	Operating
Sleep	4 V < VM < 18 V nSLEEP pin = 0	Disabled	Disabled	Disabled
Fault	Any fault condition met	Disabled	Depends on fault	Depends on fault

9 Application and Implementation

9.1 Application Information

The DRV8846 is used in stepper motor control. The following design procedure can be used to configure the DRV8846.

9.2 Typical Application



9.2.1 Design Requirements

Table 11 gives design input parameters for system design.

Table 11. System Design Input Parameters

Design Parameter	Reference	Example Value
Nominal supply voltage	VM	12 V
Supply voltage range		4 to 18 V
Motor winding resistance	R_L	3.0 Ω/phase
Motor winding inductance	L_L	330 µH/phase
Motor full step angle	θ_{step}	1.8°/step
Target stepping level	nm	1/8 step
Target motor speed	v	400 rpm
Target chopping current	I_{CHOP}	500 mA
Chopping current reference voltage	VREF	3.3 V
Current scaling	TORQUE	100%

9.2.2 Detailed Design Procedure

9.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8846 requires the desired motor speed and stepping level. The DRV8846 can support from full step to 1/32 step mode.

If the target motor speed is too high, the motor will not spin. Make sure that the motor can support the target speed.

For a desired motor speed (v), microstepping level (nm), and motor full step angle (θ_{step}),

$$f_{step}\ (\text{steps/ s}) = \frac{v(\text{rpm}) \times n_m(\text{steps}) \times 6}{\theta_{step}\ (^\circ / \text{step})} \tag{2}$$

θ_{step} can be found in the stepper motor data sheet or often written on the motor itself.

For DRV8846, the microstepping levels are set by the M0/M1 pins and can be any of the settings in Table 2. Higher microstepping means a smoother motor motion and less audible noise, but increases the switching losses and requires a higher f_{step} to achieve the same motor speed.

9.2.2.2 Current Regulation

The chopping current (I_{CHOP}) is the maximum current driven through either winding. This quantity will depend on the sense resistor value (R_{XISEN}).

$$I_{CHOP} = \frac{\text{VREF}}{6.6 \times R_{ISENSE}} \times \text{TORQUE} \tag{3}$$

I_{CHOP} is set by a comparator which compares the voltage across R_{XISEN} to a reference voltage. Note that I_{CHOP} must follow Equation 4 to avoid saturating the motor.

$$I_{CHOP}\ (\text{A}) < \frac{\text{VM (V)}}{R_L\ (\Omega) + 2 \times R_{DS(ON)}\ (\Omega) + R_{SENSE}\ (\Omega)}$$

where

- VM is the motor supply voltage.
- R_L is the motor winding resistance. (4)

9.2.2.3 Decay Modes

The DRV8846 supports four different decay modes: slow decay, fast decay, mixed decay, and adaptive decay. The first selection to try is the adaptive decay mode, which adjusts the decay mode automatically to improve current regulation. The current through the motor windings is regulated using a fixed-off-time PWM scheme. This means that after any drive phase, when a motor has reached the current chopping threshold (I_{CHOP}), the DRV8846 places the motor in one of the four decay modes until the PWM cycle has expired. Afterward, a new drive phase starts.

The blanking time, t_{BLANK}, defines the minimum drive time for the current chopping. I_{CHOP} is ignored during t_{BLANK}, so the winding current may overshoot the trip level during this blanking period.

9.2.3 Application Curves

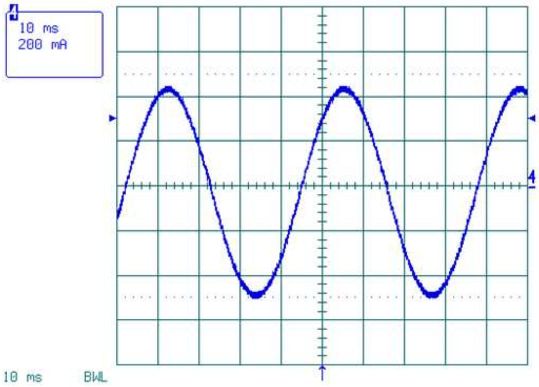


Figure 13. Microstepping Waveform, Phase A, Adaptive Decay

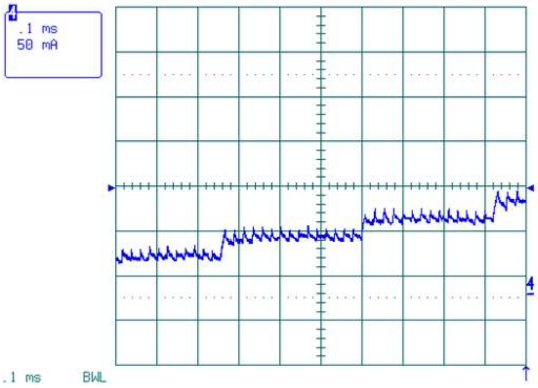


Figure 14. Microstepping Waveform, Adaptive Decay, Step Current Regulation

10 Power Supply Recommendations

The DRV8846 is designed to operate from an input voltage supply (VM) range between 4 and 18 V. A 0.1-µF ceramic capacitor rated for VM must be placed as close to the DRV8846 as possible. In addition, a bulk 10-µF capacitor must be included on VM.

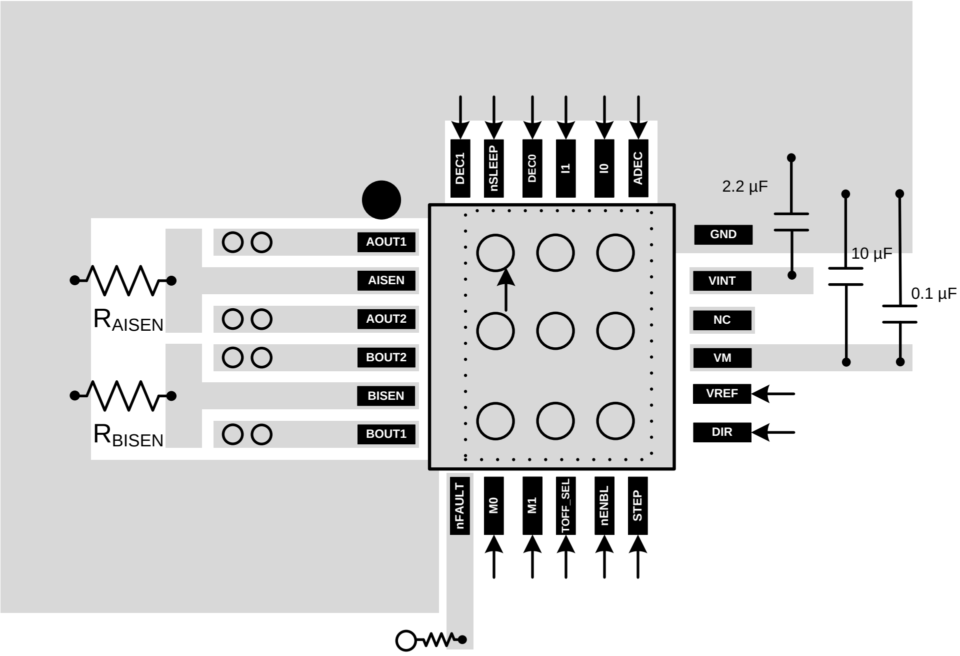
11 Layout

11.1 Layout Guidelines

The VM terminal should be bypassed to GND using a low-ESR ceramic bypass capacitor with a recommended value of 10 µF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin.

Bypass VINT to ground with a ceramic capacitor rated 6.3 V. Place this bypassing capacitor as close to the pin as possible.

11.2 Layout Example



12 Device and Documentation Support

12.1 Trademarks

PowerPAD is a trademark of Texas Instruments.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8846RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8846	Samples
DRV8846RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8846	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

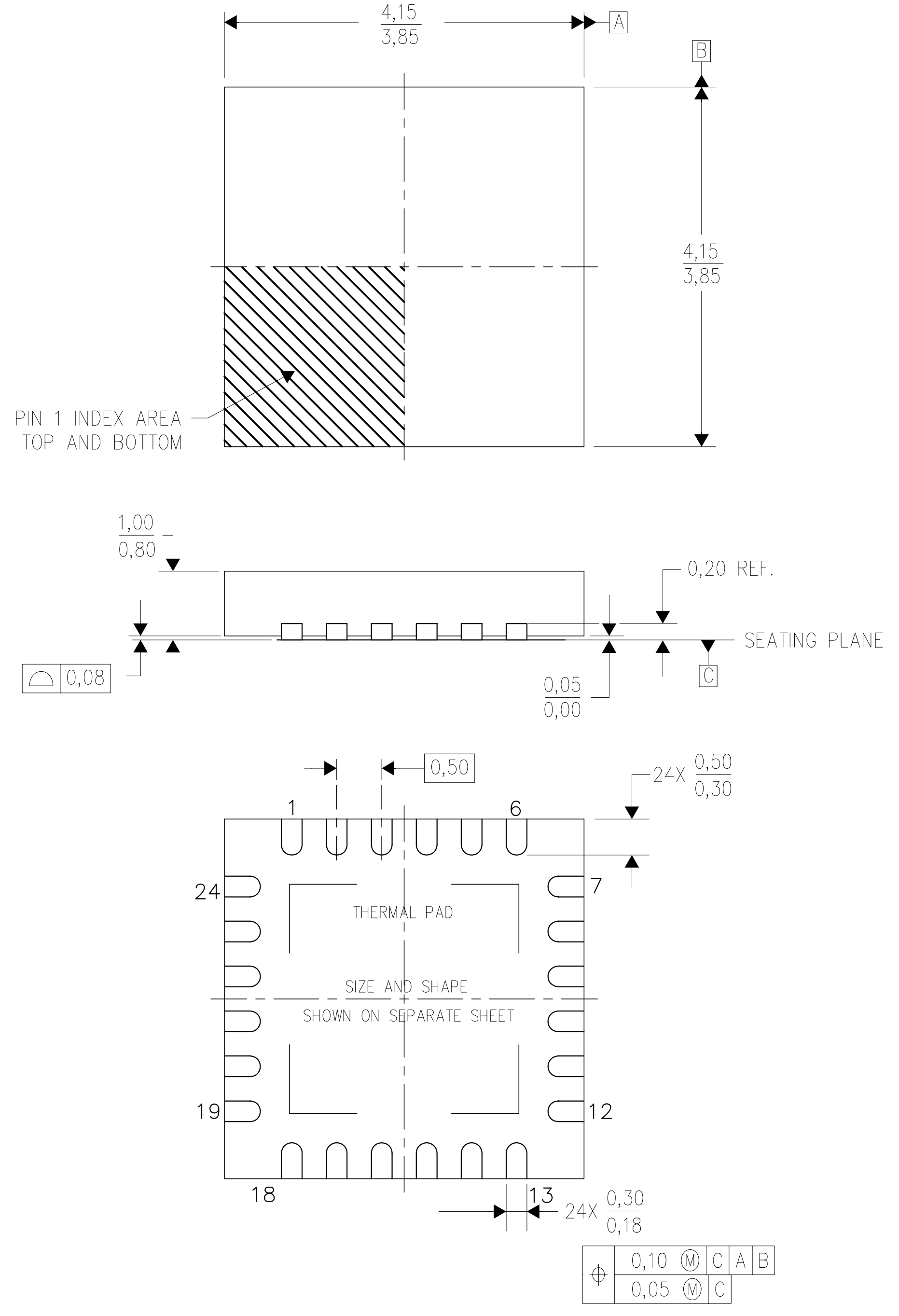
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



4204104/G 07/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No-Leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.

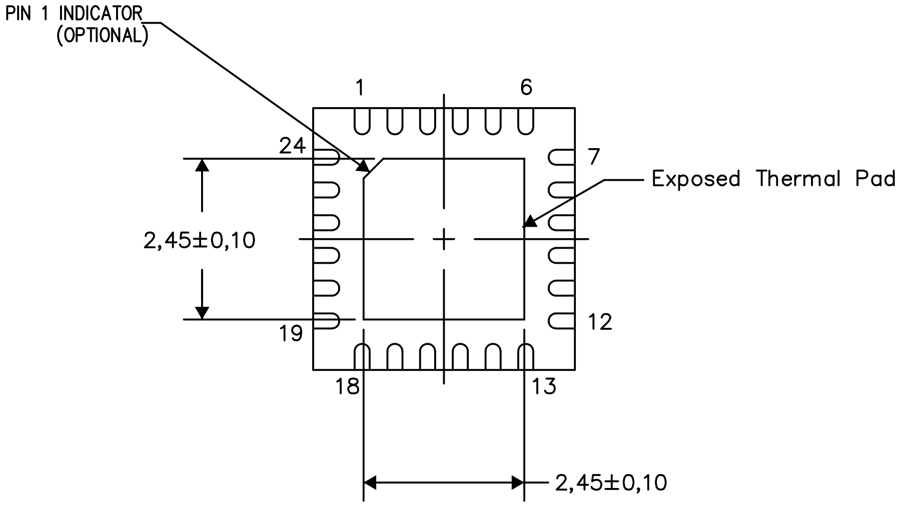
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



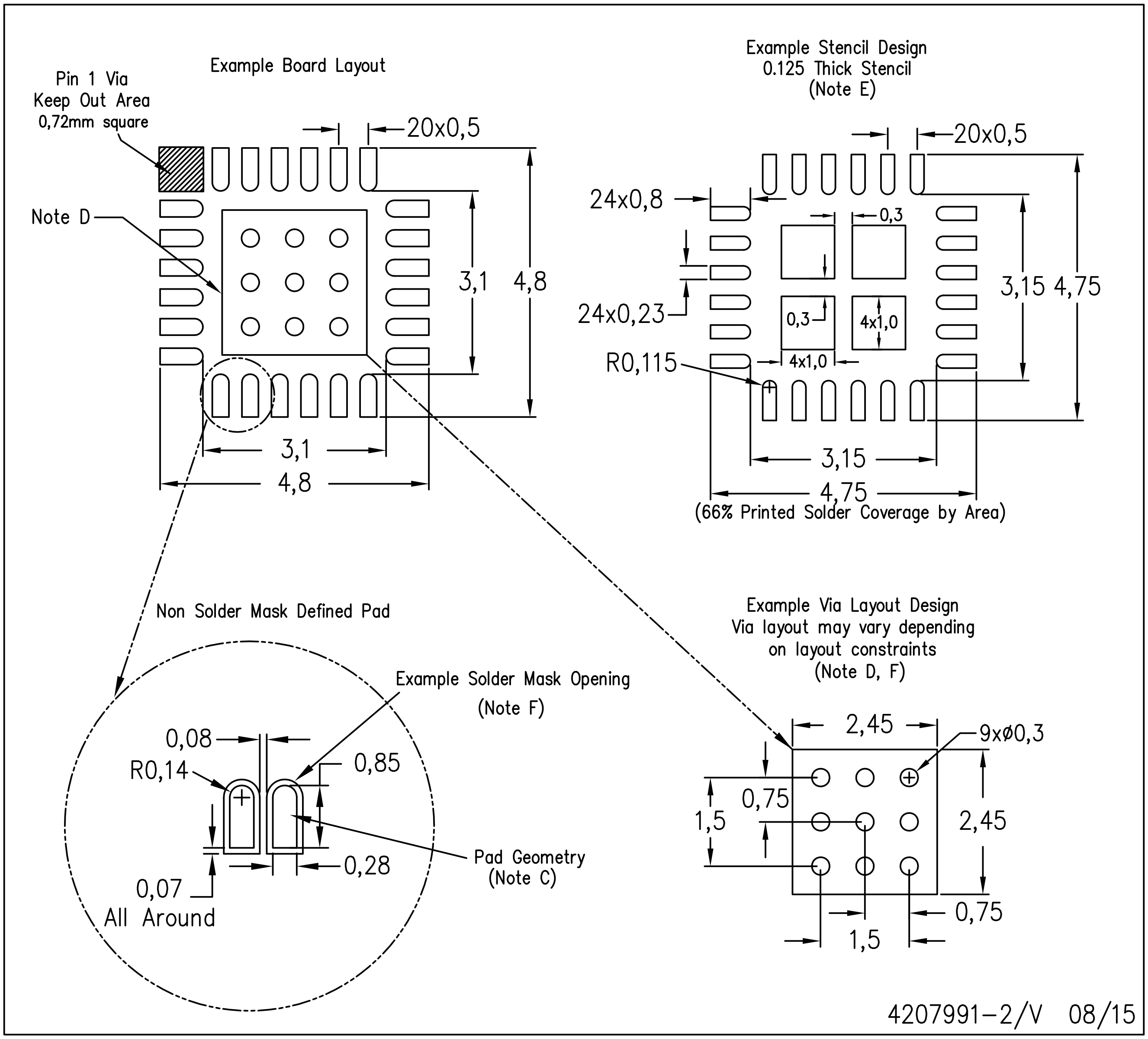
Bottom View

Exposed Thermal Pad Dimensions

4206344–3/AK 08/15

NOTES: A. All linear dimensions are in millimeters

RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Publication IPC-7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated (‘TI”) technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, “TI Resources”) are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI’s provision of TI Resources does not expand or otherwise alter TI’s applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED “AS IS” AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI’s standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated