Cool-Power®
ZVS Switching Regulators
PI3749-x0

16V to 34V_{IN}, 12V to 28V_{OUT}, 240W Cool-Power ZVS Buck-Boost

Product Description

The PI3749-x0 is high efficiency, wide range DC-DC ZVS Buck-Boost regulator. This high density System-in-Package (SiP) integrates controller, power switches, and support components. The integration of a high performance Zero-Voltage Switching (ZVS) topology, within the PI3749-x0, increases point of load performance providing best in class power efficiency. The PI3749-x0 requires an external inductor, resistive feedback divider and minimal capacitors to form a complete DC-DC switching mode buck-boost regulator.

The ZVS architecture also enables high frequency operation while minimizing switching losses and maximizing efficiency. The high switching frequency operation reduces the size of the external filtering components, improves power density, and enables very fast dynamic response to line and load transients.

Features & Benefits

- Up to 98.5% efficiency at 800kHz F_{SW}
- Up to 240W of continuous output power (for specific conditions)
- Fast transient response
- Parallel capable with single wire current sharing
- External frequency synchronization / interleaving
- High Side Current Sense Amplifier
- General Purpose Amplifier
- Input Over/Undervoltage Lockout (OVLO/UVLO)
- Output Overvoltage Protection (OVP)
- Overtemperature Protection (OTP)
- Fast and slow current limits
- -40°C to 115°C operating range (T_J)
- Excellent light load efficiency
- Optional I²C™ * functionality & programmability:
  - V_{OUT} margining
  - Fault reporting
  - Enable and SYNCI pin polarity

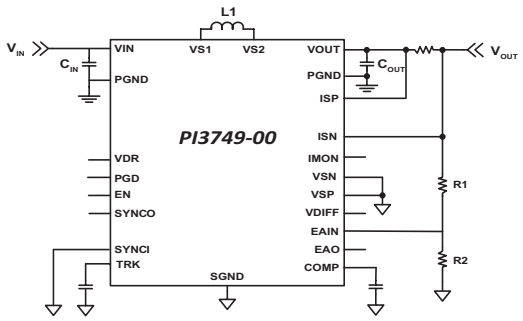
Applications

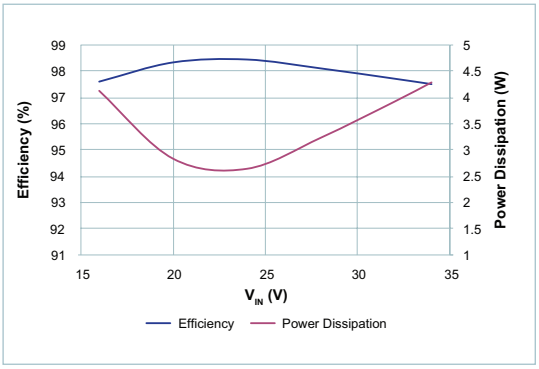
- Computing, Communications, Industrial
- Variable output step up/down voltage regulation

Package Information

- 10mm x 14mm x 2.56mm LGA SiP

Typical Application





* I²C™ is a trademark of NXP semiconductor

Contents

Order Information

Part Number	Description	Package	Transport Media	MFG
PI3749-00-LGIZ	$16V_{IN}$ to $34V_{IN}$ SiP	10mm x 14mm 108-pin LGA	TRAY	Vicor
PI3749-20-LGIZ	$16V_{IN}$ to $34V_{IN}$ SiP I^2C™ compatible	10mm x 14mm 108-pin LGA	TRAY	Vicor

Absolute Maximum Ratings

Note: Stresses beyond these limits may cause permanent damage to the device. Operation at these conditions or conditions beyond those listed in the Electrical Specifications table is not guaranteed. All voltage nodes are referenced to PGND unless otherwise noted.

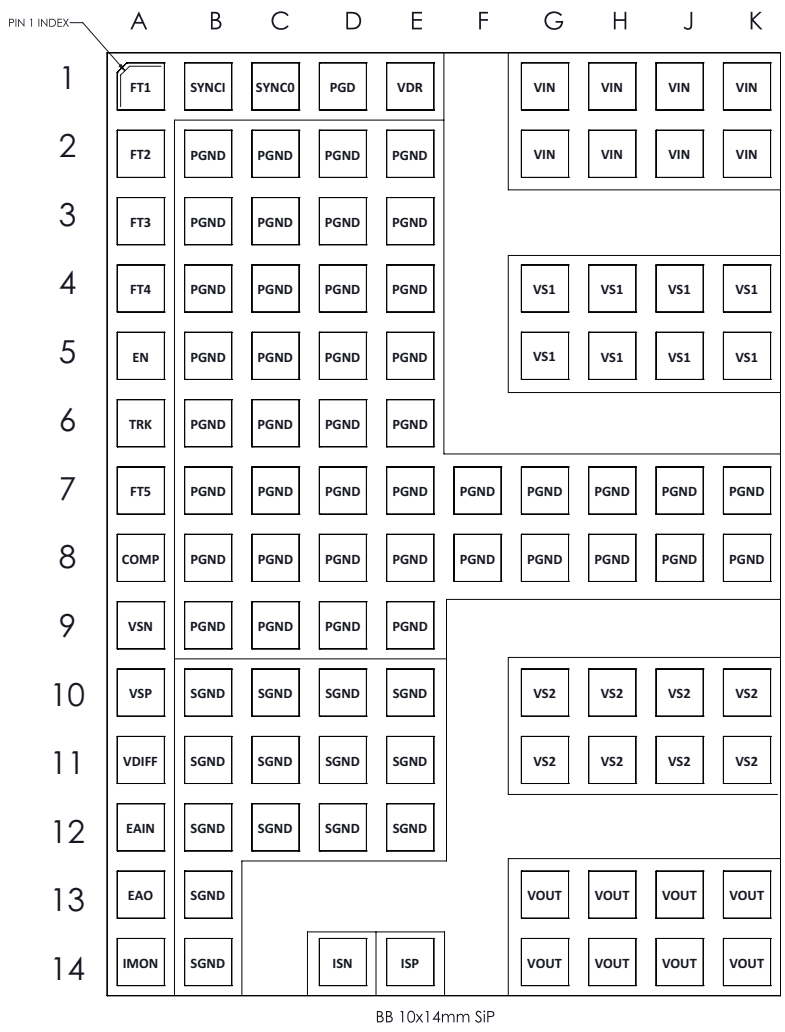
Location	Name	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1-2,G-K	VIN	36V	-0.3V	40A [1]	40A [1]
4-5,G-K	VS1	36V	$-0.7V_{DC}$	40A [1]	18A [1]
10-11,G-K	VS2	36V	$-0.7V_{DC}$	40A [1]	18A [1]
13-14,G-K	VOUT	36V	$-0.7V_{DC}$	40A [1]	40A [1]
1E	VDR	5.5V	-0.3V	30mA	200mA
1D	PGD	5.5V	-0.3V	20mA	20mA
1C	SYNCO	5.5V	-0.3V	5mA	5mA
1B	SYNCI	5.5V	-0.3V	5mA	5mA
1A	ADR1	5.5V	-0.3V	5mA	5mA
2A	ADR0	5.5V	-0.3V	5mA	5mA
3A	SCL	5.5V	-0.3V	5mA	5mA
4A	SDA	5.5V	-0.3V	10mA	10mA
5A	EN	5.5V	-0.3V	5mA	5mA
6A	TRK	5.5V	-0.3V	50mA	50mA
7A	TEST5	5.5V	-0.3V	5mA	5mA
8A	COMP	5.5V	-0.3V	5mA	5mA
9A	VSN	5.5V	-1.5V	5mA	5mA
10A	VSP	5.5V	-1.5V	5mA	5mA
11A	VDIFF	5.5V	-0.5V	5mA	5mA
12A	EAIN	5.5V	-0.3V	5mA	5mA
13A	EAO	5.5V	-0.3V	5mA	5mA
14A	IMON	5.5V	-0.3V	5mA	5mA
14D	ISN [2]	40V	$-2V_{DC}$	5mA	5mA
14E	ISP [2]	40V	$-2V_{DC}$	5mA	5mA
10-14,B + 10-12,C-E	SGND	0.3V	-0.3V	200mA	200mA
2-9,B-E + 7-8,F-K	PGND	N/A	N/A	18A [1]	18A [1]

[1] Non-Operating Test Mode Limits.
[2] The ISP pin to ISN pin has a maximum differential limit of $+5.5V_{DC}$ and $-0.5V_{DC}$.

Pin Description

Pin Number	Pin Name	Description
1-2,G-K	VIN	Input voltage and sense node for UVLO, OVLO and feed forward compensation.
4-5,G-K	VS1	Input side switching node and ZVS sense node for power switches.
10-11,G-K	VS2	Output side switching node and ZVS sense node for power switches.
13-14,G-K	VOUT	Output voltage and sense node for power switches, V_{OUT} feed forward compensation, V_{OUT_OV} and internal signals.
1E	VDR	Internal 5.1V supply for gate drivers and internal logic; not for external use.
1D	PGD	Fault & Power Good indicator. PGD pulls low when the regulator is not operating or if EAIN is less than 1.4V.
1C	SYNCO	Synchronization output. Outputs a high signal for ½ of the programmed switching period at the beginning of each switching cycle, for synchronization of other regulators.
1B	SYNCI	Synchronization input. When a falling edge synchronization pulse is detected, the PI3749-x0 will delay the start of the next switching cycle until the next falling edge sync pulse arrives, up to a maximum delay of two times the programmed switching period. If the next pulse does not arrive within two times the programmed switching period, the controller will leave sync mode and start a switching cycle automatically. Connect to SGND when not in use.
1A	ADR1	I^2C™ Addressing Pin, for use with PI3749-20 only. No connect for the PI3749-00.
2A	ADR0	I^2C Addressing Pin, for use with PI3749-20 only. No connect for the PI3749-00.
3A	SCL	I^2C Clock, for use with the PI3749-20 only. Connect to SGND for PI3749-00.
4A	SDA	I^2C Clock, for use with the PI3749-20 only. Connect to SGND for PI3749-00.
5A	EN	Regulator Enable control. Asserted high or left floating = regulator enabled; asserted low, regulator output disabled.
6A	TRK	Soft-start and track input. An external capacitor may be connected between TRK pin and SGND to decrease the rate of output rise during soft-start.
7A	TEST5	For factory use only. Connect to SGND in application.
8A	COMP	Error amp compensation dominant pole. Connect a capacitor between COMP and SGND to set the control loop dominant pole.
9A	VSN	General purpose amplifier inverting input
10A	VSP	General purpose amplifier non-inverting input
11A	VDIFF	General Purpose amplifier output. When unused connect VDIFF to VSN and VSP to SGND.
12A	EAIN	Error amplifier inverting input and sense for PGD. Connect by resistive divider to the output.
13A	EAO	Transconductance error amplifier output, PWM input and external connection for load sharing. Connect a capacitor between EAO and SGND to set the control loop high frequency pole.
14A	IMON	High side current sense amplifier output
14D	ISN	High side current sense amplifier negative input
14E	ISP	High side current sense amplifier positive input
10-14,B + 10-12,C-E	SGND	Signal ground. Internal logic and analog ground for the regulator. SGND and PGND are star connected within the regulator package.
2-9,B-E + 7-8,F-K	PGND	Power ground. V_{IN}, V_{OUT}, VS1 and VS2 power returns. SGND and PGND are star connected within the regulator package.

Package Pin-Out



BB 10x14mm SiP

TOP VIEW THROUGH THE PRODUCT

Large Pin Blocks

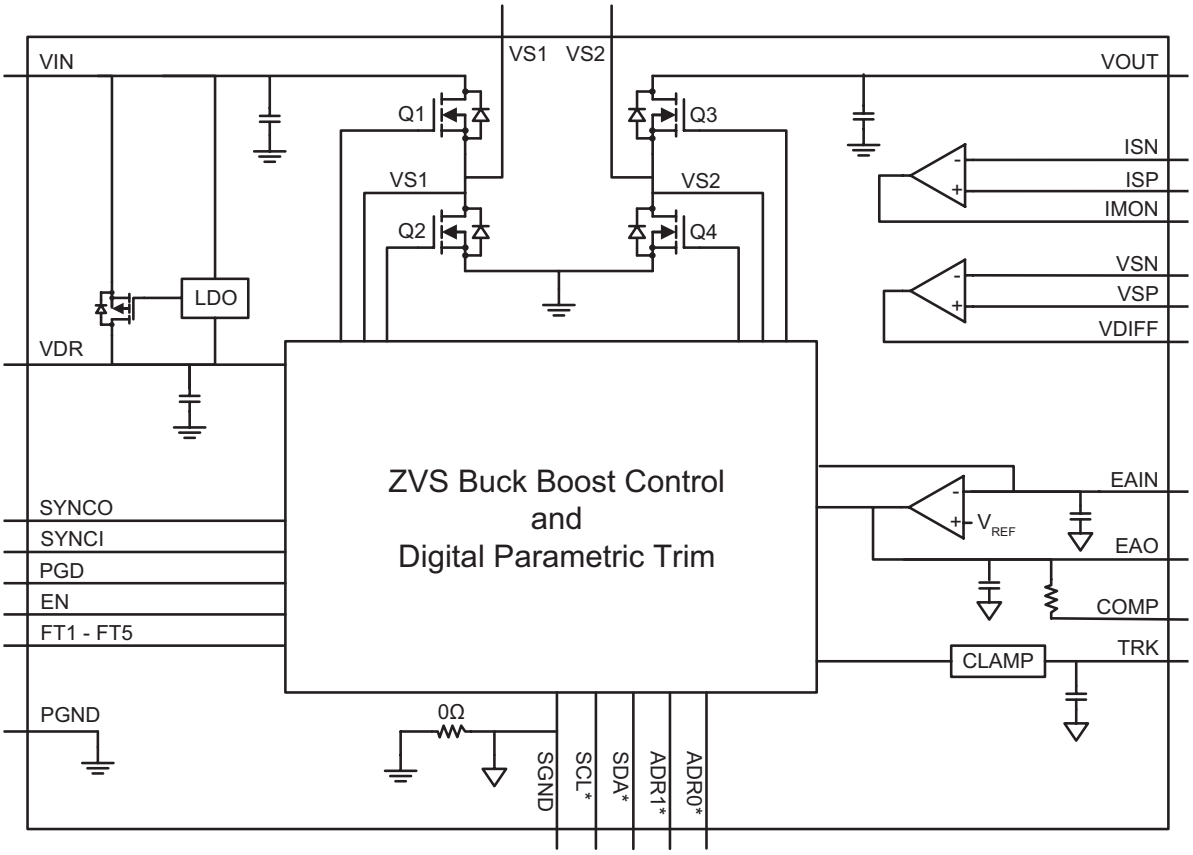
Pin Block Name	Group of pins
VIN	K1-2, J1-2, H1-2, G1-2
VS1	K4-5, J4-5, H4-5, G4-5
PGND	K7-8, J7-8, H7-8, G7-8, F7-8, E2-9, D2-9, C2-9, B2-9
VS2	K10-11, J10-11, H10-11, G10-11
VOUT	K13-14, J13-14, H13-14, G13-14
SGND	E10-12, D10-12, C10-12, B10-14

Storage and Handling Information

Maximum Storage Temperature Range	-65°C to 150°C
Maximum Operating Junction Temperature Range	-40°C to 115°C
Soldering Temperature for 20 seconds	245°C
MSL Rating	3
ESD Rating [3]	500V HBM; 1.0kV CDM

[3] JESD22-C101F, JESD22-A114F.

Block Diagram



*Simplified Block Diagram (I^2C pins SCL, SDA, ADRO, ADR1, only active for PI3749-20 device version)

Electrical Characteristics

Specifications apply for the conditions -40°C < T_J < 115°C, V_{IN} = 16V – 34V, V_{OUT} = 24V, L_{EXT} = 480nH [4], external C_{IN} = C_{OUT} = 20µF, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}		16	24	34	V
Input Current	I_{IN_DC}	I_{OUT} = 4A, V_{IN} = 24V, V_{OUT} = 24V, T_{CASE} = 25°C		4.06		A
Input Current	I_{IN_DC}	I_{OUT} = 7.0A, V_{IN} = 16V, V_{OUT} = 24V, T_{CASE} = 25°C		10.8		A
Input Current During Output Short (Fault Condition Duty Cycle)	I_{IN_SHORT}	[5]		2.5		mA
Input Quiescent Current	I_{Q_VIN}	Enabled (no load)		6.6		mA
Input Voltage Slew Rate	V_{IN_SR}	[5]			1	V/µs
Internal Input Capacitance	C_{IN}	50V, X7R type 25°C, V_{OUT} = 0V		2		µF
V_{IN} UVLO Threshold Rising	$V_{IN\_UVLO\_START}$		13.0	14.1	15.0	V
V_{IN} UVLO Hysteresis	$V_{IN\_UVLO\_HYS}$			0.7		V
V_{IN} OVLO Threshold Rising	$V_{IN\_OVLO\_START}$		35.2	37.4	39.5	V
V_{IN} OVLO Hysteresis	$V_{IN\_OVLO\_HYS}$			0.75		V
Output Specifications						
Output Voltage Range	V_{OUT_DC}	V_{IN} = 16V to 34V	12		29	V
		V_{IN} = 24V to 34V	12		34	
Output Current Steady State	I_{OUT_DC}	V_{IN} =24V, V_{OUT} = 24V, T_{CASE} = 25°C [6]	6.8			A
		V_{IN} = 16V, V_{OUT} = 24V, T_{CASE} = 25°C [6]	7.2			
		V_{IN} = 24V, V_{OUT} = 12V, T_{CASE} = 25°C [6]	10			
Output Power Steady State	P_{OUT_DC}	V_{IN} = 24V, V_{OUT} = 24V, T_{CASE} = 25°C [6]	163.2			W
		V_{IN} = 16V, V_{OUT} = 24V, T_{CASE} = 25°C [6]	172.8			
		V_{IN} = 24V, V_{OUT} = 12V, T_{CASE} = 25°C [6]	120			
Output Ripple	V_{OUT_AC}	I_{OUT} = 4A, V_{IN} = 24V, V_{OUT} = 16V, Tcase = 25°C C_{OUT_EX} = 8 x 10µF, 50V, X7S, 20MHz BW		137		mVp-p
Internal Output Capacitance	C_{OUT}	50V, X7R type 25°C, V_{OUT} = 0V		1		µF
V_{OUT} Over Voltage Threshold	V_{OUT_OVT}	Rising V_{OUT} threshold to detect open loop	35.2	37.4	39.5	V
V Drive	V_{DR}	Internal drive supply, internal use only	4.84	5.10	5.36	V
Current Sense Amplifier (Dedicated to Monitor Input or Output Current)						
ISP Pin Bias Current (Sink)		V_{OUT} = 10V, Flows to SGND	90	150	260	µA
ISN Pin Bias Current		V_{OUT} = 10V		0		µA
Common Mode Input Range			8		36	V
IMON Source Current			1	1.8	3	mA
IMON Sink Current			1	1.6	2.6	mA
IMON Output At No Load			0		10	mV
Full Scale Error		40mV input	-4		4	%
Bandwidth		[5]		40		kHz
Settling Time for Full Scale Step		1%		20		µs
Gain	A_{V_CS}			20		V/V

[4] See Inductor Pairing section.
[5] Assured to meet performance specification by design, test correlation, characterization, and/or statistical process control.
[6] Output current capability varies with input & output voltage. See performance curves in Figures 15 – 17.

Electrical Characteristics (Cont.)

Specifications apply for the conditions -40°C < T_J < 115°C, V_{IN} = 16V – 34V, V_{OUT} = 24V, L_{EXT} = 480nH[4], external C_{IN} = C_{OUT} = 20µF, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
General Purpose Amplifier						
Open Loop Gain		[5]	96	120	140	dB
Small Signal Gain-Bandwidth		[5]	5	7	12	MHz
Offset			-1	0.2	1	mV
Common Mode Input Range			-0.1		2.5	V
Differential Mode Input Range					2	V
Maximum Output Voltage		IDIFF = -1mA			V_{DR} - 0.2V	V
Minimum Output Voltage		No Load			20	mV
Capacitive Load for Stable Operation		[5]	0		100	pF
Slew Rate				10		V/µs
Output Current			-1		1	mA
Transconductance Error Amplifier						
Reference	V_{REF}	EAIN = EAO	1.667	1.7	1.734	V
Input Range	V_{EAIN}	Note V_{EAIN_OV} below	0		V_{DR}	V
Maximum Output Voltage			3.45		4.0	V
Minimum Output Voltage				0	0.1	V
Transconductance		Factory Set		7.6		mS
Zero Resistor		Factory Set		7.0		kΩ
EAO Output Current Sourcing		V_{EAO} = 50mV, V_{EAIN} = 0V		400		µA
EAO Output Current Sinking		V_{EAO} = 2V, V_{EAIN} = 5V		400		µA
Open Loop Gain		R_{OUT} > 1MΩ [5]	70	80		dB
Control and Protection						
Switching Frequency	F_{SW}	V_{IN} = V_{OUT} = 24V, I_{OUT} = 2A		800		kHz
Switching Frequency	F_{SW}	V_{IN} = 16V, V_{OUT} = 12V, I_{OUT} = 7A		480		kHz
V_{EAO} Pulse Skip Threshold	V_{EAO_PST}	V_{EAO} to SGND		0.6		V
Control Node Range	V_{RAMP}		0		3.3	V
V_{EAO} Overload Threshold	V_{EAO_OL}	V_{EAO} to SGND	3.2		3.4	V
Overload Timeout	T_{OL}	V_{EAO} > V_{EAO_OL}		1		ms
V_{OUT} Slow Current Limit	V_{OUT_SCL}	10µs time constant		18		A
V_{EAIN} Output Overvoltage Threshold	V_{EAIN_OV}	V_{EAIN} > V_{EAIN_OV}		2.04		V
Overtemperature Fault Threshold	T_{OTP}	[5]	125	129		°C
Overtemperature Restart Hysteresis	T_{OPT_HYS}	[5]		30		°C
V_{OUT} Negative Fault Threshold			-0.35	-0.25	-0.15	V

[4] See Inductor Pairing section.
[5] Assured to meet performance specification by design, test correlation, characterization, and/or statistical process control.
[6] Output current capability varies with input & output voltage. See performance curves in Figures 15 – 17.

Electrical Characteristics (Cont.)

Specifications apply for the conditions -40°C < T_J < 115°C, V_{IN} = 16V - 34V, V_{OUT} = 24V, L_{EXT} = 480nH[4], external C_{IN} = C_{OUT} = 20µF, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Soft Start and Tracking Function						
TRK Active Range		Nominal	0		1.7	V
TRK Disable Threshold			20	40	70	mV
TRK Internal Capacitance				0.047		µF
Soft Start Charge Current			30	50	70	µA
Soft Start Discharge Current		V_{TRK} = 0.5V		8.5		mA
Soft Start Time	t_{SS}	Ext C_{SS} = 0µF		1.6		ms
Enable						
Enable High Threshold	EN_{IH}		0.9	1	1.1	V
Enable Low Threshold	EN_{IL}		0.7	0.8	0.9	V
Enable Threshold Hysteresis	EN_{HYS}		100	200	300	mV
Enable Pin Bias Current		V_{EN} = 0V or V_{EN} = 2V		-50		µA
Enable Pull-Up Voltage		Floating		2.0		V
Fault Restart Delay Time	t_{FR_DLY}			30		ms
Digital Signals						
SYNCI Threshold Rising		V_{DR} = 5.1V		3.1		V
SYNCI Threshold Falling		V_{DR} = 5.1V		2.2		V
SYNCO High	$SYNCO_{OH}$		V_{DR} - 0.5		V_{DR}	V
SYNCO Low	$SYNCO_{OL}$	$I_{SYNCOUT}$ = 1mA			0.5	V
PGD High Leakage	PGD_{ILH}	V_{PGD} = V_{DR}			10	µA
PGD Output Low	PGD_{OL}	I_{PGD} = 4mA			0.4	V
PGD EAIN Low Rise			1.41	1.45	1.48	V
PGD EAIN Low Fall			1.36	1.41	1.46	V
PGD EAIN Threshold Hysteresis				35		mV
PGD EAIN High			1.94	2.04	2.14	V
I²C Digital Signals (PI3749-20 only)						
I²C™ Address High Threshold	$V_{ADRx-HI}$		3.872	4.59		V
I²C Address Mid Threshold	$V_{ADRx-MID}$		1.452		3.752	V
I²C Address Low Threshold	$V_{ADRx-LOW}$			0.51	1.072	V
I²C Address Resistance, Within Mid Thresholds	$R_{ADRx-MID}$	Resistance to 2.5V, when ADRx pin voltage within V_{ADRx_MID}		10		V
I²C Address Resistance, Outside Mid Thresholds	$R_{ADRx-MID}$	Resistance to 2.5V, when ADRx pin voltage outside range of V_{ADRx_MID}		200		V
SCL, SDA In High	V_{SER_IH}		2.1			V
SCL, SDA In Low	V_{SER_IL}				1.5	V
SDA Out Low	V_{SER_OL}	Sinking up to 3mA			0.4	V
SCL, SDA Pull-Down Current	I_{SER_I}	Weak pull-down current to SGND			10	V

[4] See Inductor Pairing section.
[5] Assured to meet performance specification by design, test correlation, characterization, and/or statistical process control.
[6] Output current capability varies with input & output voltage. See performance curves in Figures 15 – 17.

Performance Characteristics T_A = 25°C

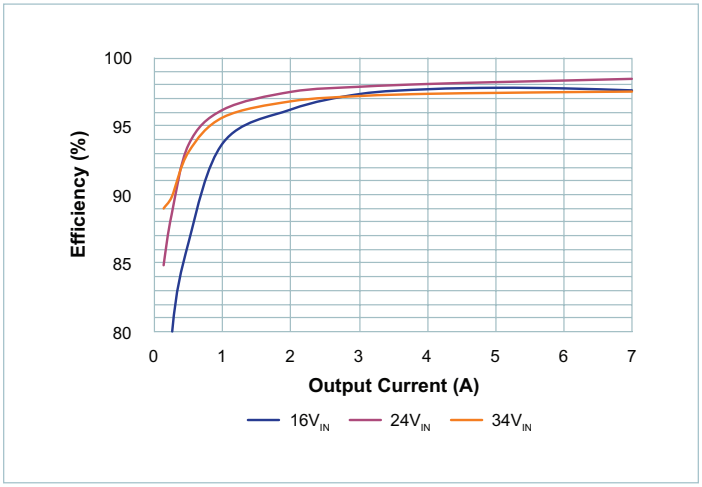


Figure 1 — *$24V_{OUT}$ Efficiency*

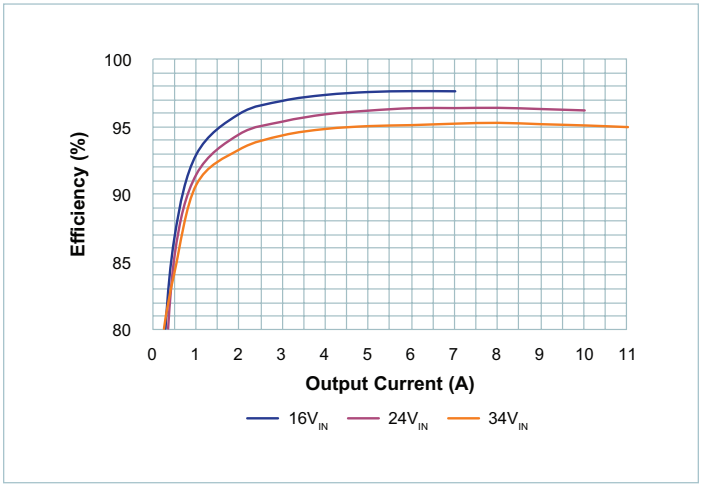


Figure 2 — *$12V_{OUT}$ Efficiency*

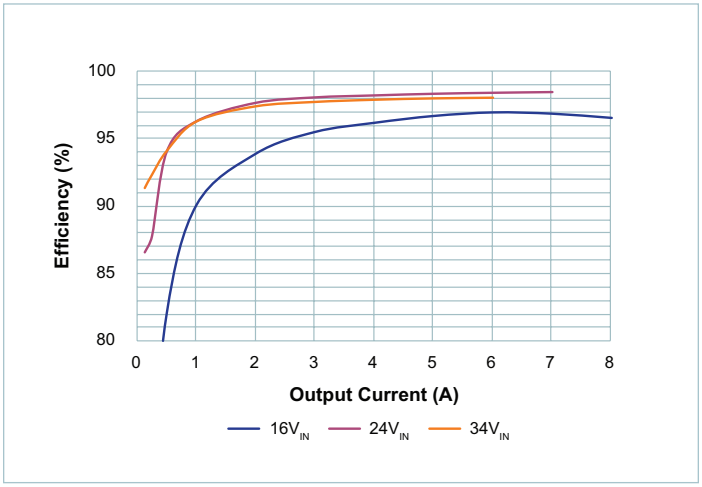


Figure 3 — *$28V_{OUT}$ Efficiency*

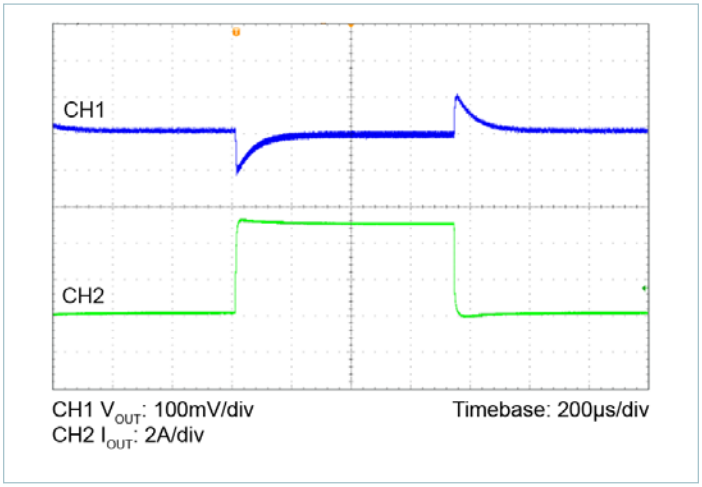


Figure 4 — *$34V_{IN}$ to $12V_{OUT}$, C_{OUT} = 8 x 10µF Ceramic 5.0A Load Step at 5A/µs*

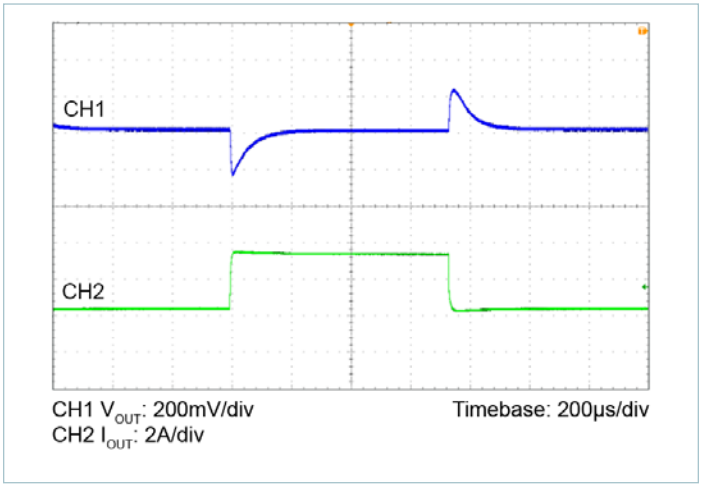


Figure 5 — *$24V_{IN}$ to $24V_{OUT}$, C_{OUT} = 8 x 10µF Ceramic 3.0A Load Step at 5A/µs*

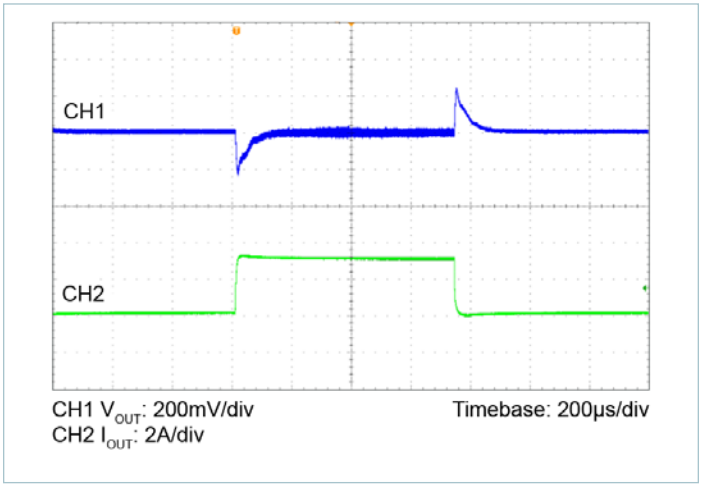


Figure 6 — *$16V_{IN}$ to $28V_{OUT}$, C_{OUT} = 8 x 10µF Ceramic 3.0A Load Step at 5A/µs*

Performance Characteristics T_A = 25°C (Cont.)

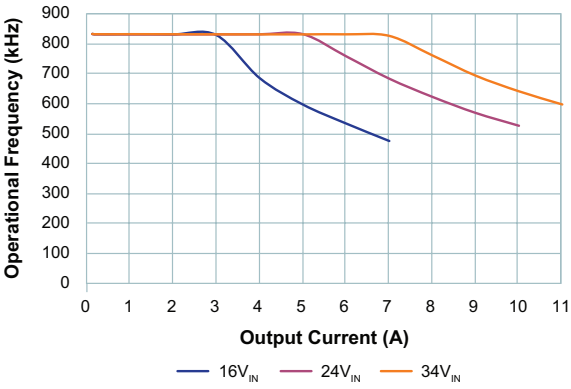


Figure 7 — *Switching Frequency vs. Output Current @ $12V_{OUT}$*

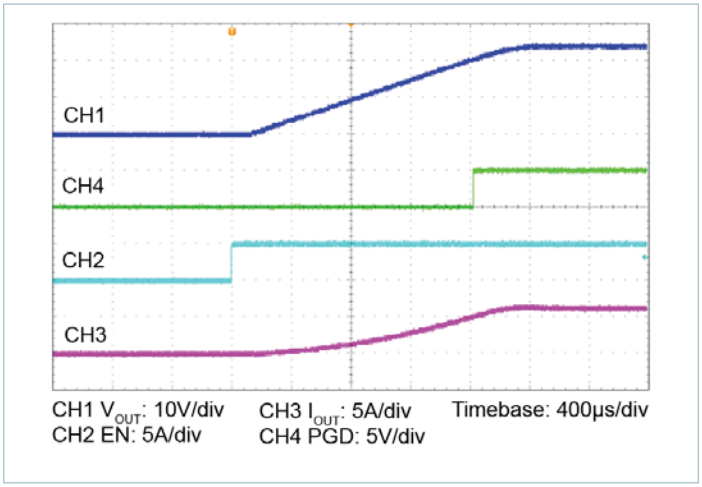


Figure 10 — *Start-up with $24V_{IN}$ to $24V_{OUT}$ at 5A*

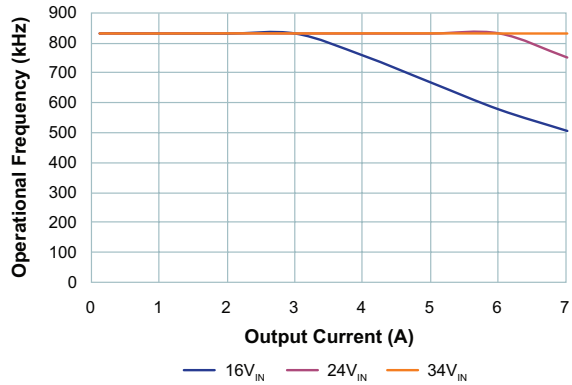


Figure 8 — *Switching Frequency vs. Output Current @ $24V_{OUT}$*

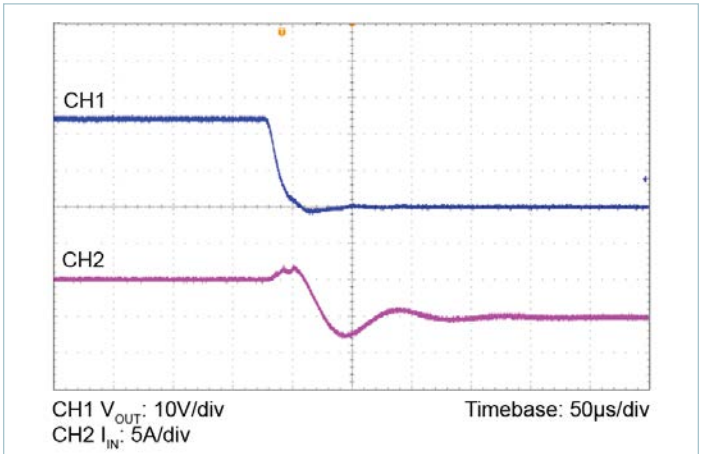


Figure 11 — *Short Circuit with $24V_{IN}$ to $24V_{OUT}$ at 5A*

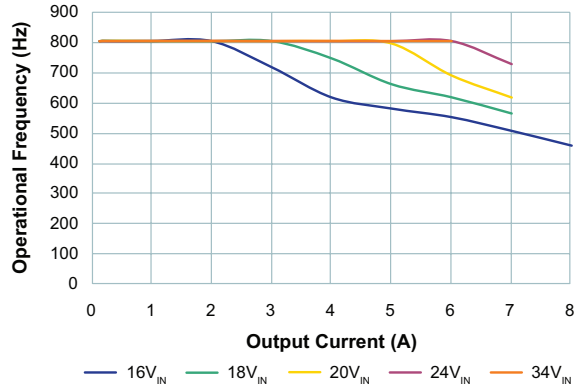


Figure 9 — *Switching Frequency vs. Output Current @ $28V_{OUT}$*

Efficiency & Power Loss T_A = 25°C [7]

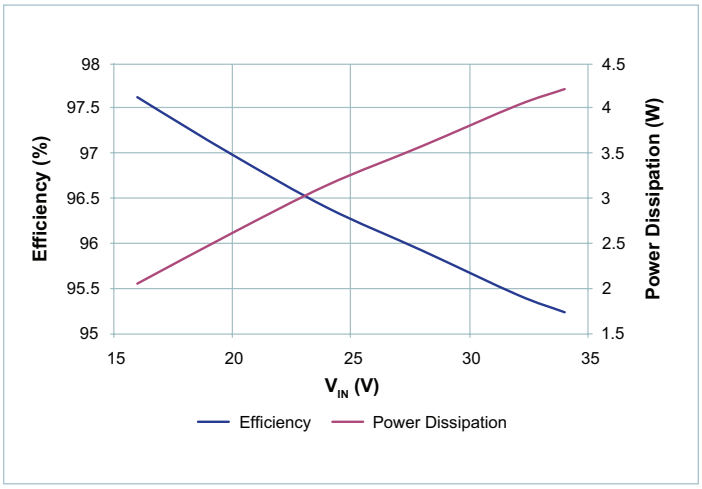


Figure 12 — *$12V_{OUT}$ Efficiency and Power Dissipation at 7A over Input Voltage Range*

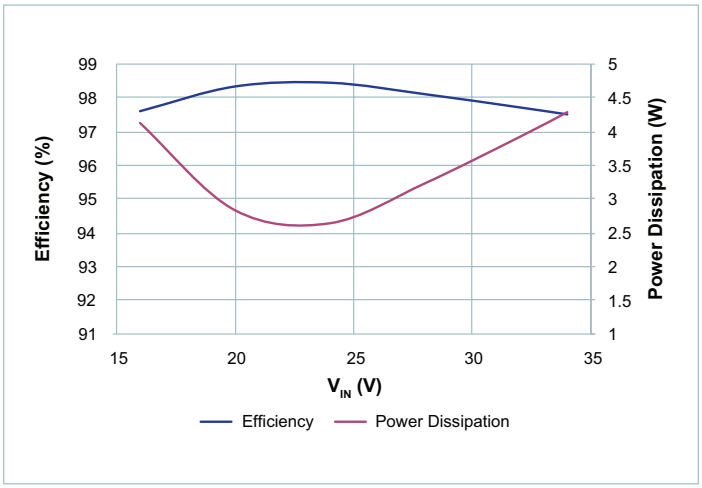


Figure 13 — *$24V_{OUT}$ Efficiency and Power Dissipation at 7A over Input Voltage Range*

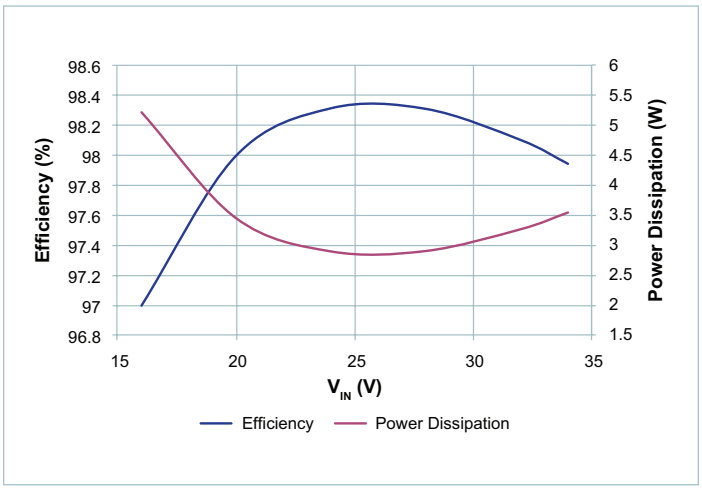


Figure 14 — *$28V_{OUT}$ Efficiency and Power Dissipation at 6A over Input Voltage Range*

Safe Operating Area T_A = 25°C [7]

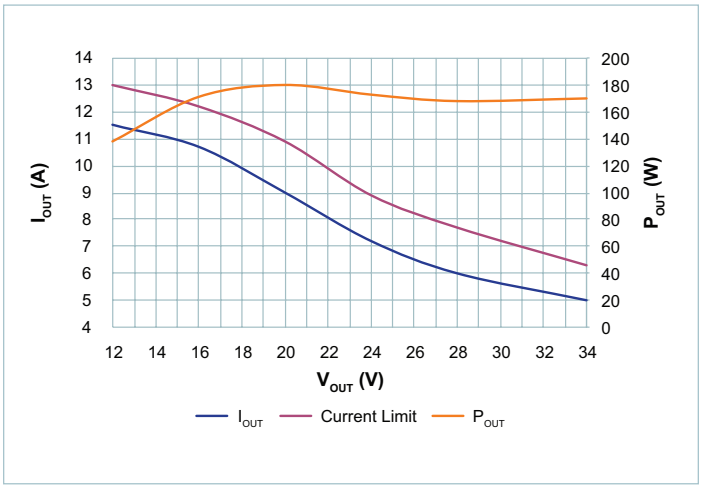


Figure 15 — *Power and current output at $34V_{IN}$*

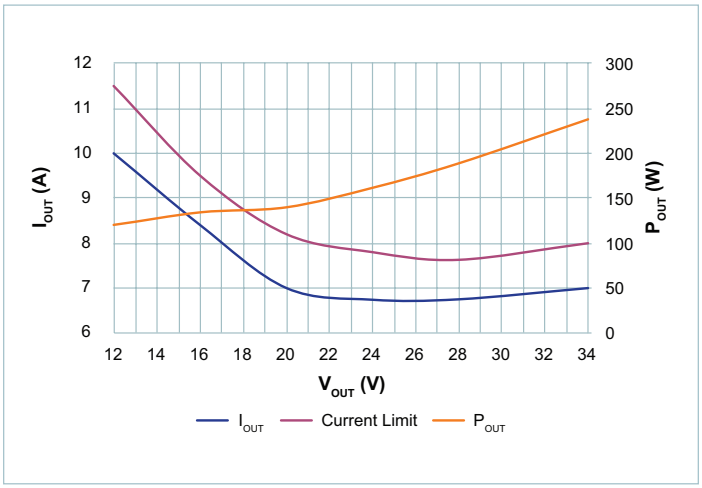


Figure 16 — *Power and current output at $24V_{IN}$*

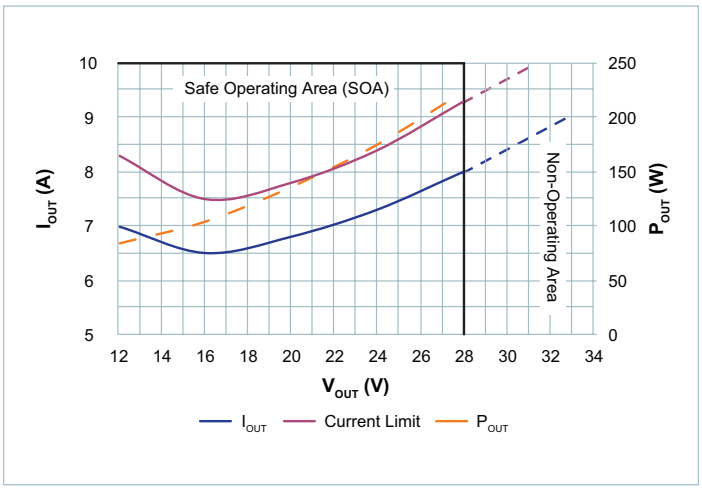


Figure 17 — *Power and current output at V_{IN} less than 24V*

[7] **Note:** Testing was performed using a 3 in. x 3 in., four 2 oz. copper layers, FR4 evaluation board platform.

Thermal De-Rating [7]

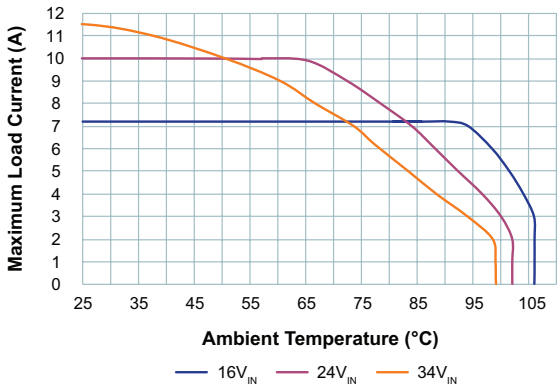


Figure 18 — *Thermal de-rating @ V_{OUT} = 12V*

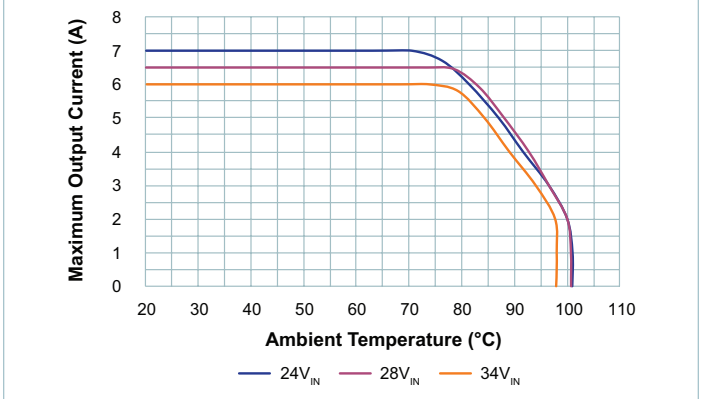


Figure 21 — *Thermal de-rating @ V_{OUT} = 30V with Limited Input Range ($24V_{IN}$ to $34V_{IN}$)*

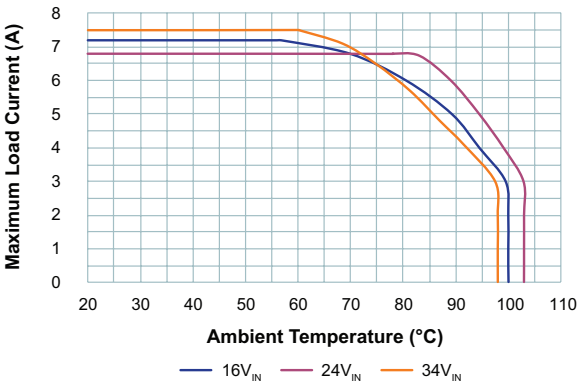


Figure 19 — *Thermal de-rating @ V_{OUT} = 24V*

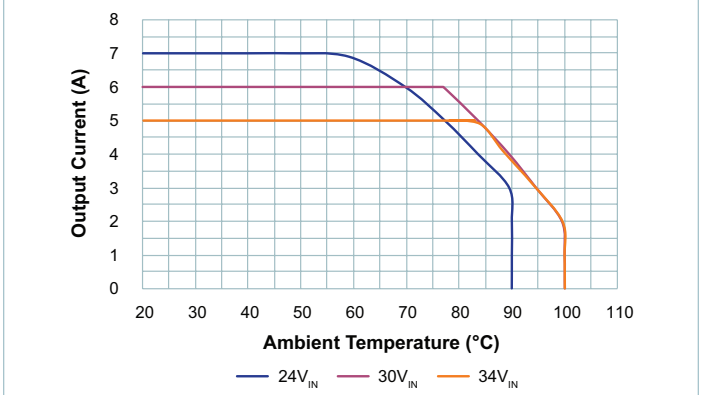


Figure 22 — *Thermal de-rating @ V_{OUT} = 34V with Limited Input Range ($24V_{IN}$ to $34V_{IN}$)*

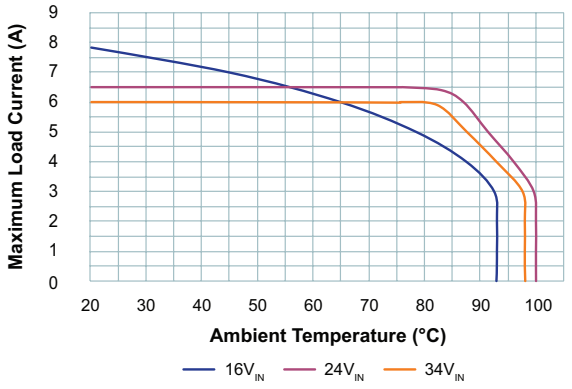


Figure 20 — *Thermal de-rating @ V_{OUT} = 28V*

[7] **Note:** Testing was performed using a 3 in. x 3 in., four 2 oz. copper layers, FR4 evaluation board platform.

MTBF

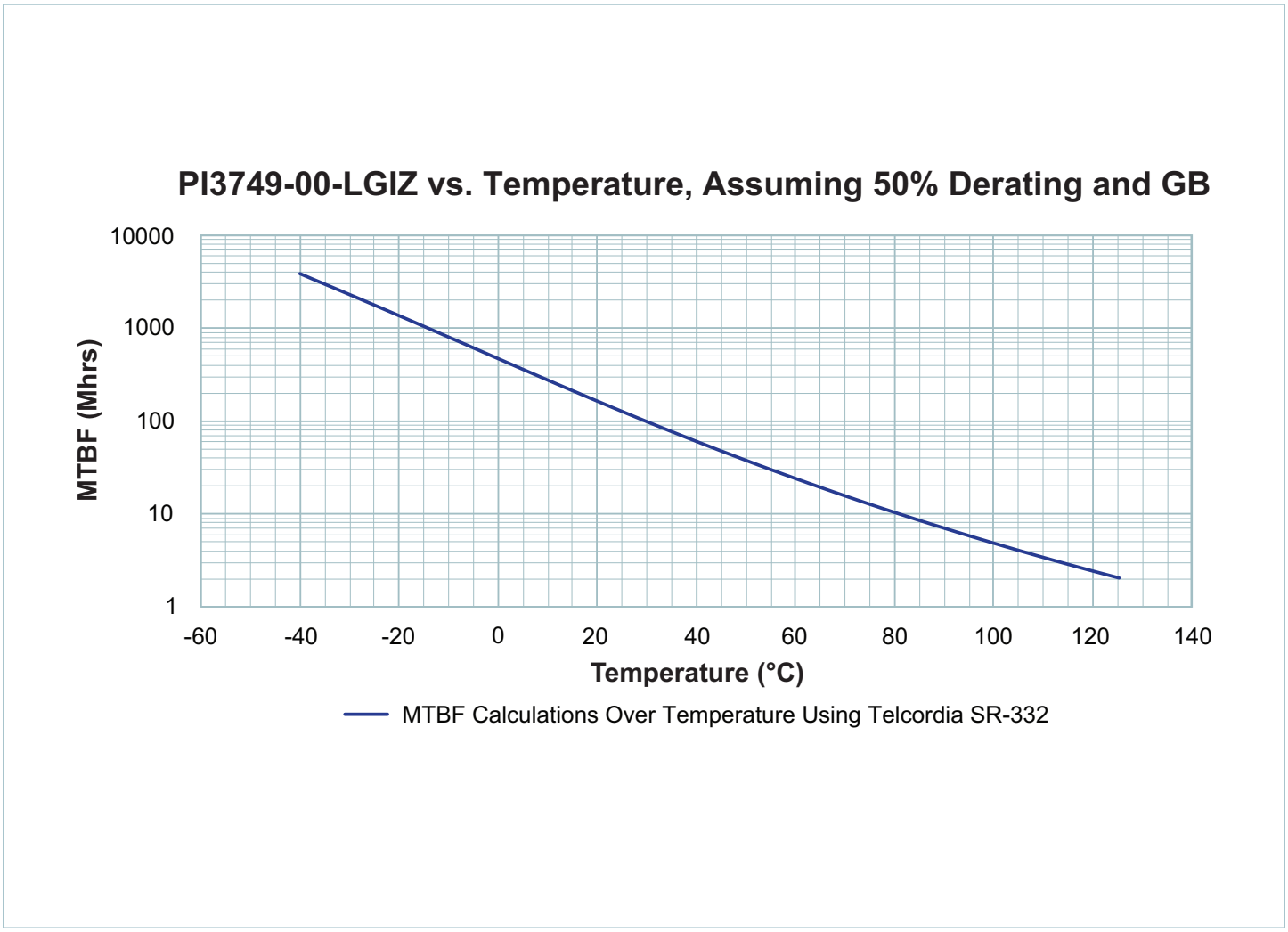


Figure 23 — *PI3749-x0 calculated MTBF Telcordia SR-332 GB*

Functional Description

The PI3749-x0 is part of a family of highly integrated ZVS Buck-Boost regulators. The PI3749-x0 has a variable output voltage that is set with a resistive divider. Performance and maximum output current are characterized with a specific external power inductor as defined in electrical specifications, with Inductor Pairing section.

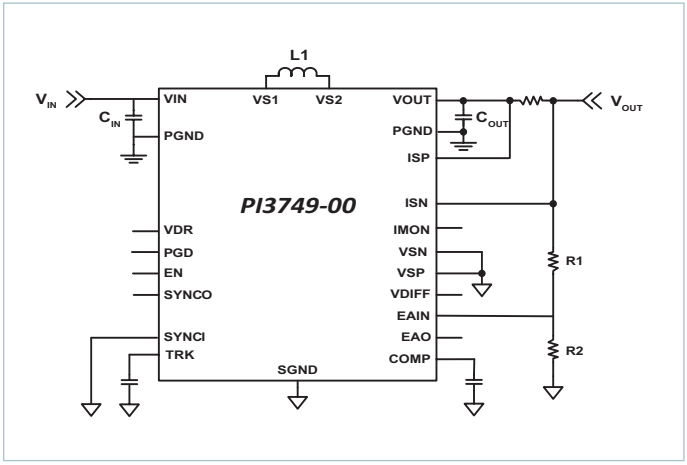


Figure 24 — *ZVS Buck-Boost with required components*

For basic operation, Figure 24 shows the minimum connections and components required.

Enable

The EN pin of the regulator is referenced to SGND and permits the user to turn the regulator on or off. The EN polarity is a positive logic assertion. If the EN pin is left floating or asserted high, the regulator output is enabled. Pulling the EN pin below $0.8V_{DC}$ with respect to SGND will discharge the SS/TRK pin until the output reaches zero or the EN pin is released.

Switching Frequency Synchronization

The SYNCI input allows the user to synchronize the controller switching frequency to the falling edge of an external clock referenced to SGND. The external clock can synchronize the unit between 50% and 110% of the preset switching frequency (F_{SW}). The SYNCI pin should be connected to SGND when not in use, and should never be left floating.

Soft-Start and Tracking

The PI3749-x0 provides a soft start and tracking feature using the TRK pin. Programmable Soft Start requires an external capacitor from the TRK pin to SGND in addition to the internal 47nF soft-start capacitor to set the start-up ramp period greater then t_{SS}. The PI3749-x0 output will proportionately follow the TRK pin when it is below $1.7V_{DC}$. If the TRK pin is goes below the disable threshold, the regulator will finish the current switching cycle and then stop switching.

Remote Sensing Differential Amplifier

A general purpose operational amplifier is provided to assist with differential remote sensing and or level shifting of the output voltage. The VDIFF pin can be connected to the transconductance error amplifier input EAIN pin, or with proper configuration can also be connected to the EAO pin to drive the modulator directly.

Power Good

The PI3749-x0 PGD pin functions as a power good indicator and pulls low when the regulator is not operating or if EAIN is less than 1.4V.

Output Current Limit Protection

PI3749-x0 has three methods implemented to protect from output short circuit or over current condition.

Slow Current Limit protection: prevents the output load from sourcing current higher than the maximum rated regulator current. If the output current exceeds the V_{OUT} Slow Current Limit (V_{OUT_SCL}) a slow current limit fault is initiated and the regulator is shutdown which eliminates output current flow. After Fault Restart Delay (t_{FR_DLY}), a soft-start cycle is initiated. This restart cycle will be repeated indefinitely until the excessive load is removed.

Fast Current Limit protection: monitors the regulator inductor current pulse-by-pulse to prevent the output from supplying very high current. If the regulator senses a high inductor current pulse, it will initiate a fault and stop switching. After Fault Restart Delay (t_{FR_DLY}), a soft-start cycle is initiated. This restart cycle will be repeated indefinitely until the excessive load is removed.

Overload Timeout protection: If the regulator is providing maximum output power for longer than the Overload Timeout Delay (T_{OL}), it will initiate a fault and stop switching. After Fault Restart Delay (t_{FR_DLY}), a soft-start cycle is initiated. This restart cycle will be repeated indefinitely until the overload load is removed.

Input Undervoltage Lockout

If V_{IN} falls below the input Under Voltage Lockout (UVLO) threshold, the PI3749-x0 will complete the current cycle and stop switching. The system will restart once the input voltage is reestablished and after the Fault Restart Delay.

Input Overvoltage Lockout

If V_{IN} rises above the input Overvoltage Lockout (OVLO) threshold, the PI3749-x0 will complete the current cycle and stop switching. The system will restart once the input voltage is reestablished and after the Fault Restart Delay.

Output Overvoltage Protection

The PI3749-x0 family is equipped with two methods of detecting an output overvoltage condition. Output Overvoltage Protection (OVP) to prevent damage to input voltage sensitive devices. If the output voltage exceeds 20% of its set regulated value as measured by the EAIN pin (V_{EAIN_OV}), the regulator will complete the current cycle, stop switching and issue an OVP fault. Also if the output voltage of the regulator exceeds the V_{OUT} Overvoltage Threshold (V_{OUT_OVT}) then the regulator will complete the current cycle, stop switching and issue an OVP fault. The system will resume operation once the output voltage falls below the OVP threshold and after Fault Restart Delay.

Overtemperature Protection

The internal package temperature is monitored to prevent internal components from reaching their thermal maximum. If the Overtemperature Protection Threshold is exceeded (T_{OTP}), the regulator will complete the current switching cycle, enter a low power mode, set a fault flag, and will soft-start when the internal temperature decreases by more than the Overtemperature Restart Hysteresis (T_{OTP_HYS}).

Pulse Skip Mode (PSM)

PI3749-x0 features a hysteretic Pulse Skip Mode to achieve high efficiency at light loads. The regulator is setup to skip pulses if V_{EAO} falls below the Pulse Skip Threshold (V_{EAO_PST}). Depending on conditions and component values, this may result in single pulses or several consecutive pulses followed by skipped pulses. Skipping cycles significantly reduces gate drive power and improves light load efficiency. The regulator will leave Pulse Skip Mode once the control node rises above the Pulse Skip Mode Threshold (V_{EAO_PST}).

Variable Frequency Operation

The PI3749-x0 is preprogrammed to a fixed, maximum, base operating frequency. The frequency is selected with respect to the required power stage inductor to operate at peak efficiency across line and load variations. The switching frequency period will stretch as needed during each cycle to accommodate low line and or high load conditions. By stretching the switching frequency period, thus decreasing the switching frequency, the ZVS operation is preserved throughout the input line voltage range maintaining optimum efficiency.

IMON Amplifier

The PI3749-x0 provides a differential amplifier with a level shifted, SGND referenced output, the IMON Pin, which is useful for sensing input or output current on high voltage rails. A fixed gain of 20:1 is provided over a large common mode range. When using the amplifier, the ISN pin must be referenced to the common mode voltage of the ISP pin for proper operation. See Absolute Maximum Ratings for more information. If not in use, the ISN and ISP pins should be connected to SGND and the IMON pin left floating.

I^2C Interface Operation

PI3749-20 devices provide an I^2C digital interface that enables the user to:

Device Configuration Options:

- Dynamic V_{OUT} margining
- Programmable Sync Phase Delay

Fault telemetry including:

- Input and Output Overvoltage
- Input and Output Undervoltage
- Internal Bias Supply Undervoltage
- Overtemperature Protection
- Multi Tiered Current Limit reporting

Applications Information

Input / Output Range Limitation

The PI3749-x0 is capable of wide step-up and step-down conversions, but high boosting ratios place thermal stress on the external inductor that may not be fully protected by the controller overtemperature shut down. For this reason boosting above 29V out when the input voltage is less than 24V is not supported.

Output Voltage Trim

The output voltage can be adjusted by feeding back a portion of the desired output through a voltage divider to the error amplifier's input (see Figure 24). Equation 1 can be used to determine resistor values needed for the voltage divider.

$$R1 = R2 \bullet \left(\frac{V_{OUT}}{1.7} - 1 \right) \qquad (1)$$

The R2 value is selected by the user; a 1.07kΩ resistor value is recommended.

If, for example, a 24V output is needed, the user can select a 1.07kΩ (1%) resistor for R2 and use equation (1) to calculate R1. Once R1 value is calculated, the user should select the nearest resistor value available. In this example, R1 is 14.03kΩ so a 14.0kΩ should be selected.

Soft-Start Adjustment and Tracking

The TRK pin offers a means to increase the regulator's soft-start time or to track with additional regulators. The soft-start slope is controlled by an internal 47nF and a fixed charge current to provide a minimum startup time of 1.6ms (typical). By adding an external capacitor to the TRK pin, the soft-start time can be increased further. The following equation can be used to calculate the proper capacitor for a desired soft-start times:

Where, t_{TRK} is the desired soft-start time and I_{SS} is the T_{RK} pin source current (see Electrical Characteristics for limits).

$$C_{TRK} = \frac{(t_{TRK} \bullet I_{SS})}{1.7} - 47 \bullet 10^{-9} \qquad (2)$$

The PI3749-x0 allows the tracking of multiple like regulators. Two methods of tracking can be chosen: proportional or direct tracking. Proportional tracking will force all connected regulators to startup and reach regulation at the same time (see Figure 25 (a)). To implement proportional tracking, simply connect all devices TRK pins together.

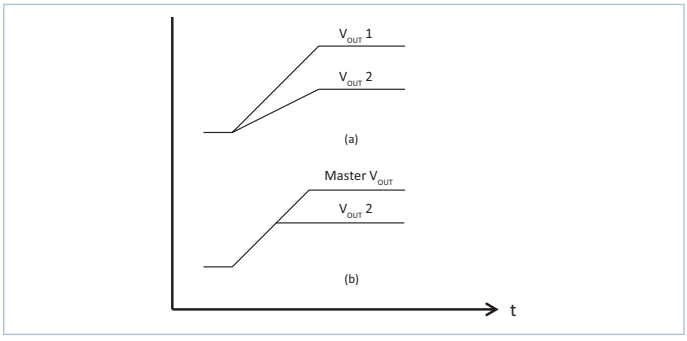


Figure 25 — *PI3749-x0 tracking methods*

For Direct Tracking, choose the regulator with the highest output voltage as the master and connect the master to the TRK pin of the other regulators through a divider (Figure 26) with the same ratio as the slave's feedback divider (see Output Voltage Trim).

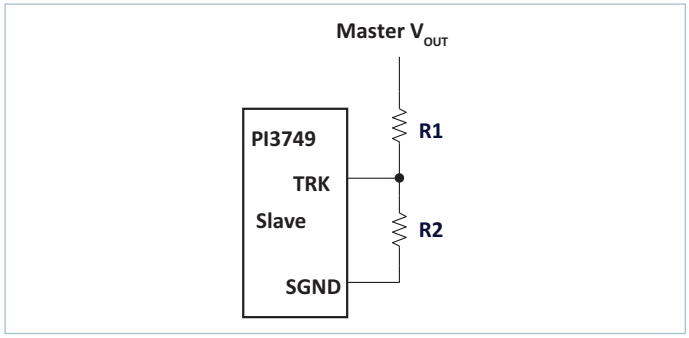


Figure 26 — *Voltage divider connections for direct tracking*

All connected regulators' soft-start slopes will track with this method. Direct tracking timing is demonstrated in Figure 25 (b). All tracking regulators should have their Enable (EN) pins connected together for proper operation.

Inductor Pairing

Operations and characterization of the PI3749-x0 was performed using a 480nH inductor, Part # HCV1206-R48-R, manufactured by Eaton. This Inductor has a form factor of 12.5mm x 10mm x 5mm. No other inductor is recommended for use with the PI3749-x0. For additional inductor information and sourcing, please contact Eaton directly.

Thermal De-rating

Thermal de-rating curves are provided (page 13) that are based on component temperature changes versus load current, input voltage and no air flow. It is recommended to use these curves as a guideline for proper thermal de-rating. These curves represent the entire system and are inclusive to both the SiP and the external inductor. Maximum thermal operation is limited by either the MOSFETs or inductor depending upon line and load conditions.

All thermal testing was performed using a 3in. x 3in., four 2oz. copper layers, FR4 evaluation board platform. Thermal measurements were made on the five main power devices; the four internal MOSFETS and the external inductor.

Filter Considerations

The PI3749-x0 requires low impedance ceramic input capacitors (X7R/X5R or equivalent) to ensure proper start up and high frequency decoupling for the power stage. The PI3749-x0 will draw nearly all of the high frequency current from the low impedance ceramic capacitors when the main high side MOSFET(s) are conducting. During the time the MOSFET(s) are off, the input capacitors are replenished from the source.
Table 1 shows the recommended input and output capacitors to be used for the PI3749-x0 as well as total RMS current, and input and output ripple voltages. Divide the total RMS current by the

number of ceramic capacitors used to calculate the individual capacitor's RMS current. Table 2 includes the recommended input and output ceramic capacitor. It is very important to verify that the voltage supply source as well as the interconnecting line are stable and do not oscillate.

Input Filter Case 1; Inductive source and local, external, input decoupling capacitance with negligible ESR (i.e.: ceramic type)

The voltage source impedance can be modeled as a series Rline L_{line} circuit. The high performance ceramic decoupling capacitors will not significantly damp the network because of their low ESR; therefore in order to guarantee stability the following conditions must be verified:

$$R_{line} > \frac{L_{line}}{\left(C_{IN\_INT} + C_{IN\_EXT}\right) \bullet \left|r_{EQ\_IN}\right|} \qquad (3)$$

$$R_{line} << \left|r_{EQ\_IN}\right| \qquad (4)$$

Where, r_{EQ_IN} can be calculated by dividing the lowest line voltage by the full load input current. It is critical that the line source impedance be at least an octave lower than the converter's dynamic input resistance, Equation (4). However, R_{line} cannot be made arbitrarily low otherwise Equation (3) is violated and the system will show instability, due to under-damped RLC input network.

Input Filter Case 2; Inductive source and local, external input decoupling capacitance with significant $R_{C_{IN\_EXT}}$ ESR (i.e.: electrolytic type)

In order to simplify the analysis in this case, the voltage source impedance can be modeled as a simple inductor L_{line}. Notice that, the high performance ceramic capacitors C_{IN_INT} within the PI3749-x0 should be included in the external electrolytic capacitance value for this purpose. The stability criteria will be:

$$\left|r_{EQ\_IN}\right| > R_{C_{IN\_EXT}} \qquad (5)$$

$$\frac{L_{line}}{C_{IN\_INT} \bullet R_{C_{IN\_EXT}}} < \left|r_{EQ\_IN}\right| \qquad (6)$$

Equation (6) shows that if the aggregate ESR is too small – for example by using very high quality input capacitors (C_{IN_EXT}) – the system will be under-damped and may even become destabilized. Again, an octave of design margin in satisfying Equation (5) should be considered the minimum.

Note: When applying an electrolytic capacitor for input filter damping the ESR value must be chosen to avoid loss of converter efficiency and excessive power dissipation in the electrolytic capacitor.

Parallel Operation

PI3749-x0 can be connected in parallel up to two phases, with interleaving. Parallel interleaved modules can be used to increase the output current capability of a single power rail and reduce output voltage ripple. Figure 27 shows the proper connection of two regulators in parallel interleaved operation. Connecting a higher number of modules (up to six maximum) is possible without interleaving or synchronization. Connecting groups of interleaved modules would be the best configuration for applications requiring higher current than two modules can produce. The user must consider a worst case sharing error of ±10% when considering a two unit parallel system to avoid overloading one module or tripping current limit during load transients.

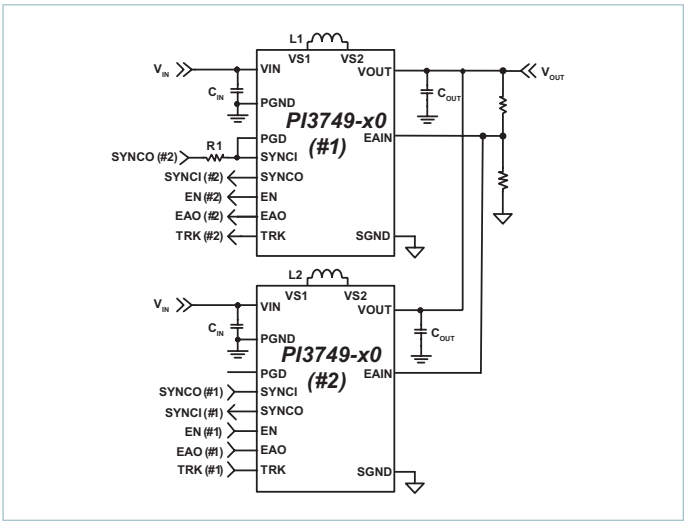


Figure 27 — *PI3749-x0 parallel operation*

By connecting the EAO pins and SGND pins of each module together, the regulators will share the output current equally, provided each power inductor is the same value and the output ripple is not excessive. Connecting all TRK pins will force all units to track each other during soft-start. Additionally, all units EN pins must be released to allow the units to start (See Figure 27).

To provide synchronization between regulators over the entire operational frequency range, the Power Good (PGD) pin must be connected to the lead regulator's (#1) SYNCI pin and a 2.5kΩ Resistor, R1, must be placed between SYNCO (#2) return and the lead regulator's SYNCI (#1) pin, as shown in Figure 27. In this configuration, at system soft-start, the PGD pin pulls SYNCI low forcing the lead regulator to initialize the open-loop startup synchronization. Once the regulators reach regulation, SYNCI is released and the system is now synchronized in a closed-loop configuration which allows the system to maintain correct synchronization when any of the individual regulators begin to enter variable frequency mode.

Any fault event flagged by one regulator will disable the other regulators. The regulators will not be synchronized during a fault or during startup (resulting in higher output ripple for that period of time) until the PGD pin is released.

V_{OUT} (V)	V_{IN} (V)	I_{LOAD} (A)	C_{INPUT} (see table 2)	C_{OUTPUT} (see table 2)	C_{INPUT} Ripple Current (I_{RMS})	C_{OUTPUT} Ripple Current (I_{RMS})	Output Ripple (mVpp)	Input Ripple (mVpp)
12	16	5	6 X 10µF	8 X 10µF	3.55	3.65	37.1	67.5
		7			4.59	4.89	60.6	113
12	20	6	6 X 10µF	8 X 10µF	4.45	4.43	44	84.3
		9			6.08	6.32	80.5	162
12	24	6	6 X 10µF	8 X 10µF	4.68	4.36	40.2	81
		10			6.93	6.84	88	184
12	28	6	6 X 10µF	8 X 10µF	5.06	4.34	43.4	90.1
		11			7.66	7.21	95	217
12	34	7	6 X 10µF	8 X 10µF	5.78	4.64	50	125
		11			7.8	6.76	87	240
24	16	5	6 X 10µF	8 X 10µF	5.13	4.49	75.4	63.5
		7			7.08	6.07	138	114
24	20	5	6 X 10µF	8 X 10µF	4.28	3.91	61.6	56
		7			5.3	4.6	85	75
24	24	5	6 X 10µF	8 X 10µF	4.24	4.13	64	82
		7			4.7	4.5	68	88
24	28	5	6 X 10µF	8 X 10µF	4.55	4.4	68	105
		7			5.1	5.1	74	121
24	34	5	6 X 10µF	8 X 10µF	5.1	4.66	72.5	142
		7			5.93	5.67	83	176
28	16	6	6 X 10µF	8 X 10µF	7.18	6.5	143.5	108
		9			10.62	9.37	301	223
28	20	5	6 X 10µF	8 X 10µF	5.09	4.65	84	70
		7			6.49	5.51	122	95
28	24	5	6 X 10µF	8 X 10µF	4.68	4.46	82	83
		6			5.06	4.68	87	83.5
28	28	5	6 X 10µF	8 X 10µF	4.66	4.54	83	107.5
		7			5.31	5.16	93	119
28	34	4	6 X 10µF	8 X 10µF	4.5	4.18	77.4	130.6
		6			5.49	5.26	95	168
34	24	5	6 X 10µF	8 X 10µF	5.6	5.39	124	95
		7			6.66	5.76	148	100
34	29	4	6 X 10µF	8 X 10µF	4.5	4.5	107	107
		6			5.6	5.33	133	122
34	34	3	6 X 10µF	8 X 10µF	3.87	3.7	90.4	118
		5			5.12	4.95	124	160

Table 1 — *Recommended input and output capacitance*

Part Number	Description	MFG Description
C3225X7S1H106M250AB	10µF Capacitor, X7S 20% 50V, 1210	TDK

Table 2 — *Capacitor manufacturer part numbers*

I²C Addressing

The PI3749-20 is hardware compatible with the NXP I²C™ Bus Specification Version 2.1, January 2000, in Standard Mode (100kHz) for all bus timing and voltage levels up to 5.5V. It operates as a slave on the I²C bus.

The PI3749-20 I²C interface responds to the address programmed by the two I²C Address pins, ADR1 and ADR0. The address pins are three level inputs, providing nine possible combination pairs, although only eight of these combinations are unique, as shown in table 3. Considering only the 7 bit address sub-field, the high-order address bits <6> through <4> are hardcoded to 4'b1001, while the lower order address bits <3> through <0> are modified by the ADRx pins.

ADDRx state		Resultant I²C address sub-field Sub-field bit positions <7.1>			Fully formed address write word (including lsb of the transfer set for a write)
ADR1	ADR0	Hexadecimal	Decimal	Binary	Binary
L	L	7'h48	72	7'b100_1000	8'b1001_0001
L	M	7'h49	73	7'b100_1001	8'b1001_0011
L	H	7'h4A	74	7'b100_1010	8'b1001_0101
M	L	7'h4B	75	7'b100_1011	8'b1001_0111
M	M	7'h4C	76	7'b100_1100	8'b1001_1001
M	H	7'h4D	77	7'b100_1101	8'b1001_1011
H	L	7'h4E	78	7'b100_1110	8'b1001_1101
H	M	7'h4F	79	7'b100_1111	8'b1001_1111
H	H	7'h4F	79	7'b100_1111	8'b1001_1111

Table 3 — *I²C Address selection*

Note that the state of the ADRx pins is resolved on each I²C address transfer. Therefore the PI3749-20 address can be changed while the regulator is powered up and in operation.

I²C Command Structure

Depending on the state of the read/write bit, two types of transfers are possible:

a. *Write: Data transferred from the I²C master to the PI3749-20 slave*
The first byte is transmitted by the master and includes the slave address and the R/W bit set to write (as shown in the last column of Table 3.) The second byte is also transmitted by the master and is the write data. The slave responds between each byte with an acknowledge bit.

b. *Read: Data returned from the PI3749-20 slave to the master*
The first byte is transmitted by the master and includes the slave address but the R/W bit is set to read. The slave responds to the first byte (the address transmitted by the master) with an acknowledge bit. The second byte is transmitted by the slave back to the master and is the read data. The master responds after the read data byte with a not-acknowledge bit (since the PI3749-20 read data are all single byte registers).

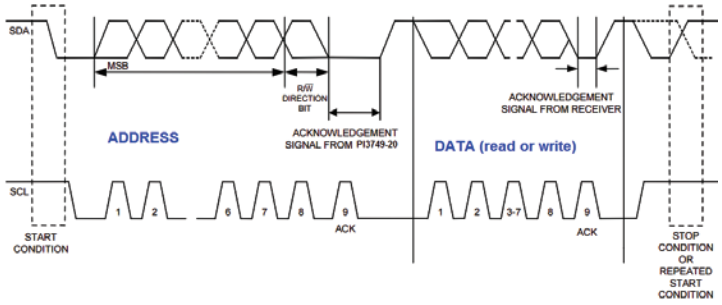


Figure 28 — *Data transfer on the I²C bus*

Per the I²C standard, the master generates all serial clock pulses, and all data is transferred MSB first.

I²C™ Parameter Readback

Fault Monitoring

Register Name	Register Address	Bit <7>	Bit <6>	Bit <5>	Bit <4>	Bit <3>	Bit <2>	Bit <1>	Bit <0>
FLT2	2	TRISE	OTP	VOUT_NEG	VOUT_OV	EAIN_HI	VIN_OV	VIN_UV	VCC_UV
FLT3	3	0	0	0	0	Q1_FIL	Q3_SIL	Q3_FIL	SLOW_IL
FLTREG_CLR	4	Write only, data ignored							

Table 4 — *PI3749-20 Fault Readback/Clear Registers*

The fault bits in the FLT2 and FLT3 registers are only latched when the regulator first stops operating due to a given fault type. If the regulator is already not operating (perhaps due to a fault protection or being disabled) then should a new fault condition occur, the fault bit associated with the new fault will not be registered.

Both versions of the PI3749-x0 will auto recover from any fault protection mechanism, once the fault is corrected. However in order to aid in monitoring of the regulator via the I²C fault monitoring registers, when a fault occurs, the associated fault bit(s) will set and latch until they are explicitly cleared by the I²C host using the FLTREG_CLR register.

A write to the FLTREG_CLR register address will clear all latched fault register bits.

Fault Bit Name	Fault Bit Location	Fault Destination
TRISE	FLT2, Bit<7>	Overtemperature Protection: The predicted maximum hot-spot temperature, based on measured temperature and loading, exceeded the maximum safe operating temperature.
OTP	FLT2, Bit<6>	Overtemperature Protection: The internal measured temperature exceeded the maximum safe operating temperature.
VOUT_NEG	FLT2, Bit<5>	V_{OUT} negative fault. The output voltage was below ground.
VOUT_OV	FLT2, Bit<4>	Output Overvoltage protection.
EAIN_HI	FLT2, Bit<3>	Current Limit: Overload Timeout.
VIN_OV	FLT2, Bit<2>	Input Overvoltage Lockout.
VIN_UV	FLT2, Bit<1>	Input Undervoltage Lockout.
VCC_UV	FLT2, Bit<0>	V_{CC} undervoltage. The internal bias supply faulted due to undervoltage.
Q1_FIL	FLT3, Bit<3>	Current Limit: Fast current limit (Q1) The peak current through Q1 and the inductor was higher than the maximum current allowed.
Q3_SIL	FLT3, Bit<2>	Current Limit: Slow current limit (Q3)
Q3_FIL	FLT3, Bit<1>	Current Limit: Fast current limit (Q3) The peak current through Q3 and the inductor was higher than the maximum current allowed.
SLOW_IL	FLT3, Bit<0>	Current Limit: Slow current limit.

Table 5 — *Fault register bit summary*

I²C Volatile Addresses for Parameter Programming

Register Name	Register Address	Readback capable?	Bit <3>	Bit <2>	Bit <1>	Bit <0>
MRGN	5	Yes	MRGN_ENA	MRGN<2>	MRGN<1>	MRGN<0>

Table 6 — *PI3749-20 Parameter Programming Volatile Registers*

MRGN: Margin Control

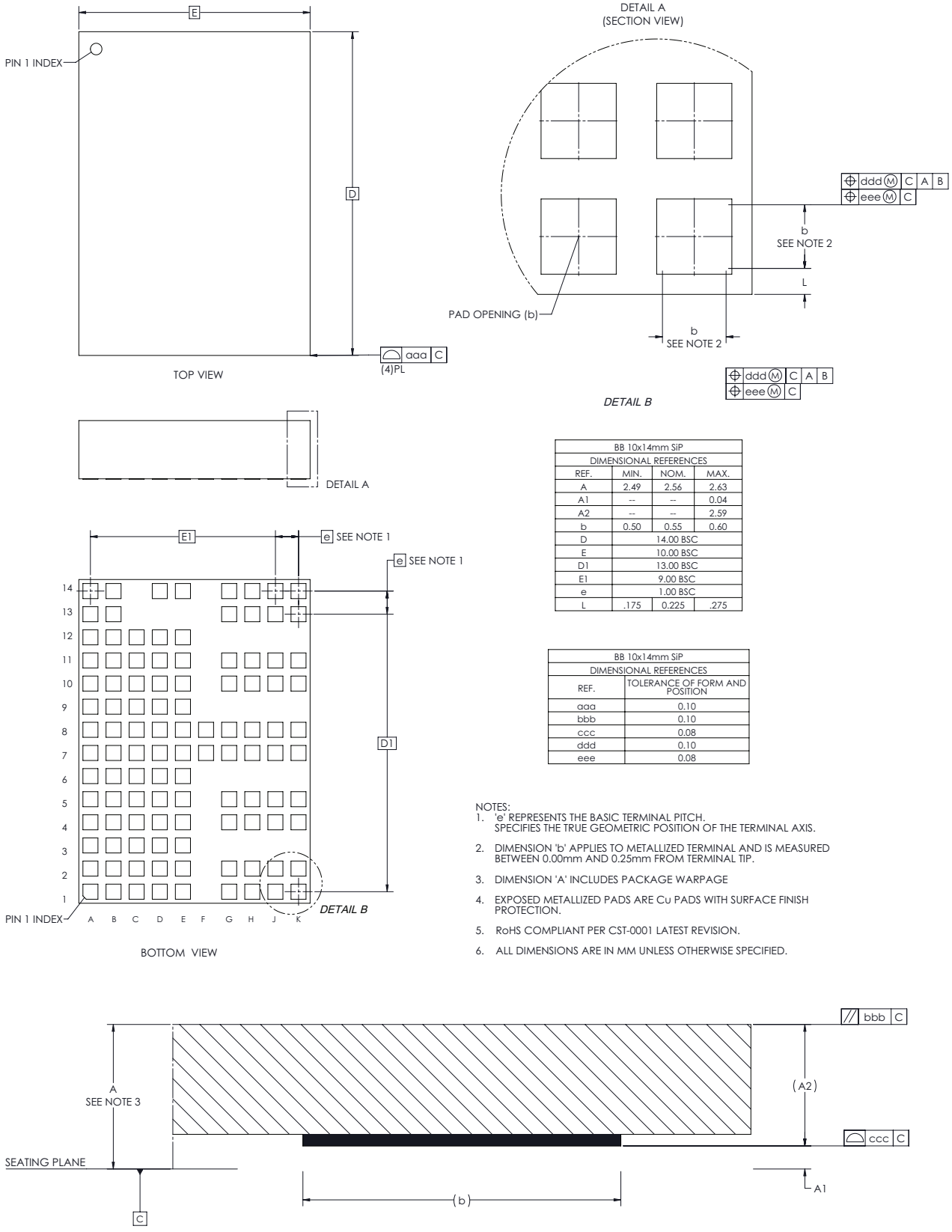
By default, output voltage margining is disabled, corresponding to B3 being cleared. In this case, the reference to the error amplifier is at its nominal value of 1.700V. When margining is enabled, the reference can be modified in 85mV steps according to Table 7.

MRGN state	MRGN data	Resultant Margin Function	
MRGN_ENA<3>	**MRGN<2..0>**	**Margin active?**	**Reference Voltage (V)**
1	100	Yes	1.360
1	101	Yes	1.445
1	110	Yes	1.530
1	111	Yes	1.615
0	xxx	No (data ignored), default	1.700
1	000	Yes	1.785
1	001	Yes	1.870
1	010	Yes	1.955
1	011	Yes	2.040

Table 7 — *Margin control register programming*

The MRGN state is always controlled by four bit wide volatile register. At power up, the register always resets to 4'b0000. The MRGN address can be freely read and written, as there are no one-time programmable fuses involved.

Package Drawings

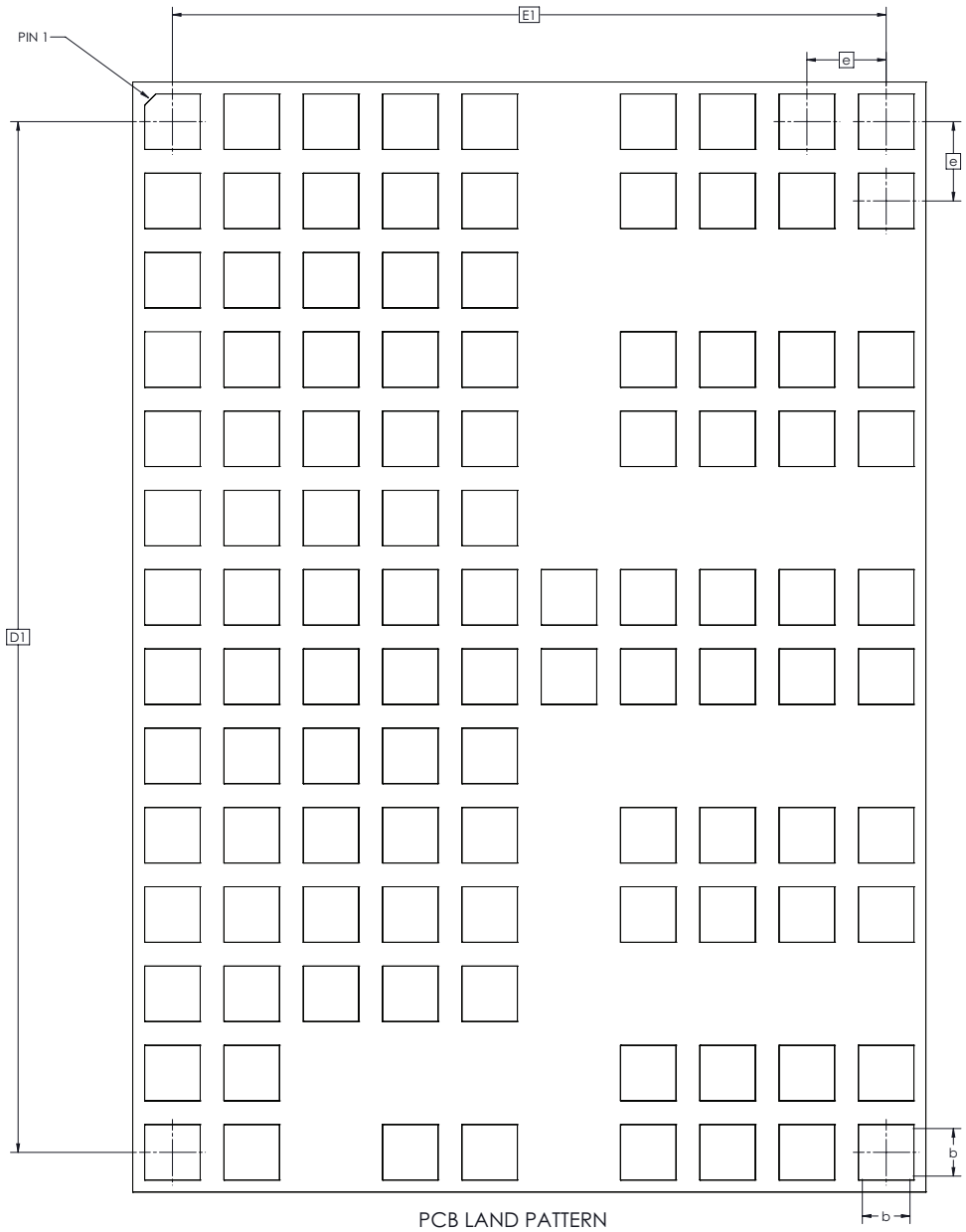


BB 10x14mm SiP			
DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	2.49	2.56	2.63
A1	--	--	0.04
A2	--	--	2.59
b	0.50	0.55	0.60
D	14.00 BSC		
E	10.00 BSC		
D1	13.00 BSC		
E1	9.00 BSC		
e	1.00 BSC		
L	.175	0.225	.275

BB 10x14mm SiP	
DIMENSIONAL REFERENCES	
REF.	TOLERANCE OF FORM AND POSITION
aaa	0.10
bbb	0.10
ccc	0.08
ddd	0.10
eee	0.08

NOTES:
1. 'e' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS.
2. DIMENSION 'b' APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.00mm AND 0.25mm FROM TERMINAL TIP.
3. DIMENSION 'A' INCLUDES PACKAGE WARPAGE
4. EXPOSED METALLIZED PADS ARE Cu PADS WITH SURFACE FINISH PROTECTION.
5. RoHS COMPLIANT PER CST-0001 LATEST REVISION.
6. ALL DIMENSIONS ARE IN MM UNLESS OTHERWISE SPECIFIED.

Receiving PCB Pattern Design Recommendations



PCB LAND PATTERN
BB 10x14mm SiP

DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
b	0.50	0.55	0.60
D1		13.00 BSC	
E1		9.00 BSC	
e		1.00 BSC	

Revision History

Revision	Date	Description	Page Number(s)
1.0	04/13/15	Initial Release	n/a
1.1	07/14/15	Updated conditions column Added additional specifications Clarified parameters and updated typical Corrected labels Corrected labels Inductor Pairing updated	7 8 9 10 15 18
1.2	08/03/15	Inductor value corrected	7-9
1.3	09/03/15	Added I^2C capability throughout	all
1.4	10/12/15	Added documentation for I^2C capability Changed frequency units for readability Reformatted for readability	1, 4, 6, 7, 8, 9 & 20 11 19
1.5	04/08/16	Updated VDIFF description	4
1.6	09/27/16	Power level updated	ALL
1.7	02/14/17	Corrections to Typical Application, Figure 24 Package drawings updated	1, 15 5, 23, 24

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