EPC2047 – Enhancement-Mode Power Transistor
Preliminary Specification Sheet

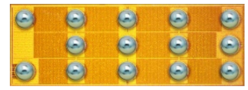
Status: Engineering

Features:

- V_{DS}, 200 V
- Maximum $R_{DS(on)}$, 10 mΩ
- I_D, 32 A

Applications:

- Multi-level AC-DC Power Supplies
- Synchronous Rectification (48 V_{OUT})
- Wireless Charging
- Solar Micro Inverters
- Robotics
- Class D Audio
- Low Inductance Motor Drives



EPC2047 eGaN® FETs are supplied in passivated die form with solder bumps.
Die Size: 4.6 mm x 1.6 mm

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage (Continuous)	200	V
I_D	Continuous (T_A = 25˚C, $R_{\theta JA}$ = 8 ˚C/W)	32	A
	Pulsed (25˚C, T_{PULSE} = 300 µs)	160	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	

Static Characteristics (T_J = 25˚C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.45 mA	200			V
I_{DSS}	Drain Source Leakage	V_{DS} = 160 V, V_{GS} = 0 V		0.1	0.3	mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		1	5	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.1	0.3	mA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 7 mA	0.8	1.6	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 20 A		7	10	mΩ
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V		2.1		V

All measurements were done with substrate shorted to source.

Thermal Characteristics

		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.8	˚C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	9.5	˚C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	52	˚C/W

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Dynamic Characteristics (T_J= 25˚C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V		875	1050	pF
C_{RSS}	Reverse Transfer Capacitance			4		
C_{OSS}	Output Capacitance			390	585	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (note 2)	V_{DS} = 0 to 100 V, V_{GS} = 0 V		450		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (note 3)			570		
R_G	Gate Resistance			0.5		Ω
Q_G	Total Gate Charge	V_{DS} = 100 V, V_{GS} = 5 V, I_D=20 A		8.2	10.2	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 100 V, I_D = 20 A		2.9		
Q_{GD}	Gate-to-Drain Charge			1.8		
$Q_{G(TH)}$	Gate Charge at Threshold			2		
Q_{OSS}	Output Charge	V_{DS} = 100 V, V_{GS} = 0 V		60	86	
Q_{RR}	Source-Drain Recovery Charge			0		

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DS}.
All measurements were done with substrate shorted to source.

Figure 1: Typical Output Characteristics at 25°C

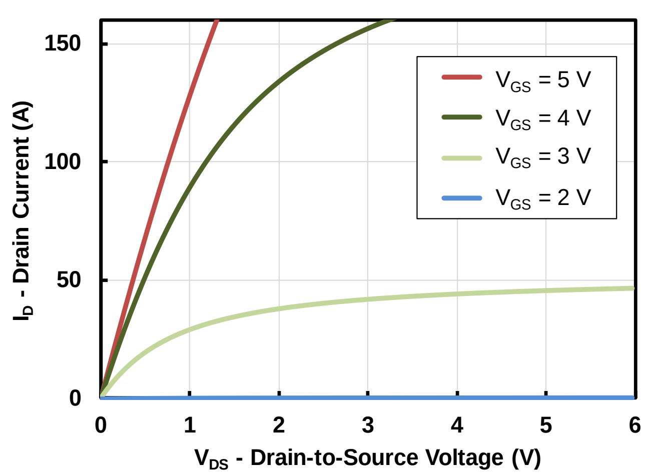


Figure 2: Transfer Characteristics

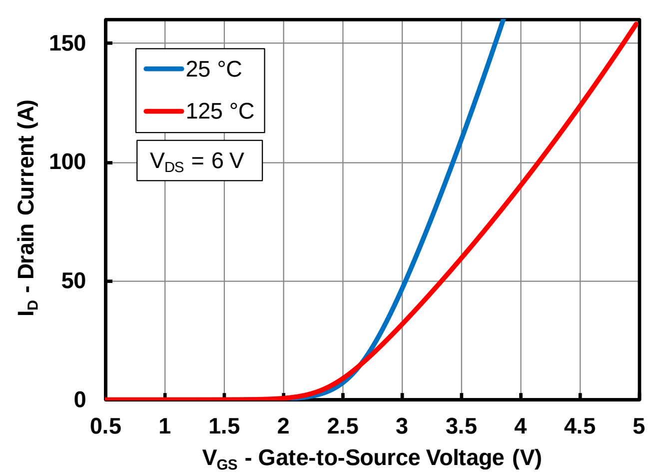


Figure 3: $R_{DS(on)}$ vs V_{GS} for Various Drain Currents

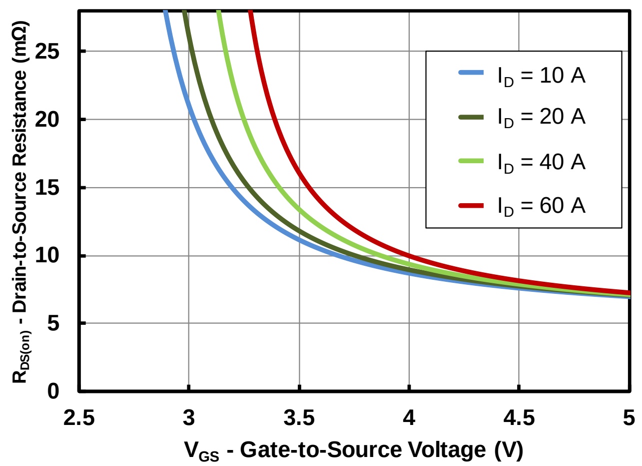


Figure 4: $R_{DS(on)}$ vs V_{GS} for Various Temperatures

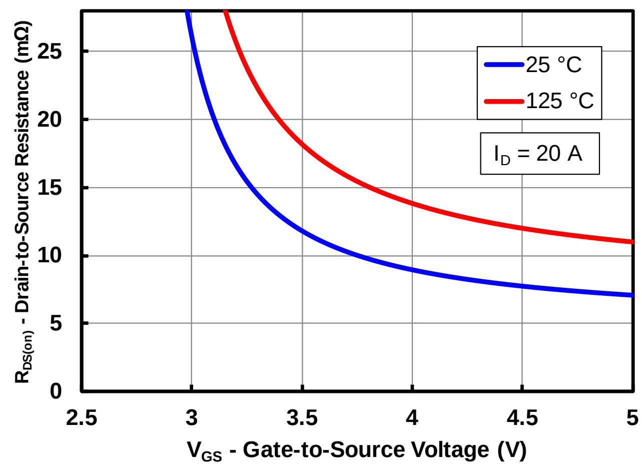


Figure 5a: Capacitance (Linear Scale)

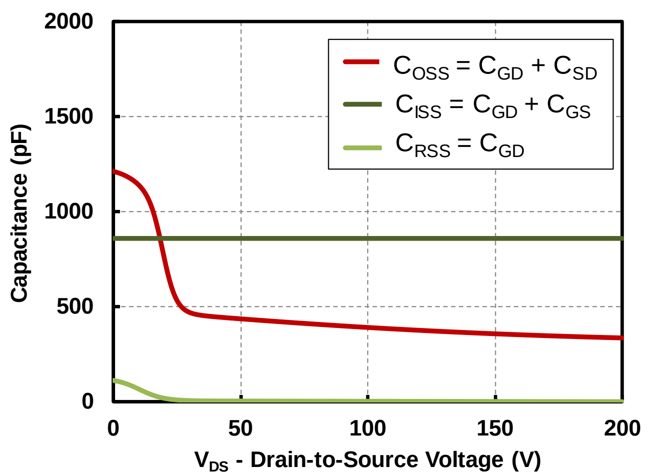


Figure 5b: Capacitance (Log Scale)

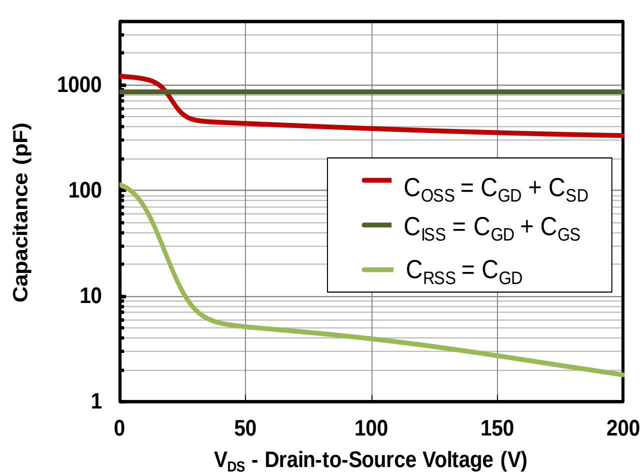


Figure 5c: Output Charge and C_{OSS} Stored Energy

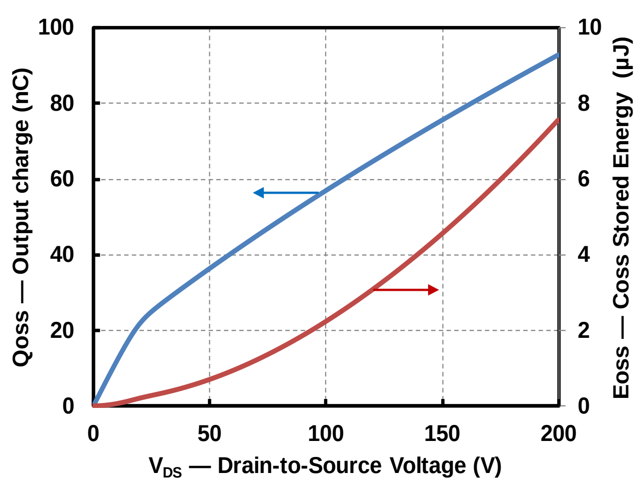


Figure 7: Gate Charge

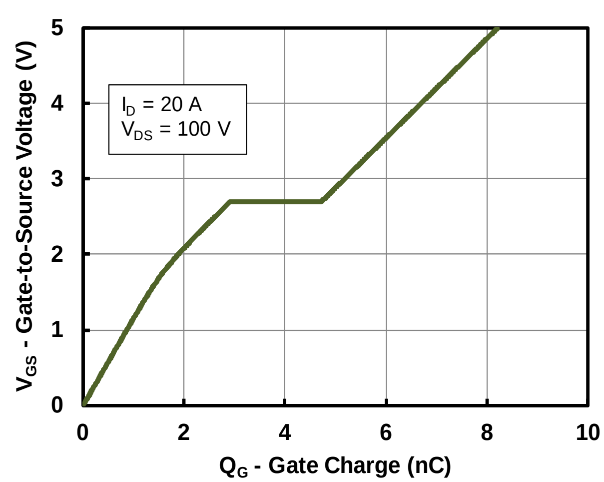


Figure 8: Reverse Drain-Source Characteristics

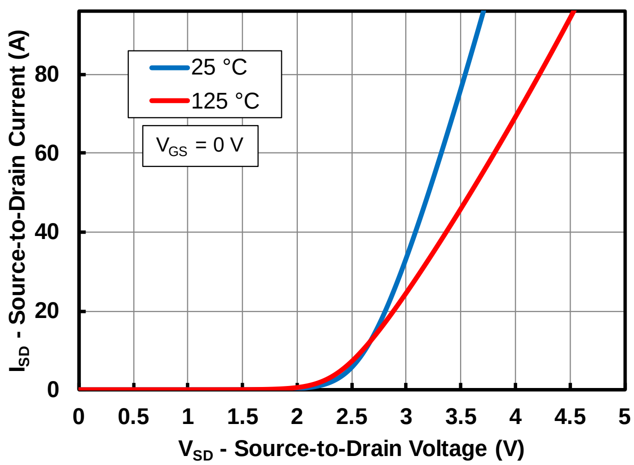


Figure 9: Normalized On-State Resistance vs Temperature

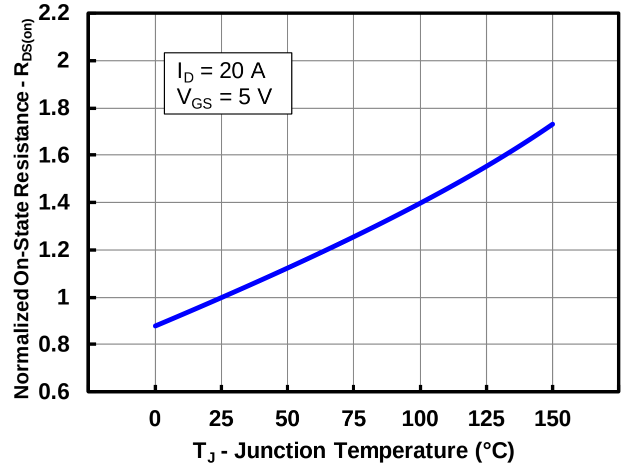


Figure 10: Normalized Threshold Voltage vs Temperature

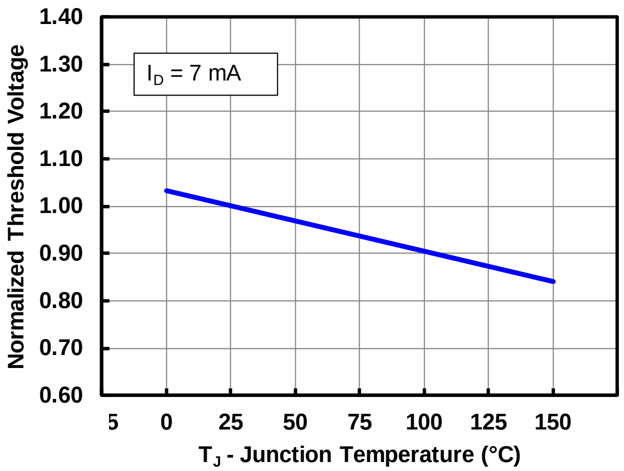


Figure 11: Safe Operating Area

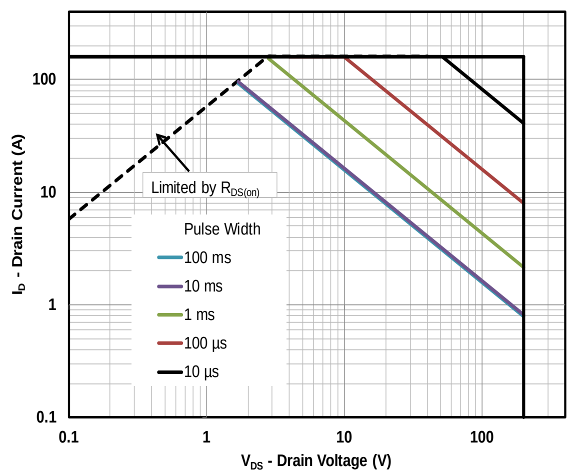
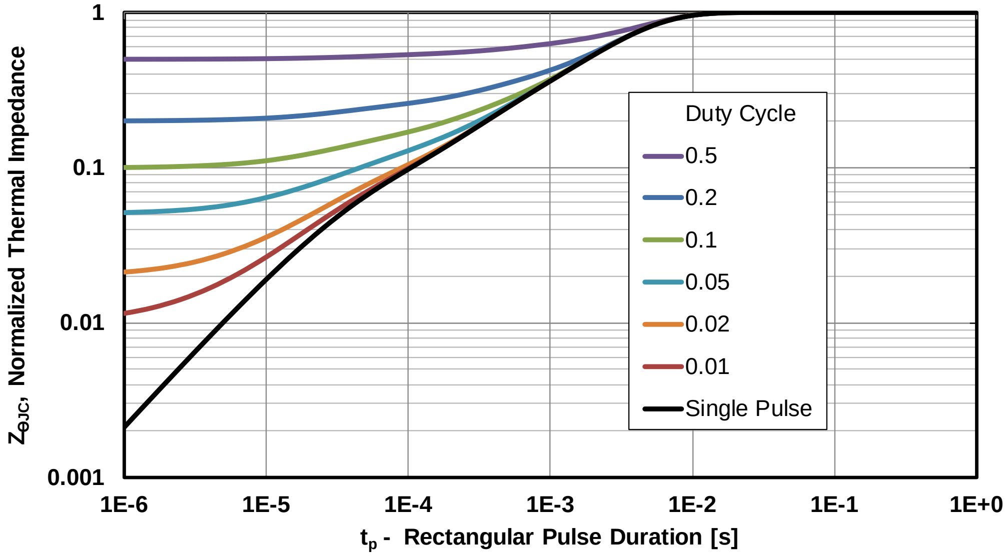
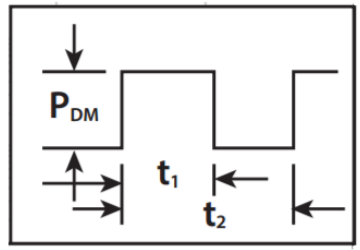


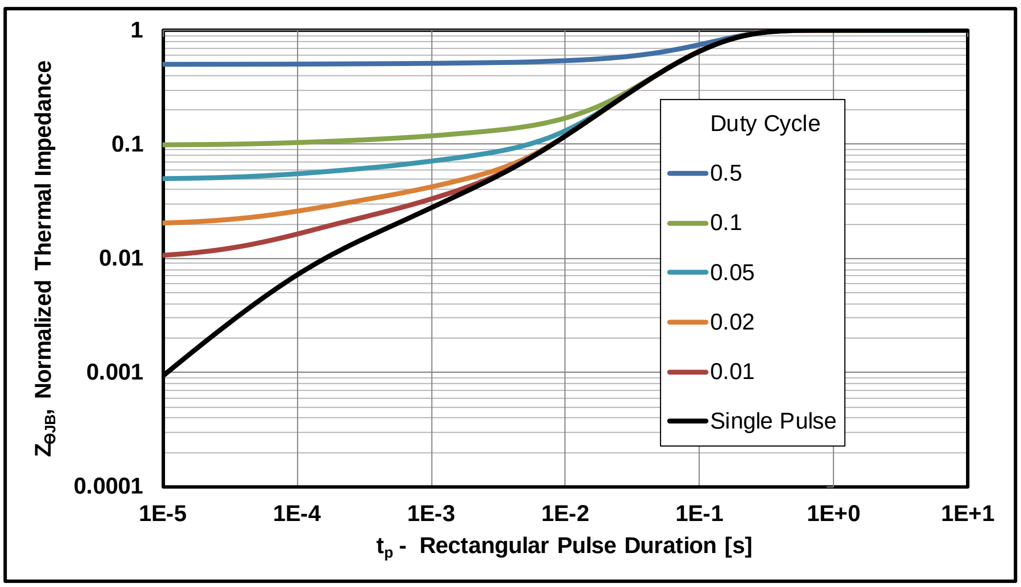
Figure 12a: Transient Thermal Response Curves (Junction-to-Case)

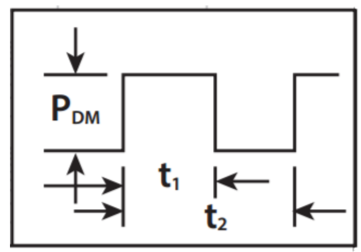




Notes:
Duty Factor: $D = t_1/t_2$
Peak $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C$

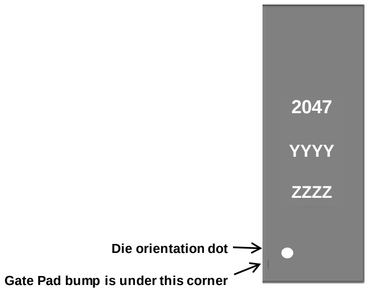
Figure 12b: Transient Thermal Response Curves (Junction-to-Board)





Notes:
Duty Factor: $D = t_1/t_2$
Peak $T_J = P_{DM} \times Z_{\theta JB} \times R_{\theta JB} + T_B$

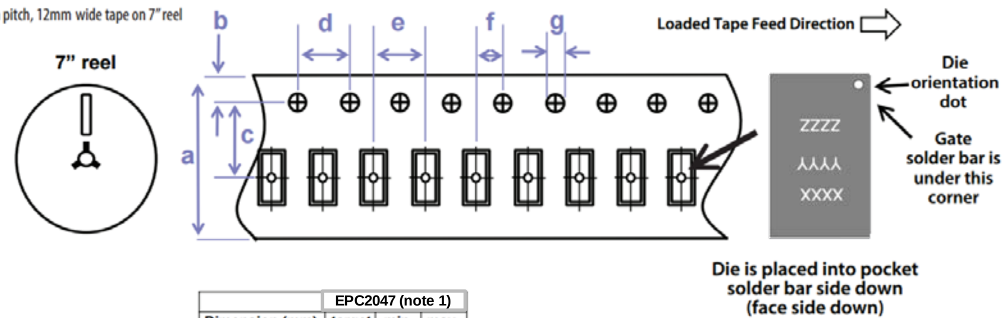
DIE MARKINGS



Part Number	Laser Marking		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2047	2047	YYYY	ZZZZ

TAPE AND REEL CONFIGURATION

4mm pitch, 12mm wide tape on 7" reel

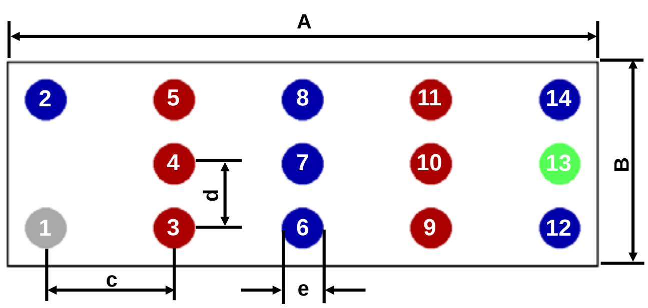


Dimension (mm)	EPC2047 (note 1) target	min	max
a	12.00	11.70	12.30
b	1.75	1.65	1.85
c (see note)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

DIE OUTLINE

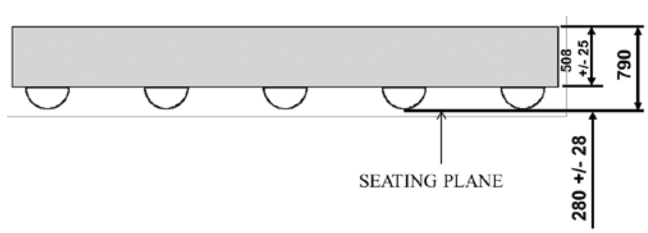
Solder Bar View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	4570	4600	4630
B	1570	1600	1630
c	1000	1000	1000
d	500	500	500
e	332	369	406

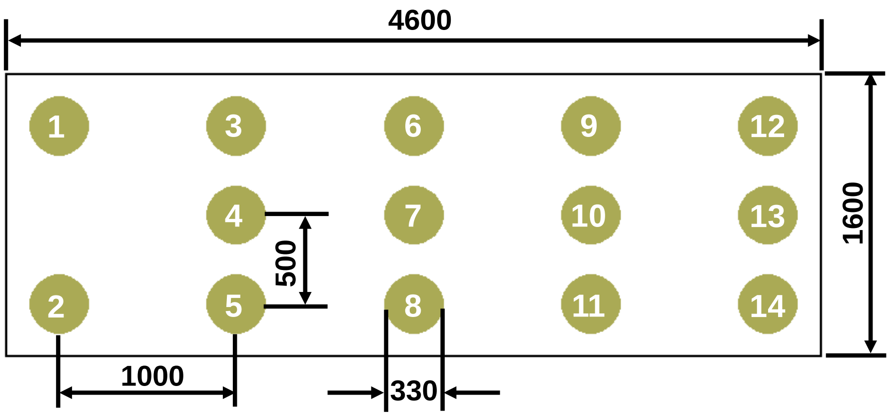
Pads 1 is Gate;
Pads 3, 4, 5, 9, 10, 11 are Drain;
Pads 2, 6, 7, 8, 12, 14 are Source;
Pad 13 is Substrate.

Side View



RECOMMENDED LAND PATTERN

(measurements in µm)

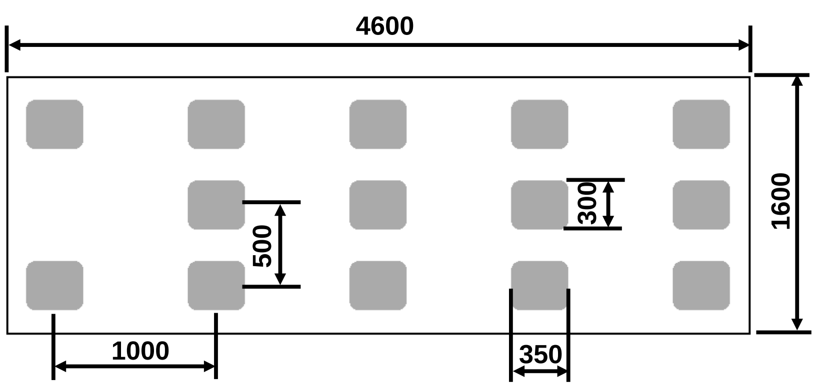


Pads 1 is Gate;
Pads 3, 4, 5, 9, 10, 11 are Drain;
Pads 2, 6, 7, 8, 12, 14 are Source;
Pad 13 is Substrate.

The land pattern is solder mask defined
Solder mask is 10µm smaller per side than bump

RECOMMENDED STENCIL DRAWING

(measurements in µm)



Recommended stencil should be 4mil (100µm) thick, must be laser cut, openings per drawing.

The corner has a radius of R60

Intended for use with SAC305 Type 3 or Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

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