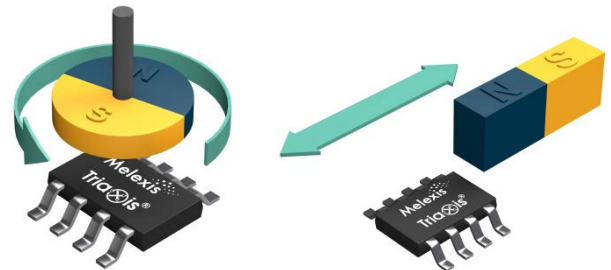


# MLX90365 Triaxis Position Sensor IC

Datasheet

## Features and Benefits

- Absolute Rotary & Linear Position Sensor IC
- Triaxis® Hall Technology
- Simple Magnetic Design
- Programmable Transfer Characteristic (Multi-Points – Piece-Wise-Linear)
- Selectable Output Mode: Analog (Ratiometric) – Pulse Width Modulation (PWM)
- 12 bit Resolution - 10 bit Thermal Accuracy
- Open/Short Diagnostics
- On Board Diagnostics
- Over-Voltage Protection
- Under-Voltage Detection
- 48 bit ID Number option
- Automotive Temperature Range
- AEC-Q100 Qualified
- Single Die – SOIC-8 Package RoHS Compliant
- Dual Die (Full Redundant) – TSSOP-16 Package RoHS Compliant
- Thermal Offset correction

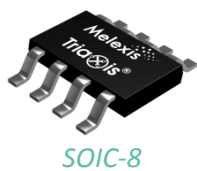


## Description

The MLX90365 is a monolithic sensor IC sensitive to the flux density applied orthogonally and parallel to the IC surface.

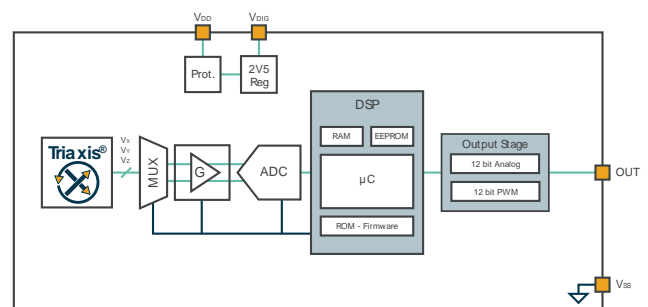
The MLX90365 is sensitive to the three components of the flux density applied to the IC (i.e.  $B_x$ ,  $B_y$  and  $B_z$ ). This allows the MLX90365 with the correct magnetic circuit to decode the absolute position of any moving magnet (e.g. rotary position from 0 to 360 Degrees or linear displacement, stroke). It enables the design of novel generation of non-contacting position sensors that are frequently required for both automotive and industrial applications.

MLX90365 reports a programmable ratiometric analog output signal compatible with any resistive potentiometer or programmable linear Hall sensor. Through programming, the MLX90365 provides also a digital PWM (Pulse Width Modulation) output characteristic.



## Applications

- Absolute Rotary Position Sensor
- Absolute Linear Position Sensor
- Pedal Position Sensor
- Steering Wheel Position Sensor
- Throttle Position Sensor
- Float-Level Sensor
- Ride Height Position Sensor
- Non-Contacting Potentiometer



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# 1. Ordering Information

Product Code	Temperature Code	Package Code	Option Code	Packing Form Code
MLX90365	E	DC	ABD-000	RE
MLX90365	E	GO	ABD-000	RE
MLX90365	K	DC	ABD-000	RE
MLX90365	K	GO	ABD-000	RE
MLX90365	L	DC	ABD-000	RE
MLX90365	L	GO	ABD-000	RE
MLX90365	L	DC	ABD-200	RE
MLX90365	L	DC	ABE-000	RE
MLX90365	L	GO	ABE-000	RE

## Legend:

Temperature Code:	E: from -40 Deg.C to 85 Deg.C K: from -40 Deg.C to 125 Deg.C L: from -40 Deg.C to 150 Deg.C
Package Code:	“DC” for SOIC-8 package “GO” for TSSOP-16 package (dual die)
Option Code:	ABD-xxx: die version XXX-000 – Standard XXX-200 – Preprogrammed – See section End-User Programmable Items
Packing Form:	“RE” for Reel “TU” for Tube
Ordering Example:	MLX90365EDC-ABD-000-RE

Table 1 – Legend

## 2. Functional Diagram

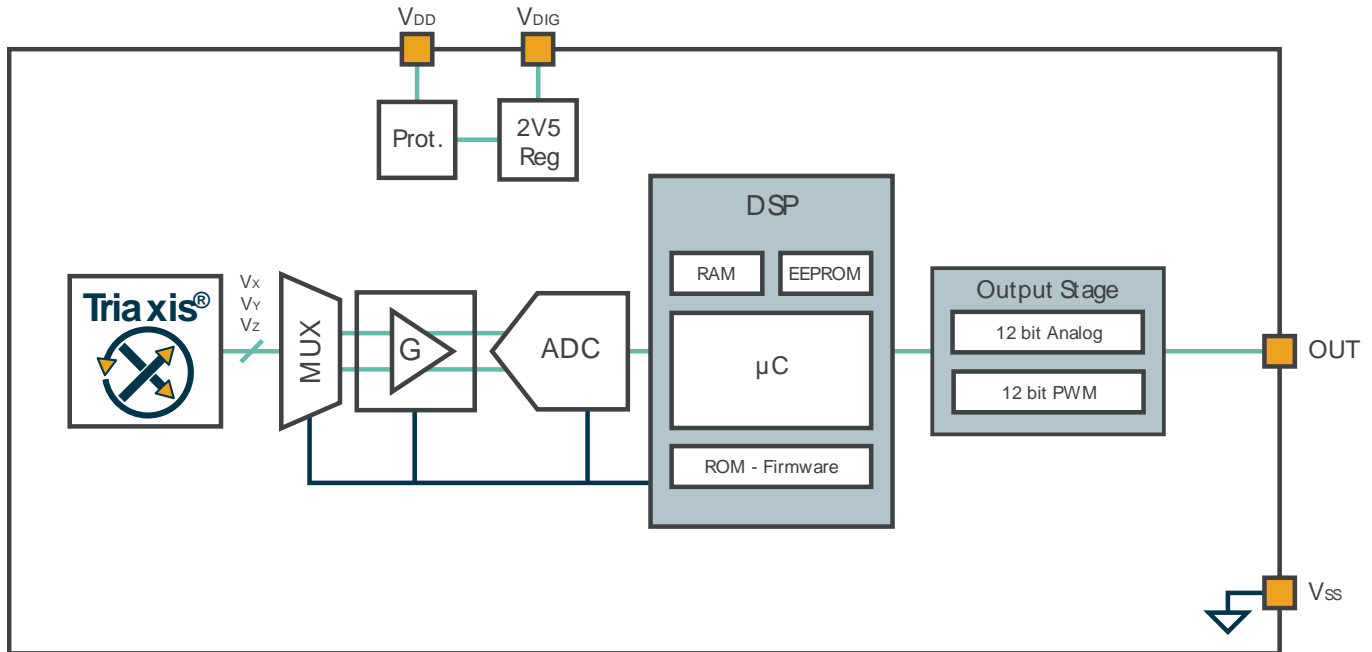


Figure 1 – Block Diagram

## 3. Glossary of Terms

Gauss (G), Tesla (T)	Units for the magnetic flux density - 1 mT = 10 G
TC	Temperature Coefficient (in ppm/Deg.C.)
NC	Not Connected
ADC	Analog-to-Digital Converter
LSB	Least Significant Bit
MSB	Most Significant Bit
DNL	Differential Non-Linearity
INL	Integral Non-Linearity
RISC	Reduced Instruction Set Computer
ASP	Analog Signal Processing
DSP	Digital Signal Processing
ATAN	Trigonometric function: arctangent (or inverse tangent)
IMC	Integrated Magneto-Concentrator (IMC®)
CoRDIC	Coordinate Rotation Digital Computer (i.e. iterative rectangular-to-polar transform)
EMC	Electro-Magnetic Compatibility
FE	Falling Edge
RE	Rising Edge
FW	Firmware
HW	Hardware
PWM	Pulse Width Modulation
%DC	Ratio T <sub>on</sub> / T <sub>period</sub> where T <sub>on</sub> is the high state duration and T <sub>period</sub> is the duration of 1

	pwm period
DAC	Digital to Analog Converter
MT3V	More than 3V Condition (when VDD >3V with 0.1V hysteresis)
MT4V	More than 4V Condition (when VDD <4V with 0.1V hysteresis)
LSD	Low Side Driver = Open drain N
PP	Push-Pull

Table 2 – Glossary of Terms

## 4. Pinout

PIN	SOIC-8	TSSOP-16
1	VDD	V <sub>DIG1</sub>
2	Test 0	V <sub>SS1</sub> (Ground <sub>1</sub> )
3	Test 2	V <sub>DD1</sub>
4	Not Used	Test 0 <sub>1</sub>
5	OUT	Test 2 <sub>2</sub>
6	Test 1	OUT <sub>2</sub>
7	V <sub>DIG</sub>	Not Used <sub>2</sub>
8	V <sub>SS</sub> (Ground)	Test 1 <sub>2</sub>
9		V <sub>DIG2</sub>
10		V <sub>SS2</sub> (Ground <sub>2</sub> )
11		V <sub>DD2</sub>
12		Test 0 <sub>2</sub>
13		Test 2 <sub>1</sub>
14		Not Used <sub>1</sub>
15		OUT <sub>1</sub>
16		Test 1 <sub>1</sub>

For optimal EMC behavior, it is recommended to connect the unused pins (Not Used and Test) to the Ground (see section 16).

## 5. Absolute Maximum Ratings

Parameter	Value
Supply Voltage, VDD (overvoltage)	+ 24 V
Reverse Voltage Protection	– 12 V (breakdown at -14 V)
Positive Output Voltage	+ 18 V (breakdown at 24 V)
Output Current (I <sub>OUT</sub> )	+ 30 mA (in breakdown)
Reverse Output Voltage	– 0.3 V
Reverse Output Current	– 50 mA (in breakdown)
Operating Ambient Temperature Range, T <sub>A</sub>	– 40°C ... + 150 Deg.C
Storage Temperature Range, T <sub>S</sub>	– 40°C ... + 150 Deg.C
Magnetic Flux Density	± 1 T

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

## 6. Electrical Specification

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Nominal Supply Voltage	VDD		4.5	5	5.5	V
Supply Current <sup>(1)</sup>	IDD	Power saving Enabled Power saving Disabled		6 8	10 <sup>(2)</sup> 12	mA
Isurge Current <sup>(3)</sup>	Isurge				20	mA
Power-On reset ( rising )	HPOR_LH	Refer to internal voltage Vdig	2	2.25	2.5	V
Power-On reset Hysteresis	HPOR_Hyst		50		200	mV
Start-up Level ( rising )	MT4V LH		3.8	4.0	4.2	V
Start-up Hysteresis	MT4V Hyst		50		200	mV
PTC Entry Level ( rising )	MT7V_LH		5.8	6.2	6.6	V
PTC Entry Level Hysteresis	MT7V_Hyst		50		200	mV
Output Short Circuit Current	I <sub>short</sub>	Vout = 0 V Vout = 5 V Vout = 18 V (T <sub>A</sub> = 25°C)			15 15 18	mA mA mA
Output Load Analog	R <sub>L</sub>	Pull-down to Ground Pull-up to 5V	4.7 4.7	10 10		kΩ kΩ
Output Load PWM	R <sub>L_PWM</sub>	Pull-down to Ground Pull-up to 5V	1 1			kΩ kΩ
Analog Saturation Output Level	Vsat_lo	Pull-up load R <sub>L</sub> ≥ 10 kΩ to 5 V Pull-up load R <sub>L</sub> ≥ 5 kΩ to 18V		0.5 2	2 3	%VDD
	Vsat_hi	Pull-down load R <sub>L</sub> ≥ 5 kΩ Pull-down load R <sub>L</sub> ≥ 10 kΩ	95 97.5	97 98.5		%VDD

1 For the dual version, the supply current is multiplied by 2.

2 To reach 10mA, the power saving option should be enabled. This option switches off and on internal blocks dynamically. It can be disabled in case of extreme emission requirements or if an analog output is required with a resistor on either supply or output line.

3 The specified value is valid during early start-up time only; the current might dynamically exceed the specified value, shortly, during the Start-up phase.



Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Digital Saturation Level Open drain Output ( $R_{L\_PWM}$ to $V_{PU}^{(4)}$ )	Vo_min	Pull-up load $R_{L\_PWM} = 1\text{ k}\Omega$ to 5V	98			% $V_{PU}^{(4)}$
		Pull-up load $R_{L\_PWM} = 1\text{ k}\Omega$ to 14V	95			
		Pull-up load $R_{L\_PWM} = 1\text{ k}\Omega$ to 18V	90			
		Pull-up load $R_{L\_PWM} < 5.6\text{ k}\Omega$ to 5V	96			
		Pull-up load $R_{L\_PWM} < 5.6\text{ k}\Omega$ to 14V	85			
		Pull-up load $R_{L\_PWM} < 5.6\text{ k}\Omega$ to 18V	73			
Active Diagnostic Output Level	Dsat_lo	Pull-up load $R_L \geq 10\text{ k}\Omega$ to 5 V		0.5	2	%VDD
		Pull-up load $R_L \geq 5\text{ k}\Omega$ to 18V		2	3	
Digital Saturation Output Level	Dsat_hi	Pull-down load $R_L \geq 5\text{ k}\Omega$	95	97		%VDD
		Pull-down load $R_L \geq 10\text{ k}\Omega$	97.5	98.5		
Passive Diagnostic Output Level (Broken Track Diagnostic) <sup>(5)</sup>	BVssPD <sup>(6)</sup>	Broken Vss & Pull-down load $R_L \geq 5\text{ k}\Omega$	95			%VDD
		Pull-down load $R_L \geq 10\text{ k}\Omega$	97.5			
	BVssPU	Broken Vss & Pull-up load $R_L \geq 1\text{ k}\Omega$	99.5	100		%VDD
Clamped Output Level	Clamp_lo	Broken VDD & Pull-down load $R_L \geq 1\text{ k}\Omega$		0	0.5	%VDD
	Clamp_hi	Broken VDD & Pull-up load $R_L \geq 5\text{ k}\Omega$			2	%VDD
Clamped Output Level	Clamp_lo	Programmable	0		100	%VDD <sup>(7)</sup>
	Clamp_hi	Programmable	0		100	%VDD <sup>(7)</sup>

As an illustration of the previous table, the MLX90365 fits the typical classification of the output span described on the Figure 2.

<sup>4</sup>  $V_{PU}$  being the pull-up voltage connected externally to the output through the pull-up resistor

<sup>5</sup> For detailed information on diagnostics, see also section Self Diagnostic

<sup>6</sup> In case the dual-die variant is used BVssPD level can be influenced. Refer to Technical note MLX90365\_Broken\_Vss\_DualDie

<sup>7</sup> Clamping levels need to be considered vs the saturation of the output stage (see Vsat\_lo and Vsat\_hi)

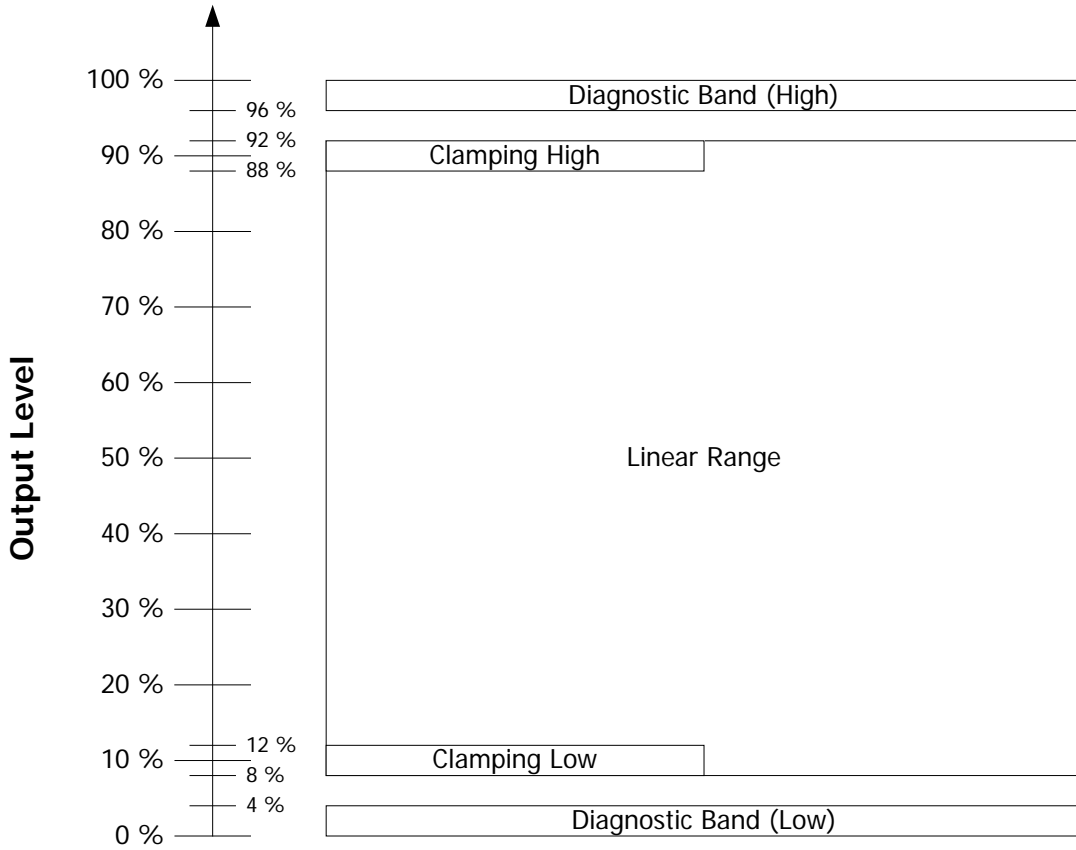


Figure 2 – Example of Output Span Classification for typical application

## 7. Isolation Specification

DC Operating Parameters at Nominal Supply Voltage (unless otherwise specified) and for  $T_A$  as specified by the Temperature suffix (E or K or L). Only valid for the package code GO i.e. dual die version.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Isolation Resistance		Between dice	4			MΩ

## 8. Timing Specification

### ANALOG OUTPUT

DC Operating Parameters at Nominal Supply Voltage (unless otherwise specified) and for TA as specified by the Temperature suffix (E or K or L).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Main Clock Frequency	Ck	All contributors included thermal drift	12.6	13.3	14	MHz
Main Clock Frequency Thermal Drift	$\Delta T_{ck}$				$\pm 3\%$	Ck <sub>NOM</sub>
Refresh Rate	t <sub>per</sub>		275	290	305	$\mu s$
Step Response Time	T <sub>s</sub>	Filter=0 <sup>(8)</sup>		657 <sup>(9)</sup>	896	$\mu s$
		Filter=1		876	1195	
		Filter=2		1095	1494	
Watchdog	T <sub>wd</sub>		114.5	118	121.5	ms
Start-up Cycle	T <sub>su</sub>	Analog OUT Slew-rate excluded			5	ms
Analog OUT Slew-rate		Mode 1 from COUT = 47 nF to 330 nF	25	37		V/ms
		Mode 2 up to COUT = 10 nF	300	320		
		Mode 3 up to COUT = 47 nF	17	19		
		Mode 4 up to COUT = 330 nF	1.8	2.5		

<sup>8</sup> See section 14.6 for details concerning Filter parameter

<sup>9</sup> This represents a theoretical average response time

## PWM OUTPUT

DC Operating Parameters at Nominal Supply Voltage  $V_{DD} = V_{PU}$  (unless otherwise specified) and for  $T_A$  as specified by the Temperature suffix L.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PWM Frequency	$F_{PWM}$	Programmable Range (PWM Output Enabled)	100		1000	Hz
		Initial Tolerance (25 Deg.C.)			± 2%	FPWM
		After EOL tuning (25 Deg.C.)			± 1%	FPWM
		Thermal/Lifetime drift			± 3%	FPWM
Start-up Cycle	Tsu	PWM OUT Slew-rate excluded 100Hz		11.8	13	ms
		250Hz		5.8	7	
		1000Hz		5.8	7	
Digital Output Rise Time		LSD – Mode 5				
		4.7nF, $R_L = 1\text{ k}\Omega$ PU		10	12	$\mu\text{s}$
		4.7nF, $R_L = 10\text{ k}\Omega$ PU		100	120	$\mu\text{s}$
		10nF, $R_L = 1\text{ k}\Omega$ PU		20	24	$\mu\text{s}$
		PP – Mode 7				
		4.7nF, $R_L = 1\text{ k}\Omega$ PU		3	5	$\mu\text{s}$
4.7nF, $R_L = 10\text{ k}\Omega$ PU		3	5	$\mu\text{s}$		
10nF, $R_L = 1\text{ k}\Omega$ PU		4	7	$\mu\text{s}$		
Digital Output Fall Time		LSD – Mode 5				
		4.7nF, $R_L = 1\text{ k}\Omega$ PU		2	3	$\mu\text{s}$
		4.7nF, $R_L = 10\text{ k}\Omega$ PU		2	3	$\mu\text{s}$
		10nF, $R_L = 1\text{ k}\Omega$ PU		4	7	$\mu\text{s}$
		PP – Mode 7				
		4.7nF, $R_L = 1\text{ k}\Omega$ PU		2	3	$\mu\text{s}$
4.7nF, $R_L = 10\text{ k}\Omega$ PU		2	3	$\mu\text{s}$		
10nF, $R_L = 1\text{ k}\Omega$ PU		4	7	$\mu\text{s}$		

## 9. Accuracy Specification

### 9.1. ANALOG OUTPUT

DC Operating Parameters at Nominal Supply Voltage (unless otherwise specified) and for  $T_A$  as specified by the Temperature suffix (E or K or L).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
ADC Resolution on the raw signals sine and cosine <sup>(10)</sup>	RADC			15		bits
Thermal Offset Drift #1 <sup>(11)</sup> at the DSP input (excl. DAC and output stage)		Temperature suffix E	-60		+60	LSB <sub>15</sub>
		Temperature suffix K	-60		+60	
		Temperature suffix L	-90		+90	
Thermal Offset Drift #2 (DAC and Output Stage)			-0.2		+0.2	%VDD
Thermal Drift of Sensitivity Mismatch <sup>(12)</sup>		XY axis – Temp. suffix E	-0.3		+0.3	%
		XY axis – Temp. suffix K & L	-0.5		+0.5	
		XZ (YZ) axis – Temp. suffix E	-1		+1	
		XZ (YZ) axis – Temp. suffix K & L	-1		+1	
Magnetic Angle phase error		$T_A = 25^\circ\text{C}$ – XY axis	-0.3		0.3	Deg.
		$T_A = 25^\circ\text{C}$ – XZ axis	-2		2	
		$T_A = 25^\circ\text{C}$ – YZ axis	-2		2	
Thermal Drift of Magnetic Angle phase error		XY axis, XZ (YZ) axis		0.01		Deg.
XY – Intrinsic Linearity Error <sup>(13)</sup>	Le	$T_A = 25^\circ\text{C}$ – factory trim. “SMISM”	-1		1	Deg
XZ - Intrinsic Linearity Error <sup>(13)</sup>	Le	$T_A = 25^\circ\text{C}$ – “k” trimmed for XZ	-2.5	$\pm 1.2$ 5	+2.5	Deg

<sup>10</sup> 16 bits corresponds to 15 bits + sign. Internal computation is performed using 16 bits.

<sup>11</sup> For instance, in case of a rotary position sensor application, Thermal Offset Drift #1 equal  $\pm 60\text{LSB}_{15}$  yields to max.  $\pm 0.3$  Deg. angular error for the computed angular information (output of the DSP). This is only valid if  $k = 1$ .

<sup>12</sup> For instance, in case of a rotary position sensor application, Thermal Drift of Sensitivity Mismatch equal  $\pm 0.5\%$  yields to max.  $\pm 0.15$  Deg. angular error for the computed angular information (output of the DSP).

<sup>13</sup> The Intrinsic Linearity Error refers to the IC itself (offset, sensitivity mismatch, orthogonality) taking into account an ideal rotating field for  $B_x$  and  $B_y$ . Once associated to a practical magnetic construction and the associated mechanical and magnetic tolerances, the output linearity error increases. However, it can be improved with the multi-point end-user calibration.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
YZ - Intrinsic Linearity Error <sup>(13)</sup>	Le	T <sub>A</sub> = 25°C – “k” trimmed for YZ	-2.5	±1.2 5	+2.5	Deg
Analog Output Resolution	RDAC	12b DAC (Theoretical, Noise free)		0.02 5		%VDD/L SB12
		INL (before EOL calibration)	-4		+4	LSB12
		DNL	0.05	1	3	LSB12
Output stage Noise		Clamped Output		0.05	0.075	%VDD
Noise pk-pk <sup>(14)</sup>		Filter = 0, 40mT		0.10	0.2	Deg
		Filter = 2, 20mT		0.10	0.2	
Ratiometry Error		4.5V ≤ VDD ≤ 5.5V	-0.05		+0.05	%VDD
		LT4V ≤ VDD ≤ MT7V	-0.1		+0.1	

## 9.2. PWM OUTPUT

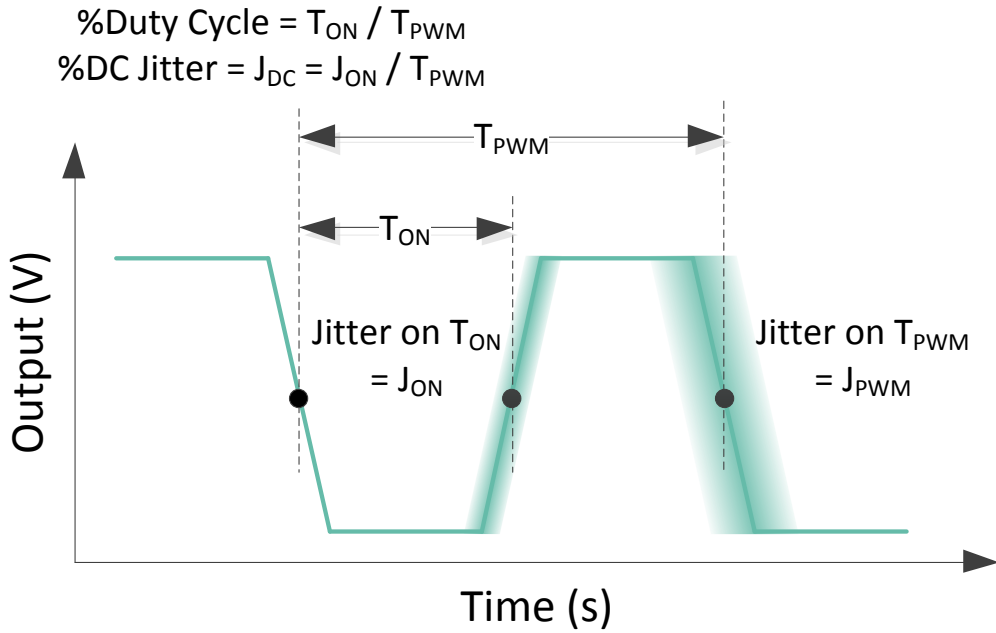
DC Operating Parameters at VDD = VPU = 5V (unless otherwise specified) and for T<sub>A</sub> as specified by the Temperature suffix L.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PWM Output Resolution	RPWM	12 bits		0.025		%DC/ LSB
PWM % DC Jitter	JDC	LSD – Mode5				%DC
		100Hz, 4.7nF, RL = 1 kΩ PU		±0.003	±0.016	
		200Hz, 4.7nF, RL = 1 kΩ PU		±0.005	±0.02	
		1000Hz, 4.7nF, RL = 1 kΩ PU		±0.009	±0.035	
		PP – Mode7				
		100Hz, 4.7nF, RL = 1 kΩ PU		±0.003	±0.016	
200Hz, 4.7nF, RL = 1 kΩ PU		±0.005	±0.02			
1000Hz, 4.7nF, RL = 1 kΩ PU		±0.009	±0.035			

<sup>14</sup> Noise pk-pk (peak-to-peak) is here intended as 6 times the Noise standard Deviation. The application diagram used is described in the recommended wiring. For detailed information, refer to section Filter in application mode (Section 14.6).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PWM Freq Jitter	JPWM	LSD – Mode5 100-1000 Hz, 4.7nF, R <sub>L</sub> = 1 kΩ PU		±0.04	±0.15	Hz
		PP – Mode7 100-1000 Hz, 4.7nF, R <sub>L</sub> = 1 kΩ PU		±0.04	±0.15	
PWM % DC thermal drift		LSD – Mode5 100Hz, 4.7nF, R <sub>L</sub> = 1 kΩ PU		±0.02	±0.03	%DC
		200Hz, 4.7nF, R <sub>L</sub> = 1 kΩ PU		±0.02	±0.03	
		1000Hz, 4.7nF, R <sub>L</sub> = 1 kΩ PU		±0.02	±0.05	
		PP – Mode7 100Hz, 4.7nF, R <sub>L</sub> = 1 kΩ PU		±0.02	±0.03	
		200Hz, 4.7nF, R <sub>L</sub> = 1 kΩ PU		±0.02	±0.03	
		1000Hz, 4.7nF, R <sub>L</sub> = 1 kΩ PU		±0.02	±0.05	
PWM % DC Level drift (Trigger level= 25/50/75%)		LSD – Mode5 100Hz, 4.7nF, R <sub>L</sub> = 1 kΩ PU		±0.1	±0.15	%DC
		PP – Mode7 100Hz, 4.7nF, R <sub>L</sub> = 1 kΩ PU		±0.05	±0.1	
PWM % DC Level drift		100Hz – PP Application Diagram (see below) R <sub>s</sub> = 0, 50, 100, 150 Ohm Tolerance on R ± 20% Tolerance on C ± 30%		±0.05	±0.1	%DC

Jitter is defined by  $\pm 3 \sigma$  for 1000 successive acquisitions with clamped output, see figure below.



Parameter	Symbol	Test Conditions
PWM T <sub>ON</sub> , T <sub>PWM</sub>	T <sub>ON</sub> T <sub>PWM</sub>	Trigger level = 50 % V <sub>pp</sub>
Rise time, Fall time		10% and 90% of amplitude
Jitter	J <sub>ON</sub> J <sub>PWM</sub>	± 3 σ for 1000 successive acquisitions
Duty Cycle	% DC	T <sub>ON</sub> / T <sub>PWM</sub>

Figure 3 – MLX90365 PWM measurement conditions.



## 10. Magnetic Specification

DC Operating Parameters at Nominal Supply Voltage (unless otherwise specified) and for TA as specified by the Temperature suffix (E or K or L).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Magnetic Flux Density	$B_x, B_y^{(15)}$	$\sqrt{B_x^2 + B_y^2}$			70 <sup>(16)</sup>	mT
Magnetic Flux Density	$B_z$				126	mT
Magnetic Flux Norm	Norm	$\sqrt{B_x^2 + B_y^2 + (B_z/1.2)^2}$	20 <sup>(17)</sup>			mT
IMC Gain in X and Y <sup>(18)</sup>	GainIMC <sub>x</sub> y		1.2	1.4	1.8	
IMC Gain in Z <sup>(18)</sup>	GainIMC <sub>z</sub>		1.1		1.3	
k factor	k	GainIMC <sub>xy</sub> / GainIMC <sub>z</sub>	1	1.2	1.5	
Magnet Temperature Coefficient	TCm		-2400		0	ppm/°C

## 11. CPU & Memory Specification

The DSP is based on a 16 bit RISC  $\mu$ Controller. This CPU provides 2.5 Mips while running at 10 MHz.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
ROM				10		KB
RAM				384		B
EEPROM				128		B

## 12. Traceability Information

Every device contains a unique ID that is programmed by Melexis in the EEPROM. Melexis strongly recommends storing this value during the EOL (End-Of-Line) programming to ensure full traceability of the final product.

<sup>15</sup> The condition must be fulfilled for at least one field  $B_x$  or  $B_y$ .

<sup>16</sup> Above 70 mT, the IMC<sup>®</sup> starts saturating yielding to an increase of the linearity error.

<sup>17</sup> Below 20 mT, the performances slightly degrade due to a reduction of the signal-to-noise ratio, signal-to-offset ratio.

<sup>18</sup> This is the magnetic gain linked to the Integrated Magneto Concentrator structure. This is the overall variation. Within one lot, the part to part variation is typically  $\pm 10\%$  versus the average value of the IMC gain of that lot.

These parameters shall never be erased during the EOL programming.

Parameter	Comments	Default Values	Parameter # bit
MELEXISID1	Melexis identification reference	MLX	16
MELEXISID2	Melexis identification reference	MLX	16
MELEXISID3	Melexis identification reference	MLX	16

## 13. End-User Programmable Items

Parameter	Comments	Standard	PPAR	# bit
OUT mode	Define the output stage mode	1	1	3
DIAG mode	Diagnostic mode	7	7	3
DIAG Level	Diagnostic Level	0	0	1
MAPXYZ	Mapping fields for output angle	0	0	2
CLAMP_HIGH	Clamping High (50%)	50%	10%	16
CLAMP_LOW	Clamping Low (50%)	50%	90%	16
FILTER	Filter mode selection	0	1	2
SMISM	Sensitivity mismatch factor X,Y	MLX	MLX	15
k	Sensitivity mismatch factor X (Y) , Z	MLX	N/A	15
SEL_k	Affected signal component by k: B1 or B2 (in combination of MAPXYZ)	0	0	1
GAINMIN	Low threshold for virtual gain	00h	00h	8
GAINMAX	High threshold for virtual gain	28h	28h	8
GAINSATURATION	Gain Saturates on MIN and MAX	0h	0h	1
FIELDTHRESH_Low	Field limit under which a fault is reported	10mT	10mT	8
FIELDTHRESH_High	Field limit above which a fault is reported	FFh	FFh	8
PWM	PWM function	0h	N/A	1
PWMPOL	PWM polarity	0h	N/A	1
PWMT	PWM Frequency (trimmed at 200Hz)	MLX	N/A	8
DC_FAULT	PWM Duty Cycle if Fault	1h	N/A	8

Parameter	Comments	Standard	PPAR	# bit
DC_FTL	PWM Duty Cycle if Field Strength Too Low	1h	N/A	8
DC_WEAK	PWM Duty Cycle if Weak Magnet	1h	N/A	8
WEAKMAGTHRESH	Weak Magnet threshold Byte (1LSB = 1mT)	0h	N/A	8
DP	Discontinuity point	0h	0h	15
CW	Clock Wise	0h	0h	1
FHYST	Hysteresis filter	0h	0h	8
4POINTS	Selection of correction method 4 or 16 pts	1h	1h	1
LNR_S0	4pts – Initial Slope	0 %/deg	0 %/deg	16
LNR_A_X	4pts – AX Coordinate	0 deg	0 deg	16
LNR_A_Y	4pts – AY Coordinate	10 %	10 %	16
LNR_A_S	4pts – AS Coordinate	0.22%/deg	0.22%/deg	16
LNR_B_X	4pts – BX Coordinate	360 deg	360 deg	16
LNR_B_Y	4pts – BY Coordinate	100%	100%	16
LNR_B_S	4pts – BS Coordinate	0 %/deg	0 %/deg	16
LNR_C_X	4pts – CX Coordinate	360 deg	360 deg	16
LNR_C_Y	4pts – CY Coordinate	100%	100%	16
LNR_C_S	4pts – CS Coordinate	0 %/deg	0 %/deg	16
LNR_D_X	4pts – DX Coordinate	360 deg	360 deg	16
LNR_D_Y	4pts – DY Coordinate	100%	100%	16
LNR_D_S	4pts – DS Coordinate	0 %/deg	0 %/deg	16
W	17pts – Output angle range	0h	N/A	4
USERID1	Cust. ID reference	Bin1	Bin1	16
USERID2	Cust. ID reference	204h	3h	16
USERID3	Cust. ID reference	MLX	MLX	16
LNR_Yn	17pts – Y-coordinate point n (n = 2,1,2 ...16)	N/A	N/A	16
DIAG Settings	16 Bit Diagnostics enabling	FDFh	4080h	16
CRC_DISABLE	Enable EERPOM CRC check ( 3131h= disable)	0h	0h	16

Parameter	Comments	Standard	PPAR	# bit
MEMLOCK	Write-protects USER/MLX EEPROM param.	0h	3h	2
ANGLEOFSSLOPECOLD	Temperature coefficient offset at cold temperatures For ABE only	0h	N/A	8
ANGLEOFSSLOPEHOT	Temperature coefficient offset at hot temperatures For ABE only	0h	N/A	8

Melexis strongly recommends checking the User Identification data (Parameters USERID) during EOL programming.

## 14. Description of End-User Programmable Items

### 14.1. Output modes

#### 14.1.1. OUT mode

Defines the Output Stage mode (analog, digital, high-impedance, standby) in application.

Output mode[2:0]	Type	Descriptions	Comments
0	Disable	Output HiZ	Not recommended
1	Analog	Analog Rail-to-Rail for Coutmin = 47nF	Analog Only (Default)
2	Analog	Analog Rail-to-Rail for Coutmax = 10nF	Analog Only
3	Analog	Analog Rail-to-Rail for Coutmax = 68nF	Analog Only
4	Analog	Analog Rail-to-Rail for Coutmax = 330nF	Analog Only
5	Digital	open drain NMOS	PWM
6	Digital	open drain PMOS	PWM
7	Digital	Push-Pull	PWM

### 14.1.2. PWM Output Mode

If PWM output mode is selected, the output signal is a digital signal with Pulse Width Modulation (PWM). The PWM polarity is selected by the PWMPOL parameter:

- PWMPOL = 1 for a low level at 100%
- PWMPOL = 0 for a high level at 100%

The PWM frequency is selected by the PWMT parameter. The following table provides typical code for different target PWM frequency and for both low and high speed modes.

PWM F (Hz)	PWMT (LSB) @13.3MHz	PWM res. (µs)	PWM res. (%)	PWM res. (bit)
100	44333	0.240	0.0024	15
250	17733	0.240	0.006	14
500	8866	0.240	0.012	13
1000	4433	0.240	0.024	12

Notes:

- A more accurate trimming can be performed to take into account initial tolerance of the main clock.
- The PWM frequency is subjected to the same tolerances as the main clock (see  $\Delta T_{CK}$ ).

## 14.2. Output Transfer Characteristic

There are 2 different possibilities to define the transfer function (LNR):

- With 4 arbitrary points (defined on X and Y coordinates) and 5 slopes
- With 17 equidistant points for which only the Y coordinates are defined.

Parameter	LNR type	Value	Unit
CLOCKWISE	Both	0 → CounterClockWise 1 → ClockWise	LSB
DP	Both	0 ... 359.9999	deg
LNR_A_X LNR_B_X LNR_C_X LNR_D_X	Only 4 pts	0 ... 359.9999	deg
LNR_A_Y LNR_B_Y LNR_C_Y LNR_D_Y	Only 4 pts	0 ... 100	%
LNR_S0 LNR_A_S LNR_B_S LNR_C_S LNR_D_S	Only 4 pts	-17 ... 0 ... 17	%/deg
LNR_Y0 LNR_Y1 ... LNR_Y16	Only 17 pts	-50 ... + 150	%
W	Only 17 pts	65.5 ... 360	Deg
CLAMP_LOW	Both	0 ... 100	%
CLAMP_HIGH	Both	0 ... 100	%
ANGLEOFSSLOPECOLD	Only ABE	0..255	LSB
ANGLEOFSSLOPEHOT	Only ABE	0..255	LSB

### 14.2.1. Enable scaling Parameter (only for LNR type 4 pts)

This parameter enables to scale LNR\_x\_Y from -50% - 150% according to the following formula

$$(Scaled\ Out)\%V_{DD} = 2 \times Out\%V_{DD} - 50\%$$

## 14.2.2. CLOCKWISE Parameter

The CLOCKWISE parameter defines the magnet rotation direction.

- CCW is defined by the 1-4-5-8 pin order direction for the SOIC-8 package and 1-8-9-16 pin order direction for the TSSOP-16 package.
- CW is defined by the reverse direction: 8-5-4-1 pin order direction for the SOIC-8 and 16-9-8-1 pin order direction for the TSSOP-16 package.

Refer to the drawing in the sensitive spot positioning sections (Section 19.3 and 19.6).

## 14.2.3. Discontinuity Point (or Zero Degree Point)

The Discontinuity Point defines the  $0^\circ$  point on the circle. The discontinuity point places the origin at any location of the trigonometric circle. The DP is used as reference for all the angular measurements.

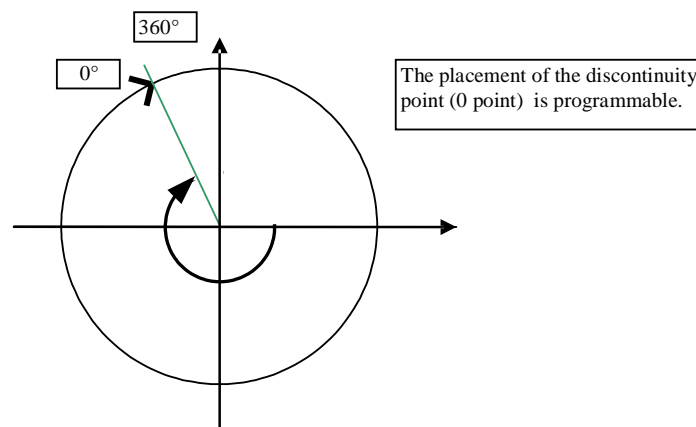


Figure 4 - Discontinuity Point Positioning

## 14.2.4. 4-Pts LNR Parameters

The LNR parameters, together with the clamping values, fully define the relation (the transfer function) between the digital angle and the output signal.

The shape of the MLX90365 transfer function from the digital angle value to the output voltage is described by the drawing below. Six segments can be programmed but the clamping levels are necessarily flat.

Two, three, or even six calibration points are then available, reducing the overall non-linearity of the IC by almost an order of magnitude each time. Three to six calibration points will be preferred by customers looking for excellent non-linearity figures. Two-point calibrations will be preferred by customers looking for a cheaper calibration set-up and shorter calibration time.

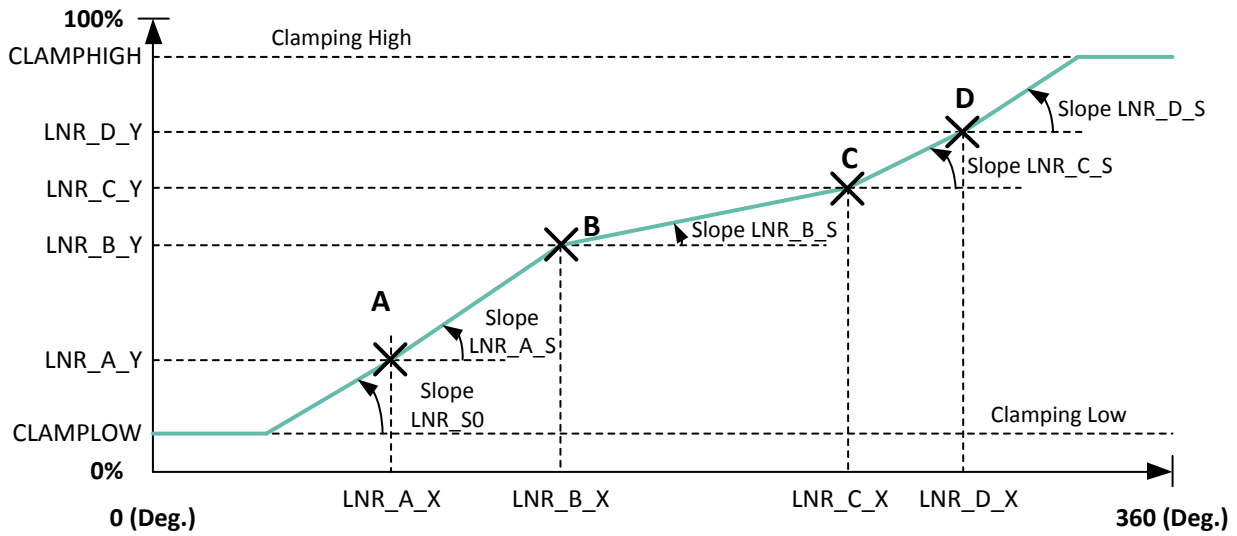


Figure 5 - 4-Points LNR Parameters

### 14.2.5. 17-Points LNR Parameters

The LNR parameters, together with the clamping values, fully define the relation (the transfer function) between the digital angle and the output signal.

The shape of the MLX90365 transfer function from the digital angle value to the output voltage is described by the drawing below. In the 17-Points mode, the output transfer characteristic is Piece-Wise-Linear (PWL).

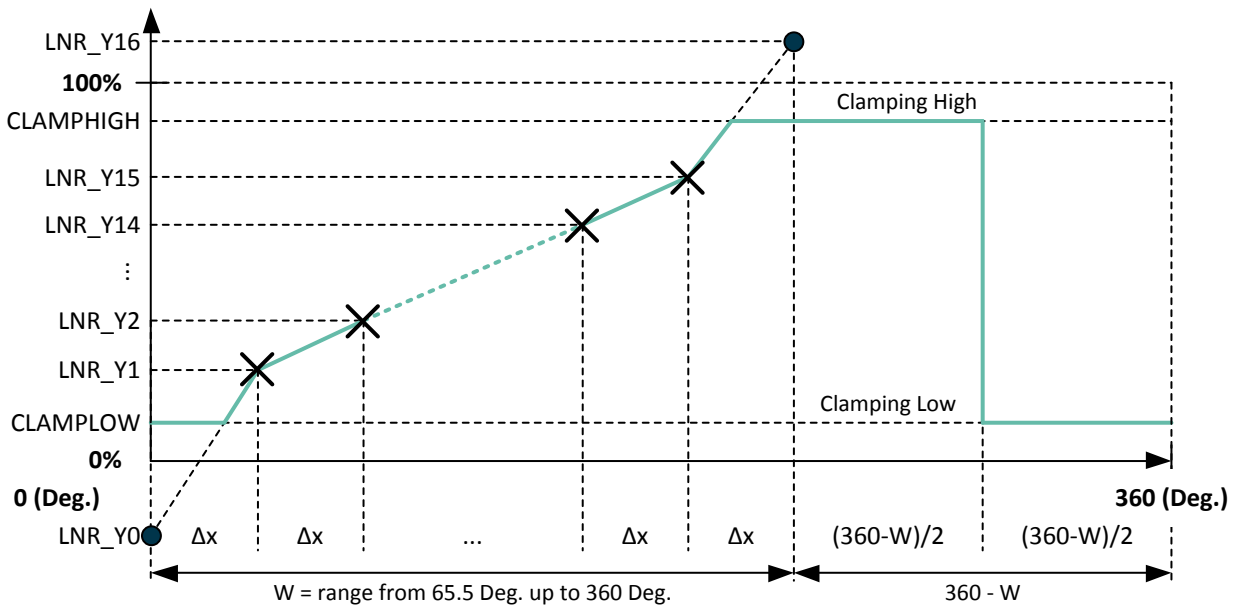


Figure 6 - Input range from 65.5° up to 360°

All the Y-coordinates can be programmed from -50% up to +150% to allow clamping in the middle of one segment (like on the Figure 6), but the output value is limited to CLAMPLOW and CLAMPHIGH values.



Between two consecutive points, the output characteristic is interpolated.

The parameter W determines the input range on which the 17 points (16 segments) are uniformly spread:

W	Range	$\Delta x$	W	Range	$\Delta x$
0 (0000b)	360.0deg	22.5deg	8	180.0deg	11.3deg
1	320.0deg	20.0deg	9	144.0deg	9.0deg
2	288.0deg	18.0deg	10	120.0deg	7.5deg
3	261.8deg	16.4deg	11	102.9deg	6.4deg
4	240.0deg	15.0deg	12	90.0deg	5.6deg
5	221.5deg	13.8deg	13	80.0deg	5.0deg
6	205.7deg	12.9deg	14	72.0deg	4.5deg
7	192.0deg	12.0deg	15 (1111b)	65.5deg	4.1deg

Outside of the selected range, the output will remain in clamping levels.

### 14.2.6. CLAMPING Parameters

The clamping levels are two independent values to limit the output voltage range. The CLAMPLOW parameter adjusts the minimum output voltage level. The CLAMPHIGH parameter sets the maximum output voltage level. Both parameters have 16 bits of adjustment and are available for both LNR modes. In analog mode, the resolution will be limited by the D/A converter (12 bits) to 0.024%V<sub>DD</sub>. In PWM mode, the resolution will be 0.024%DC.

### 14.2.7. Thermal Output Offset correction Specific to ABE version

On the version ABE, the two parameters ANGLEOFSSLOPEHOT and ANGLEOFSSLOPECOLD, defined in the section 13, enable to add, to the output an offset depending on the measured temperature depicted in the Figure 7.

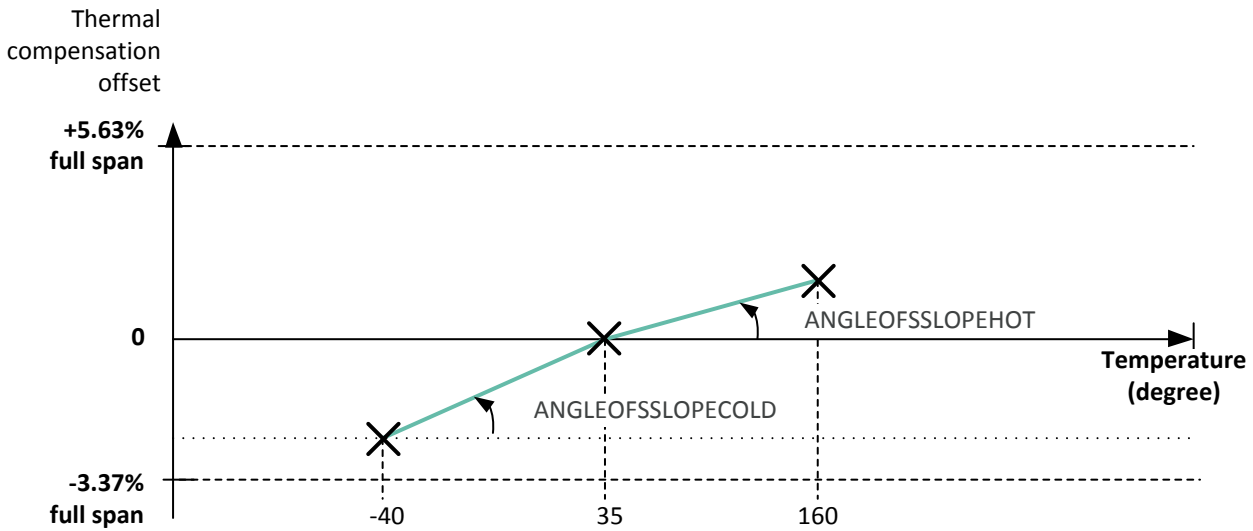


Figure 7 - Input range from -40° up to 150°

The thermal offset is added before the clamping (see section 14.2.6). The span of this offset is +5.63/-3.37% of the full output scale. The added thermal offset varies with temperature see the equation below and the thermal coefficient is defined separately before (used coefficient ANGLEOFSSLOPECOLD) and after 35°C (used coefficient ANGLEOFSSLOPEHOT).

If temperature is higher than 35°C then:

$$\text{output} \leq \text{output} - \Delta T * \text{ANGLEOFSSLOPEHOT}$$

If temperature is lower than 35°C then:

$$\text{output} \leq \text{output} - \Delta T * \text{ANGLEOFSSLOPECOLD}$$

Where output is the calculated output adjusted by the thermal correction offset  $\Delta T * \text{ANGLEOFSSLOPECOLD}$ . Where  $\Delta T$  is the difference between current temperature and reference temperature 35degreeC. The output correction capability at hot and room (extreme temperature and maximum value of ANGLEOFSSLOPEHOT and ANGLEOFSSLOPECOLD) are given in the table below.

Parameter	min	typ	max	Unit
Output correction correction capability at 160DegC	5%	5.62%		of Full span
Output correction correction capability at -40DegC	3.09%	-3.372%		of Full span

### 14.3. Identification

Parameter	Value
MELEXISID1	0...65535
MELEXISID2	0...65535
MELEXISID3	0...65535
USERID1	0...65535
USERID2	0...65535
USERID3	0...65535

Identification number: 48 bits (3 words) freely useable by Customer for traceability purpose.

### 14.4. Lock

The MEMLOCK write protects all the EEPROM parameters set by the Melexis and user. Once the lock is enabled, it is not possible to change the EEPROM values anymore.

Note that the Memlock bits should be set by the solver function "MemLock".

### 14.5. Sensor Front-End

Parameter	Value
MAPXYZ	0 .. 3
SMISM	0 .. 32768
k	0 .. 32768
SEL_k	0 or 1
GAINMIN	0 ... 41
GAINMAX	0 ... 41
GAINSATURATION	0.. 1

### 14.5.1. MAPXYZ

The MAPXYZ parameter defines which fields are used to calculate the angle. The different possibilities are described in the tables below.

This 2 bits value selects the first (B1) and second (B2) field components according the table below.

MAPXYZ	B1	B2	Angular
0 – 00b	X	Y	XY mode
1 – 01b	Zx	X	XZx mode
2 – 10b	Y	Zx	YZx mode

Note: MAPXYZ = 3 is not recommended.

### 14.5.2. SMISM, k and SEL\_k Parameters

#### (i) SMISM

When the mapping (B1=X, B2=Y) is selected, SMISM defines the sensitivity mismatch factor that is applied on B1, B2; When another B1, B2 mapping is selected, this parameter is “don’t care”.

This parameter is trimmed at factory; Melexis strongly recommends TO NOT overwrite it for optimal performances.

#### (ii) k

When the mapping (B1=X, B2=Y) is **NOT** selected, k defines the sensitivity mismatch factor that is applied on B1 or B2 (according to parameter SEL\_k – see below). When the mapping (B1=X, B2=Y) is selected, this parameter is “don’t care”.

This parameter is trimmed at factory for mapping (B1=Z, B2=X). Melexis recommends to fine trim it when a smaller linearity error (Le) is required and a different mapping than (B1=X, B2=Y) is selected.

#### (iii) SEL\_k

When the mapping (B1=X, B2=Y) is **NOT** selected, SEL\_k defines the component on which the sensitivity mismatch factor k (see above): SEL\_k = 0 means  $B1 \rightarrow k \cdot B1$  and SEL\_k = 1 means  $B2 \rightarrow k \cdot B2$ .

### 14.5.3. GAINMIN and GAINMAX Parameters

GAINMIN and GAINMAX define the thresholds on the gain code outside which the fault “GAIN out of Spec.” is set;

If GAINSATURATION is set, then the virtual gain code is saturated at GAINMIN and GAINMAX, and no Diagnostic fault is set since the saturations applies before the diagnostic check.

## 14.6. Filter

Parameter	Value	Parameter
FILTER	0...2	FILTER
FHYST	0...255	FHYST

The MLX90365 includes 2 types of filters:

- Hysteresis Filter: programmable by the FHYST parameter
- Low Pass FIR Filters controlled with the FILTER parameter

### 14.6.1. Hysteresis Filter

The FHYST parameter is a hysteresis filter. The output value of the IC is not updated when the digital step is smaller than the programmed FHYST parameter value. The output value is modified when the increment is bigger than the hysteresis. The hysteresis filter reduces therefore the resolution to a level compatible with the internal noise of the IC. The hysteresis must be programmed to a value close to the noise level. (1 LSB = ± 0.012%)

### 14.6.2. FIR Filters

The MLX90365 features 2 FIR filter modes controlled with Filter = 1...2. Filter = 0 corresponds to no filtering. The transfer function is described below:

$$y_n = \frac{1}{\sum_{i=0}^j a_i} \sum_{i=0}^j a_i x_{n-i}$$

The filters characteristic is given in the following table:

Filter	0	1	2
J No	0	1	3
Type	Disable	Finite Impulse Response	
Coefficients a <sub>i</sub>	1	11	1111
Title	No filter	ExtraLight	Light
99% Response Time	1	2	4
Efficiency RMS (dB)	0	3.0	6.0

## 14.7. Programmable Diagnostic Settings

### 14.7.1. DIAG mode

The Diag mode defines the Output Stage mode in case of diagnostic.

DIAG mode [2:0]	Type	Descriptions	Comments
0	Disable	Output HiZ	Not recommended
5	Digital	open drain NMOS	
6	Digital	open drain PMOS	
7	Digital	Push-Pull	

### 14.7.2. DIAG Level

The Diag level determines the reporting level (diagnostic low, diagnostic high) during start-up (both analog and PWM mode), or during a fault reporting (Only in Analog mode).

In PWM mode, the fault reporting level shall in principle be 0 when the leading edge is a rising edge, (resp. 1 for a falling edge) in order to detect the first cycle after start-up. MLX recommends then DIAG Level = PWMPOL.

### 14.7.3. Field Strength Diagnostic

#### (i) FIELDTHRESHLOW

Defines the field strength limit under which a fault is reported. The run-time field strength estimation (FieldStrength) is compared to  $2^8 * \text{FIELDTHRESHLOW}$ .

The sensitivity of FIELDTHRESHLOW is typically 1mT/LSB. By default it is programmed to 10mT

#### (ii) FIELDTHRESHHIGH

Defines the field strength limit under which a fault is reported. See above for more details.

### 14.7.4. PWM Diagnostic

#### (i) DC\_FAULT

Defines the duty-cycle that is outputted in case of diagnostic reporting.

#### (ii) WEAKMAGTHRESH

Defines the threshold on the field strength which determines the weak magnet condition; when WEAKMAGTHRESH = 0, there is no reporting of weak magnet condition.

### (iii) DC\_FTL

Defines the duty-cycle that is outputted in case of Field Too Low; the Field Too Low Diagnostic is stronger than the Weak Magnet Diagnostic, from 0% till 255% by steps of (100/256)%

### (iv) DC\_WEAK

Defines the duty-cycle that is outputted in case of Weak Magnet, from 0% till 255% by steps of (100/256)%

## 14.7.5. Diagnostic Features

It is recommended to enable the diagnostic features for safety critical applications.

Refer to Application\_note\_Diagnostic\_Behavior\_90365 for EE\_CRC\_Enable function description and for Diagnostic features which can be enabled by user.

## 14.8. EEPROM endurance

Although the EEPROM is used for Calibration Data Storage (similarly to an OTPROM), the MLX90365 embedded EEPROM is qualified to guarantee an endurance of minimum 1000 write cycles at 125°C for (engineering/calibration purpose).

## 15. Self Diagnostic

The MLX90365 provides numerous self-diagnostic features. Those features increase the robustness of the IC functionality as it will prevent the IC to provide erroneous output signal in case of internal or external failure modes (“fail-safe”).

Diagnostic Item	Action	Effect on Outputs	Type	Monitoring Rate	Reporting Rate
Start-up phase Diagnostics					
RAM March C-10N Test	Fail-safe mode ** ** CPU reset after 120ms	Diagnostic low/ high Reporting (optional)	Digi HW	n/applicable (start-up only)	n/applicable (start-up only)
Watchdog BIST	Fail-safe mode ** ** CPU reset after 120ms	Diagnostic low/ high Reporting (optional)	Digi HW	n/applicable (start-up only)	n/applicable (start-up only)
FieldTooLow, W/ Programmable Threshold	Diagnostic ( No Debouncing )	Diagnostic low/high Reporting (optional)	Environ &Analog	n/applicable (start-up only)	n/applicable (start-up only)

Diagnostic Item	Action	Effect on Outputs	Type	Monitoring Rate	Reporting Rate
FieldTooHigh w/ Programmable Threshold	Diagnostic ( No Debouncing )	Diagnostic low/high Reporting (optional)	Environ &Analog	n/applicable (start-up only)	n/applicable (start-up only)
WeakMagnet Diagnostic	Diagnostic ( No Debouncing )	Diagnostic low/high Reporting (optional)	Environ	n/applicable (start-up only)	n/applicable (start-up only)
Under Voltage Monitoring <i>SUPPLYMONI</i> = ( <i>MT3VB</i> ) OR ( <i>MT4VB</i> )	Start-up on Hold ** ** CPU reset after 120ms	Diagnostic low/high	Environ &Analog	n/applicable (start-up only)	n/applicable (start-up only)
Over Voltage Monitoring <i>MT7V</i>	PTC entry	Output in High- Impedance	Environ	n/applicable (start-up only)	n/applicable (start-up only)
Temperature Sensor Monitor <i>TEMPMONI</i> <sup>(19)</sup>	Debouncing (programmable)	Diagnostic low/high Reporting (optional)	Analog	Not applicable	n/applicable (start-up only)

### Back-Ground Loop Diagnostics

ROM 16bit checksum ( continuous )	Fail-safe mode ** ** CPU reset after 120ms	Diagnostic low//high Reporting (optional)	Digi HW	80 · DTI <sub>DIG</sub>	80 · DTI <sub>DIG</sub>
RAM Test ( continuous )	Fail-safe mode ** ** CPU reset after 120ms	Diagnostic low//high Reporting (optional)	Digi HW	16 · DTI <sub>DIG</sub>	16 · DTI <sub>DIG</sub>
EEPROM 8 bit CRC Check (continuous)	Fail-safe mode ** ** CPU reset after 120ms	Diagnostic low/high Reporting (optional)	Digi HW	1 · DTI <sub>DIG</sub> (ABB) 5 · DTI <sub>DIG</sub> (ABD)	1 · DTI <sub>DIG</sub> (ABB) 5 · DTI <sub>DIG</sub> (ABD)

<sup>19</sup> The temperature monitor can be enabled only if the supply slew rate is higher than 0.5V/ms for slower rise time, please contact Melexis



Diagnostic Item	Action	Effect on Outputs	Type	Monitoring Rate	Reporting Rate
Watchdog ( continuous )	CPU reset	--	Digi HW	120ms	n/a
<b>DSP Loop Diagnostics</b>					
ADC Clipping ADCCLIP	Debouncing (programmable)	Diagnostic low/high Reporting (optional)	Environ & Analog	5/20 · DTI <sub>ANA</sub>	$DTI_{ANA} \times \frac{\text{Diag\_Debounce\_Thresh}}{\text{Diag\_Debounce\_Stepup}}$
FieldTooLow, W/ Programmable Threshold	Debouncing (programmable)	Diagnostic low/high Reporting (optional)	Environ & Analog	2/20 · DTI <sub>ANA</sub>	$DTI_{ANA} \times \frac{\text{Diag\_Debounce\_Thresh}}{\text{Diag\_Debounce\_Stepup}}$
FieldTooHigh w/ Programmable Threshold	Debouncing (programmable)	Diagnostic low/high Reporting (optional)	Environ & Analog	2/20 · DTI <sub>ANA</sub>	$DTI_{ANA} \times \frac{\text{Diag\_Debounce\_Thresh}}{\text{Diag\_Debounce\_Stepup}}$
WeakMagnet Diagnostic	Debouncing (programmable)	Diagnostic low/high Reporting (optional)	Environ	1/20 · DTI <sub>ANA</sub>	1 · DTI <sub>ANA</sub>
Virtual Gain Code Out-of- spec GAINOOS	Debouncing (programmable)	Diagnostic low/high Reporting (optional)	Environ & Analog	2/20 · DTI <sub>ANA</sub>	$DTI_{ANA} \times \frac{\text{Diag\_Debounce\_Thresh}}{\text{Diag\_Debounce\_Stepup}}$
Virtual Gain Code Saturation [GAINMIN..GAIN MAX]	Saturation (optional)	Gain Saturated @ GAINMIN-GAINMAX	Environ & Analog	n/applicable Not a diagnostic	n/applicable Not a diagnostic
ADC Monitor (Analog to Digital Converter) ADCMONI	Debouncing (programmable)	Diagnostic low/high Reporting (optional)	Analog HW	1 · DTI <sub>ANA</sub>	$DTI_{ANA} \times \frac{\text{Diag\_Debounce\_Thresh}}{\text{Diag\_Debounce\_Stepup}}$
Under Voltage Monitoring SUPPLYMONI = (MT3VB) OR (MT4VB)	Supply Debouncing (programmable)	Diagnostic low/high Reporting (optional)	Environ & Analog	1 · DTI <sub>ANA</sub>	$DTI_{ANA} \times \frac{\text{Diag\_Debounce\_Thresh}}{\text{Diag\_Debounce\_Stepup}}$
Over Voltage Monitoring MT7V	PTC entry after PTC Debouncing	Output in High- Impedance	Environ	8/20 · DTI <sub>ANA</sub>	8/20 · DTI <sub>ANA</sub>

Diagnostic Item	Action	Effect on Outputs	Type	Monitoring Rate	Reporting Rate
Temperature Sensor Monitor <i>TEMPMONI</i>	Debouncing (programmable)	Diagnostic low/high Reporting (optional)	Analog	1 · DTI <sub>ANA</sub>	$\frac{DTIANA \times \text{Diag\_Debounce\_Thresh}}{\text{Diag\_Debounce\_Stepup}}$
Temperature > 170degC (± 20) Temperature < -60degC (± 20)	Saturate value used for the compensations to -40degC and +150degC resp.	No effect	Environ & Analog	N/A Not a diagnostics	N/A Not a diagnostic

**Hardware Diagnostics ( continuously checked by dedicated Logic )**

Read/Write Access out of physical memory	Fail-safe mode ** ** CPU reset after 120ms	Diagnostic Low/High	Digi HW	N/A Immediate Diagnostic	N/A Immediate Diagnostic
Write Access to protected area (IO and RAM Words)	Fail-safe mode ** ** CPU reset after 120ms	Diagnostic low/high	Digi HW	N/A	N/A
Unauthorized Mode Entry	Fail-safe mode ** ** CPU reset after 120ms	Diagnostic low/high	Digi HW	N/A	N/A
EEPROM Error Correcting Code ( Hamming correction )	(Transparent) Error Correction	no effect	Digi HW	N/A	N/A

**Hardware Diagnostics ( continuously checked by dedicated Analog circuits )**

Broken VSS	CPU Reset on recovery	Pull down load => Diagnostic High Pull up load => Diagnostic High	Environ	n/a immediate Diagnostic	n/a immediate Diagnostic
Broken VDD	CPU Reset on recovery	Pull down load => Diagnostic Low Pull up load => Diagnostic Low	Environ	n/a immediate Diagnostic	n/a immediate Diagnostic
Resistive Cable Test	Start-up on Hold	Diagnostic low/high	Environ	n/a immediate Diagnostic	n/a immediate Diagnostic.

Dimension	Min	Typ	Max	Unit
DTI <sub>ANA</sub>	5.7	6.0	6.3	ms
DTI <sub>DIG</sub>	3.9	7.2	10 <sup>(20)</sup>	ms

Table 3: Timing Specification @13.16 MHz

## 16. Recommended Application Diagrams

### 16.1. MLX90365 in SOIC-8 Package

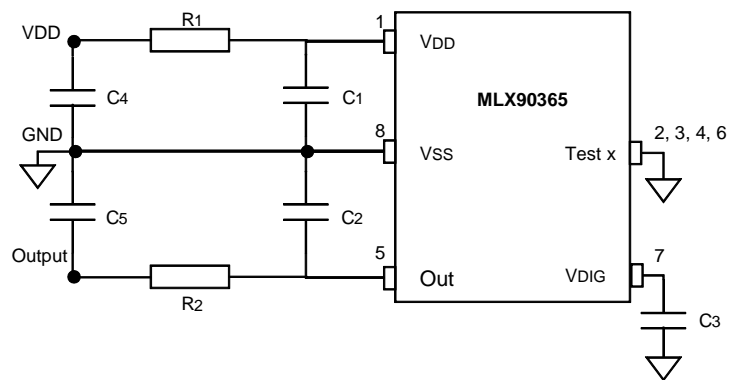


Figure 8 – Recommended wiring for the MLX90365 in SOIC-8 package

Output	Compact PCB routing			EMC robust PCB routing			Remarks
	Min	Typ.	Max	Min	Typ.	Max	
C1	100 nF	100 nF	1 uF	47 nF	100 nF	1 uF	Close to the pin
C2 (20)	47 nF	100 nF	330 nF	47 nF	100 nF	330 nF	Close to the pin
C3	47 nF	100 nF	220 nF	47 nF	100 nF	220 nF	Close to the pin
C4	-	-	-	500 pF	1 nF	10 nF	Connector Side
C5	-	-	-	500 pF	1 nF	10 nF	Connector Side
R1	-	-	-	0 Ω	10 Ω	33 Ω	Increased ratiometry error
R2	-	-	-	10 Ω	50 Ω	100 Ω	

<sup>20</sup> Corresponds to 20 output refresh

Output	Compact PCB routing			EMC robust PCB routing			Remarks
	Min	Typ.	Max	Min	Typ.	Max	
C1	100 nF	100 nF	1 uF	47 nF	100 nF	1 uF	Close to the pin
C2	22 nF	4.7 nF	22 nF	2.2 nF	4.7 nF	22 nF	Close to the pin
C3	47 nF	100 nF	220 nF	47 nF	100 nF	220 nF	Close to the pin
C4	-	-	-	500 pF	1 nF	10 nF	Connector Side
C5	-	-	-	500 pF	1 nF	2.2 nF	Connector Side
R1	-	-	-	0 Ω	10 Ω	33 Ω	Impacts the Voltage on VDD pin
R2	-	-	-	10 Ω	50 Ω	100 Ω	

## 16.2. MLX90365 in TSSOP-16 Package

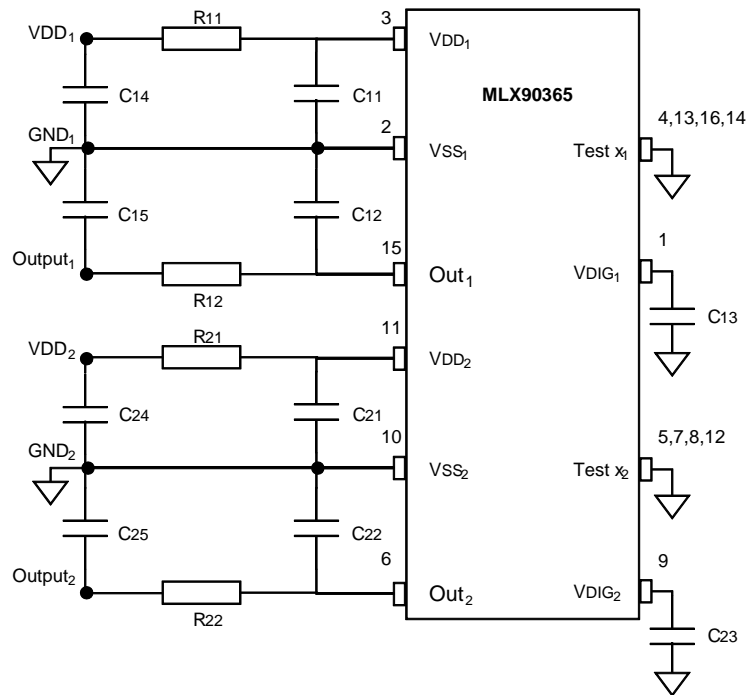


Figure 9 – Recommended wiring for the MLX90365 in SOIC-8 package

Output	Compact PCB routing			EMC robust PCB routing			
Analog Output	Min	Typ.	Max	Min	Typ.	Max	Remarks
C11, C21	100 nF	100 nF	1 uF	47 nF	100 nF	1 uF	Close to the pin
C12, C22	47 nF	100 nF	330 nF	47 nF	100 nF	330 nF	Close to the pin
C13, C23	47 nF	100 nF	220 nF	47 nF	100 nF	220 nF	Close to the pin
C14, C24	-	-	-	500 pF	1 nF	10 nF	Connector Side
C15, C25	-	-	-	500 pF	1 nF	10 nF	Connector Side
R11, R21	-	-	-	0 Ω	10 Ω	33 Ω	Increased ratiometry error
R12, R22	-	-	-	10 Ω	50 Ω	100 Ω	

Output	Compact PCB routing			EMC robust PCB routing			
PWM Output	Min	Typ.	Max	Min	Typ.	Max	Remarks
C11, C21	100 nF	100 nF	1 uF	47 nF	100 nF	1 uF	Close to the pin
C12, C22	22 nF	4.7 nF	22 nF	2.2 nF	4.7 nF	22 nF	Close to the pin
C13, C23	47 nF	100 nF	220 nF	47 nF	100 nF	220 nF	Close to the pin
C14, C24	-	-	-	500 pF	1 nF	10 nF	Connector Side
C15, C25	-	-	-	500 pF	1 nF	2.2 nF	Connector Side
R11, R21	-	-	-	0 Ω	10 Ω	33 Ω	Impacts the Voltage on VDD pin
R12, R22	-	-	-	10 Ω	50 Ω	100 Ω	

## 17. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to standards in place in Semiconductor industry.

For further details about test method references and for compliance verification of selected soldering method for product integration, Melexis recommends reviewing on our web site the General Guidelines soldering recommendation (<http://www.melexis.com/en/quality-environment/soldering>).

For all soldering technologies deviating from the one mentioned in above document (regarding peak temperature, temperature gradient, temperature profile etc), additional classification and qualification tests have to be agreed upon with Melexis.

For package technology embedding trim and form post-delivery capability, Melexis recommends consulting the dedicated trim&forming recommendation application note: lead trimming and forming recommendations (<http://www.melexis.com/en/documents/documentation/application-notes/lead-trimming-and-forming-recommendations>).

Melexis is contributing to global environmental conservation by promoting lead free solutions. For more information on qualifications of RoHS compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: <http://www.melexis.com/en/quality-environment>.

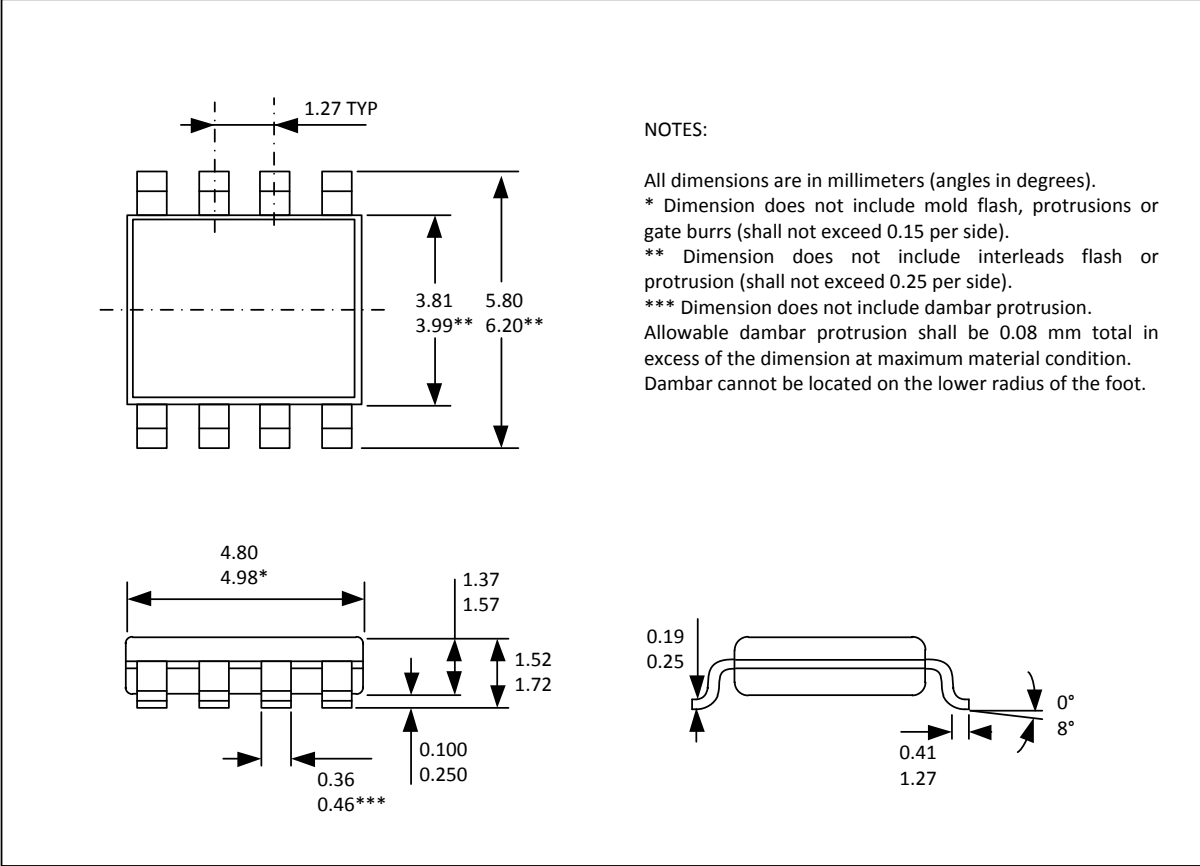
## 18. ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).

Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

# 19. Package Information

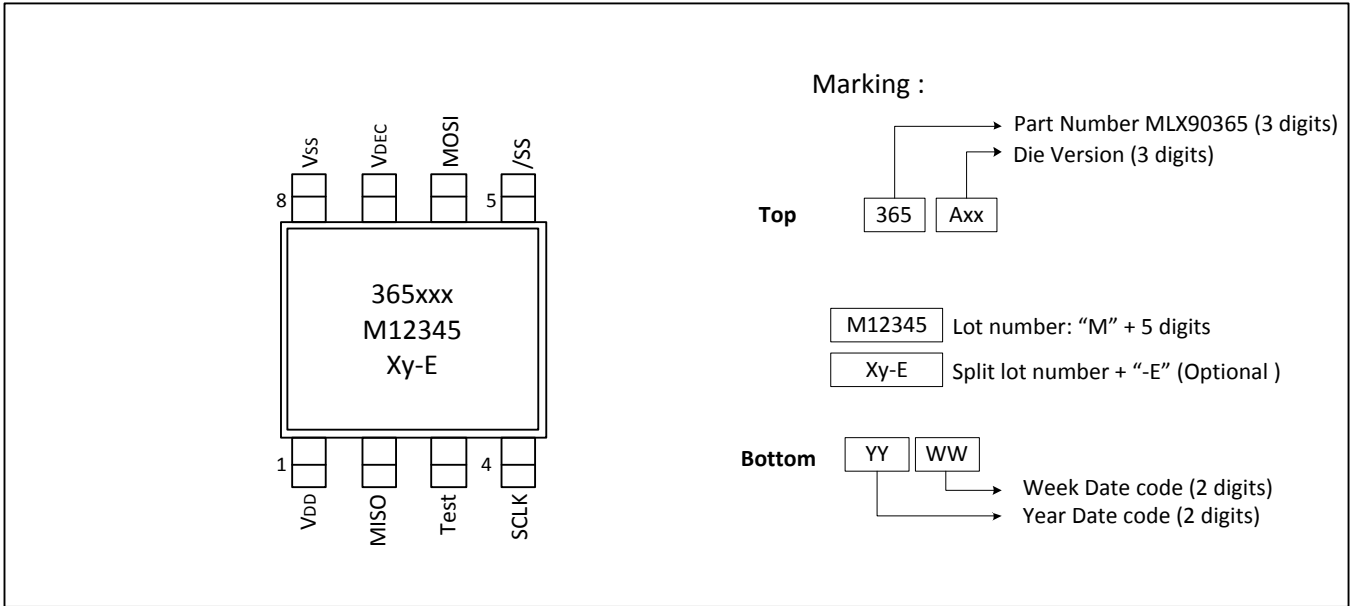
## 19.1. SOIC-8 - Package Dimensions



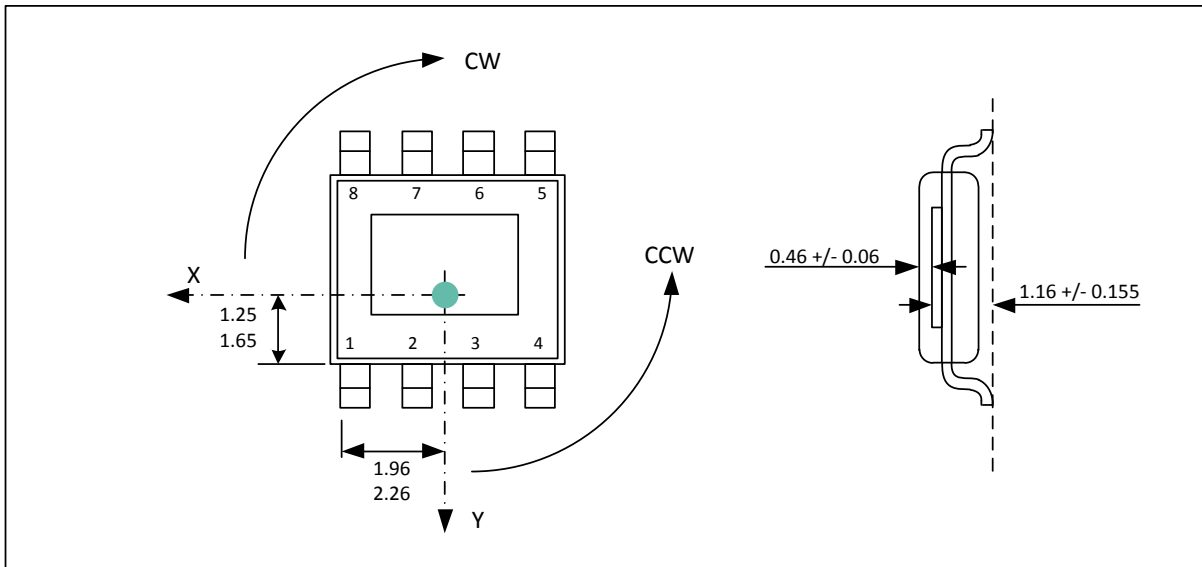
**NOTES:**

All dimensions are in millimeters (angles in degrees).  
 \* Dimension does not include mold flash, protrusions or gate burrs (shall not exceed 0.15 per side).  
 \*\* Dimension does not include interleads flash or protrusion (shall not exceed 0.25 per side).  
 \*\*\* Dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.

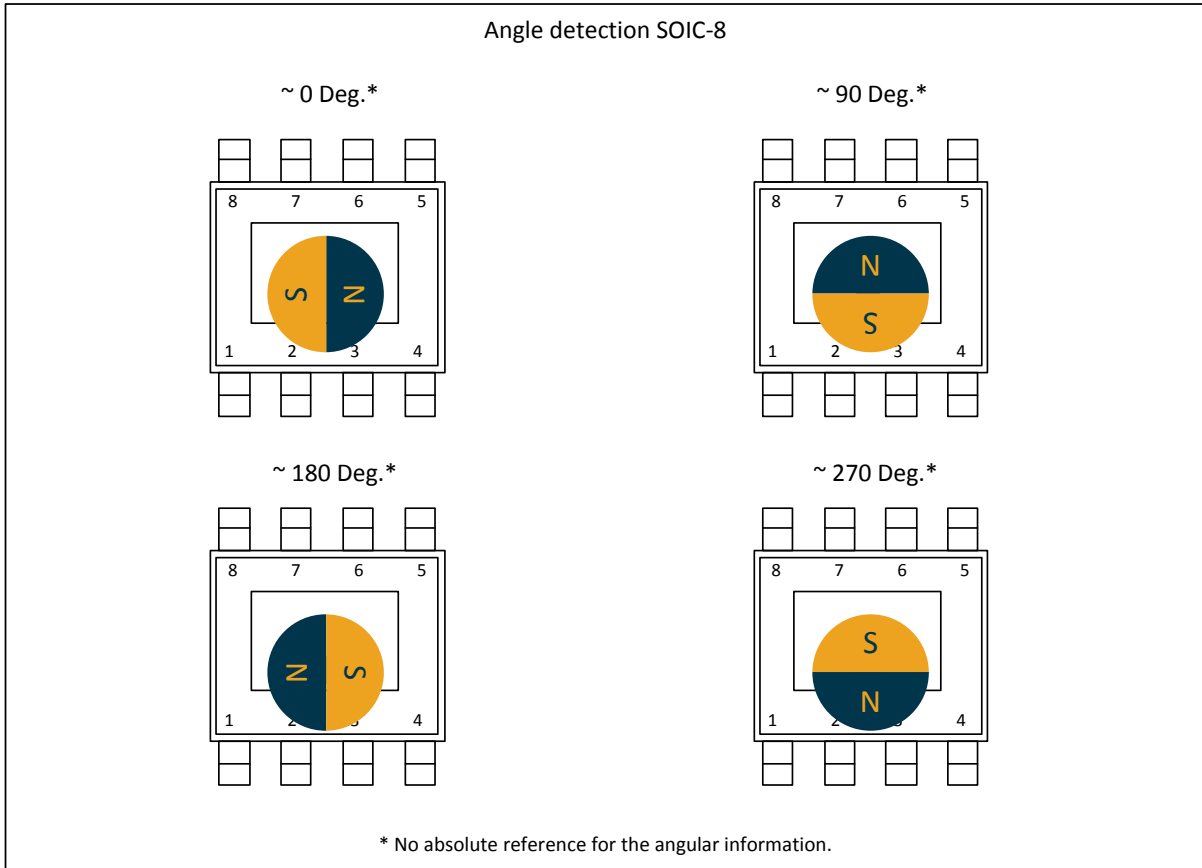
### 19.2. SOIC-8 - Pinout and Marking



### 19.3. SOIC-8 - Sensitive spot positioning

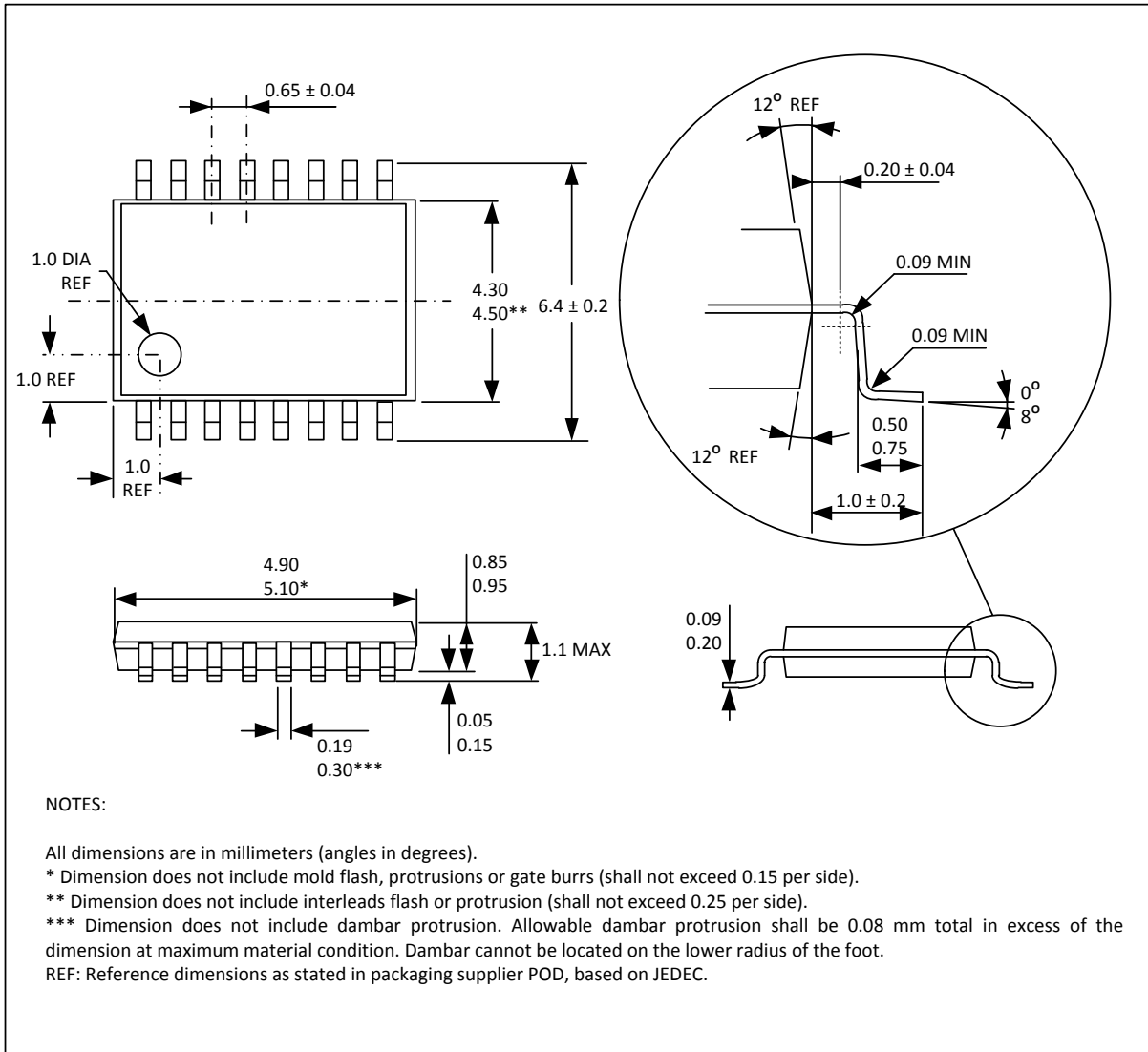




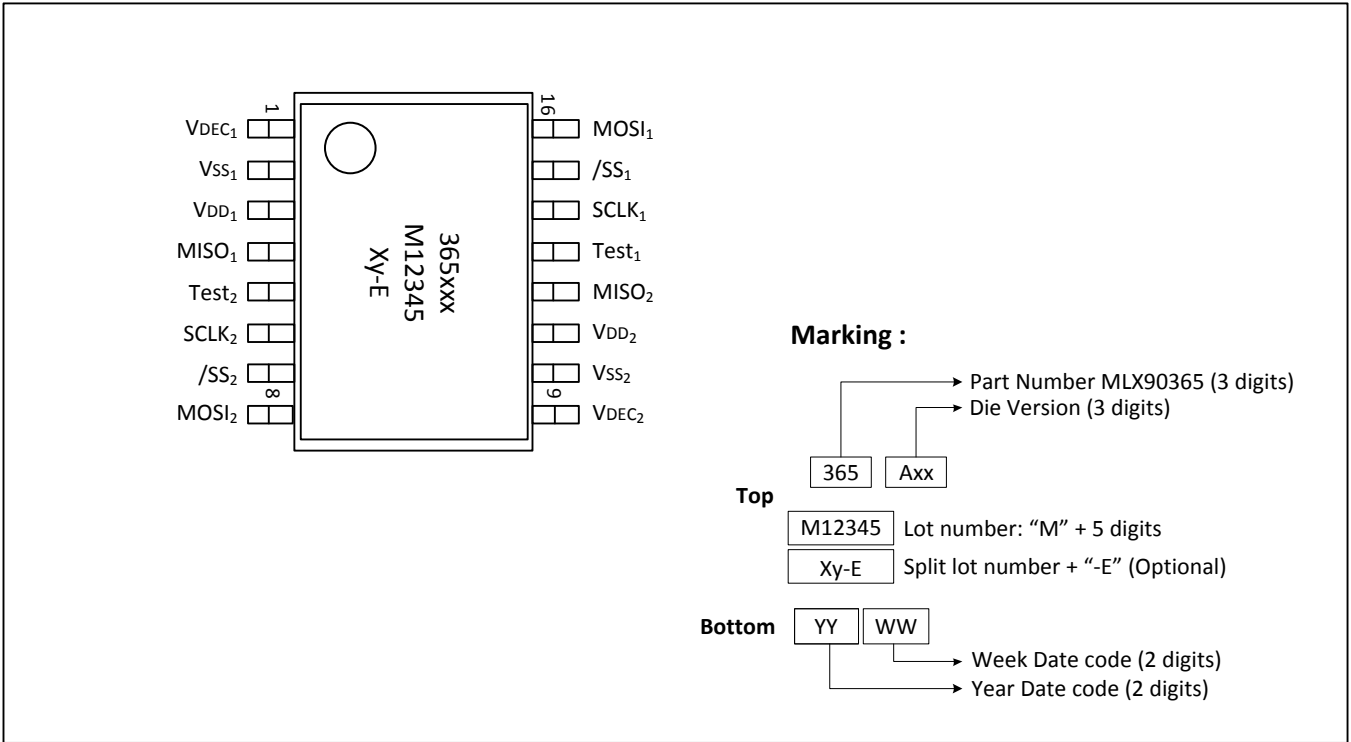


The MLX90365 is an absolute angular position sensor but the linearity error (Le – See section 9.1) does not include the error linked to the absolute reference 0 Deg.

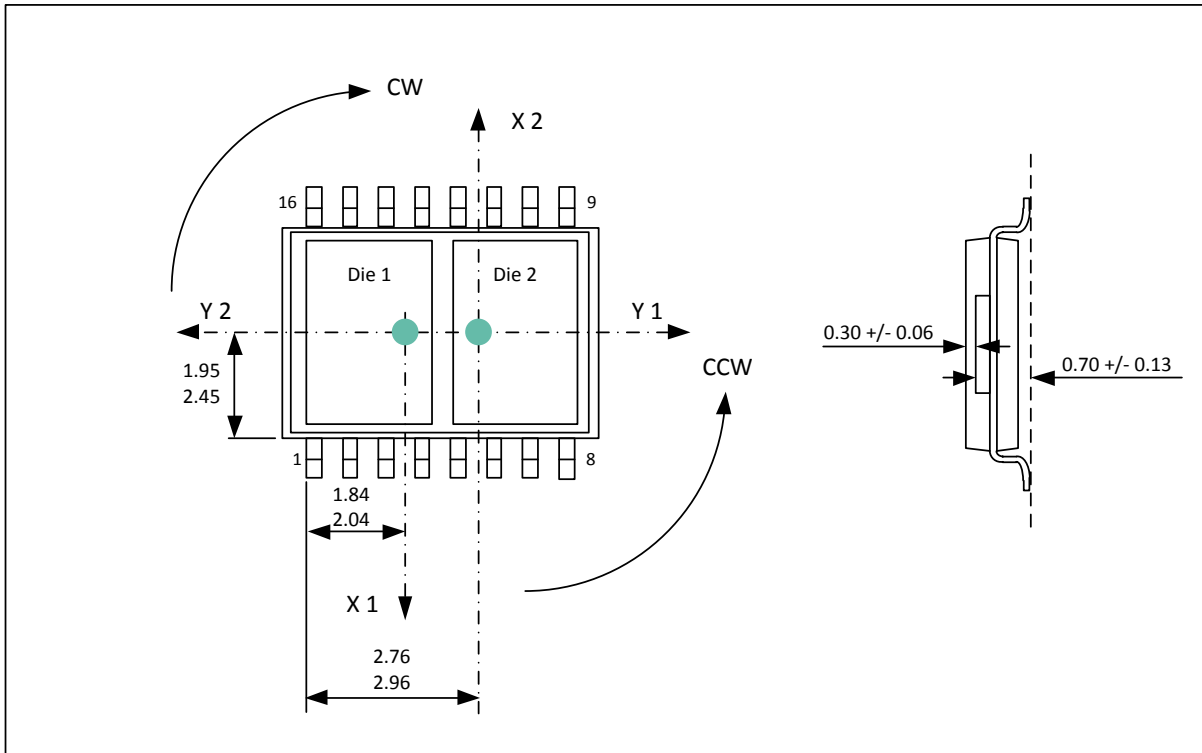
## 19.4. TSSOP-16 - Package Dimensions

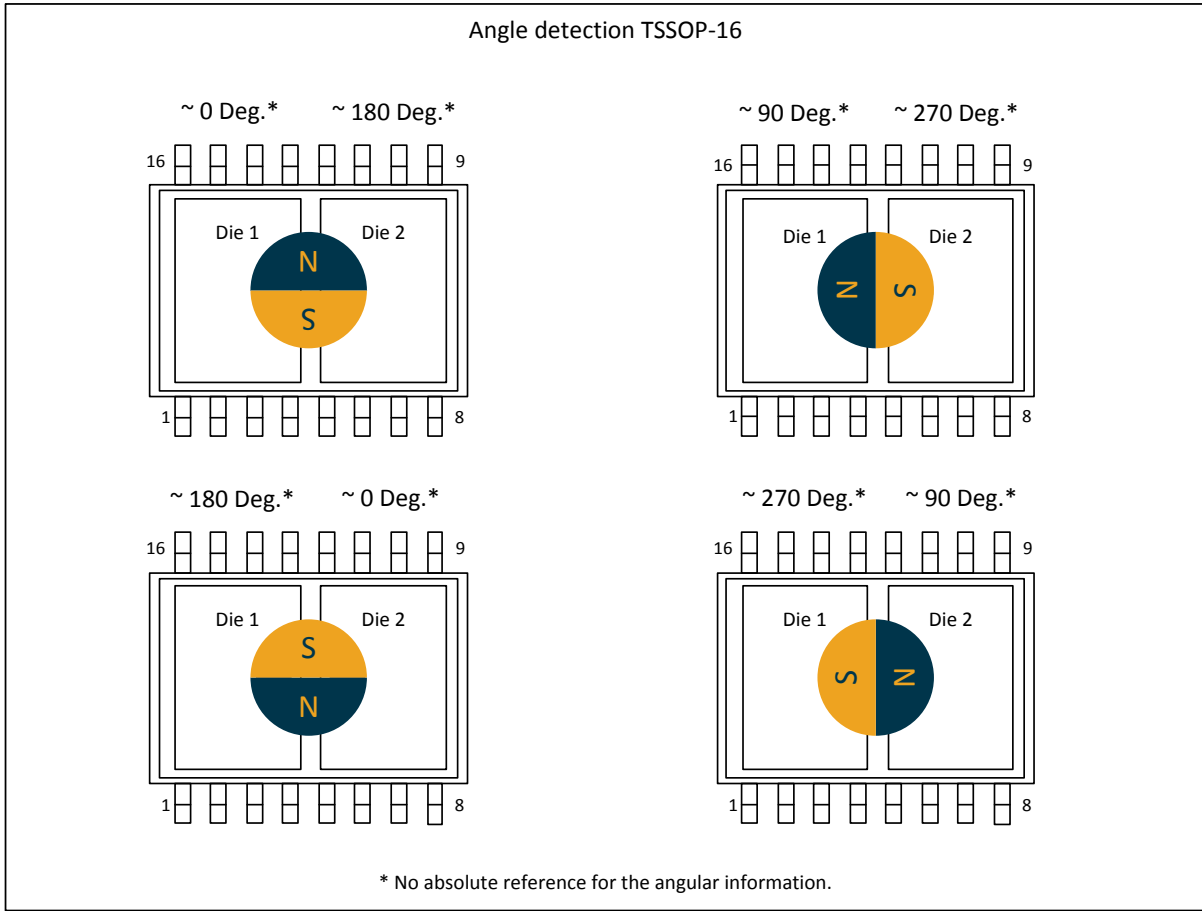


### 19.5. TSSOP-16 - Pinout and Marking



### 19.6. TSSOP-16 - Sensitive spot positioning





The MLX90365 is an absolute angular position sensor but the linearity error (Le – See section 9.1) does not include the error linked to the absolute reference 0 Deg.

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Revision Number	Date	Name	Comment
AA		vsa	Initial release
AB	04/08/11		Timing specification updated, STD EEP map defined
BA	15/02/12	vsa	Revision
01	25/05/12	klw	First release
02	01/07/12	vhi	Released datasheet for launch  Official template Benefit & Features Ordering Information Block Diagram Section 14.4.2 – Introduction of SEL_k Section 16 – New application diagrams
03	04/09/13	vsa	Correction of old errors like fig. 8 In section 1 ( Diagram ), regulator voltage corrected to 2.5V In section 5, max ratings: precise time specification In section 14.1.2 Polarity is inverted In section 15 ( Diag. Table ) Broken VDD/VSS output level corrected Implementation of new ordering codes for MFI and ABD version ( memlock version ) Embedding of the PWM specification
04	02/04/13	vsa	Correction of Rising Time in mode 5, on page 33 tssop 16 pinout and marking the marking letters are at the wrong angle.
5.0	12/03/15	sri	Added Voh_min for Rpu to supply > 5V Added PWM open drain Vo_min specification Adapted refresh-rate to +/-5% variation to match oscillator specification
5.1	9.04.2015	Sri	Vsat_hi 5kPD changed min/typ limit from 94/96% to 95/97% Vsat_hi 10kPD changed min/typ limit from 96/98% to 97.5/98.5% BVSSPD added line with 5k PD Dsat_hi 5kPD changed min/typ limit from 94/96% to 95/97% Dsat_hi 10kPD changed min/typ limit from 96/98% to 97.5/98.5% Added footnote in application recommendation.
5.2	22.05.2015	Sri	Added start-up time for PWM mode Added note in chap. 17.5.7 for diagnostic modes Step response times minimum removed, typical adjusted Thermal Offset Drift added for different temperature suffix Self-diagnostics table re-written for clarity Added recommendation in 14.7.5 for safety critical applications Passive Diagnostic Output Level, added footnote for dual-die influence in Broken Vss case Delivery form changed from tube to sample pack
5.3	09.07.2015	Sri	Footnote references updated
5.4	15.07.2015	Sri	Footnote 5: MLX90365_Broken_Vss_Dualdie
5.5	28.07.2015	Sri	Formatting change
5.6	27.10.2015	Sri/jed/CET	Added footnote for condition on 10mA max consumption. 12mA without current toggling. Added typical value for Idd in output mode 1 Addition of maximum values of startup cycle Docserver revision 6
5.7	22.01.2016	cet	Revision 5.7 incremented and document number inserted Docserver number inserted in revision 007
5.8	1.11.2016	cet/ela	Migration to the new template docserver revision 008 “Digital Saturation Level” Rpullup criteria corrected: must be higher than the minimum value Modification of the section Self Diagnostic addition of a condition “temperature monitor can be enabled only if the supply slew rate is higher than 0.5V/ms for slower rise time, please contact Melexis” / To be done: addition of ABE version / Formatting modification / Addition of ABE / Version: code version / parameters added in Section 13 Change of the recommendation of the capacitances Details given on the Safety timing DTI