



# Intel® Stratix® 10 Device Datasheet



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## Intel® Stratix® 10 Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and timing for Intel® Stratix® 10 devices.

**Table 1. Intel Stratix 10 Device Grades and Speed Grades Supported**

Device Grade	Speed Grade Supported
Extended	<ul style="list-style-type: none"> <li>• -E1V (fastest)</li> <li>• -E2V</li> <li>• -E2L</li> <li>• -E3V</li> <li>• -E3X</li> </ul>
Industrial	<ul style="list-style-type: none"> <li>• -I1V</li> <li>• -I2V</li> <li>• -I2L</li> <li>• -I3V</li> <li>• -I3X</li> </ul>

The suffix after the speed grade denotes the power options offered in Intel Stratix 10 devices.

- V—SmartVID with standard static power
- L—0.85 V fixed voltage with low static power
- X—0.80 V fixed voltage with lowest static power

## Electrical Characteristics

The following sections describe the operating conditions and power consumption of Intel Stratix 10 devices.

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## Operating Conditions

Intel Stratix 10 devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Intel Stratix 10 devices, you must consider the operating requirements described in this section.

The Maximum Allowed Overshoot During Transitions specifications will be available in a future release of the *Intel Stratix 10 Device Datasheet*.

## Absolute Maximum Ratings

This section defines the maximum operating conditions for Intel Stratix 10 devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

**Caution:** Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

**Table 2. Absolute Maximum Ratings for Intel Stratix 10 Devices—Preliminary**

Symbol	Description	Condition	Minimum	Maximum	Unit
V <sub>CC</sub>	Core voltage power supply	—	-0.50	1.26	V
V <sub>CCP</sub>	Periphery circuitry and transceiver fabric interface power supply	—	-0.50	1.26	V
V <sub>CCERAM</sub>	Embedded memory and digital transceiver power supply	—	-0.50	1.24	V
V <sub>CCPT</sub>	Power supply for programmable power technology and I/O pre-driver	—	-0.50	2.46	V
V <sub>CCBAT</sub>	Battery back-up power supply for design security volatile key register	—	-0.50	2.46	V
V <sub>CCIO_SDM</sub>	Configuration pins power supply	—	-0.50	2.46	V
V <sub>CCIO</sub>	I/O buffers power supply	3 V I/O	-0.50	4.10	V
		LVDS I/O <sup>(1)</sup>	-0.50	2.46	V
V <sub>CCA_PLL</sub>	Phase-locked loop (PLL) analog power supply	—	-0.50	2.46	V
V <sub>CCT_GXB</sub>	Transmitter analog power supply	—	-0.50	1.47	V

*continued...*

(1) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.



Symbol	Description	Condition	Minimum	Maximum	Unit
V <sub>CCR_GXB</sub>	Receiver analog power supply	—	-0.50	1.47	V
V <sub>CCH_GXB</sub>	Transmitter output buffer power supply	—	-0.50	2.46	V
V <sub>CCL_HPS</sub>	HPS core voltage and periphery circuitry power supply	—	-0.50	1.30	V
V <sub>CCIO_HPS</sub>	HPS I/O buffers power supply	LVDS I/O <sup>(1)</sup>	-0.50	2.46	V
V <sub>CCPLL_HPS</sub>	HPS PLL power supply	—	-0.50	2.46	V
V <sub>I</sub>	DC input voltage	3 V I/O	-0.30	3.80	V
		LVDS I/O	-0.30	2.50	V
I <sub>OUT</sub>	DC output current per pin	—	-25	40	mA
T <sub>J</sub>	Operating junction temperature	—	-55	125	°C
T <sub>STG</sub>	Storage temperature (no bias)	—	-55	150	°C

### Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 2.70 V for LVDS I/O can only be at 2.70 V for ~4% over the lifetime of the device.

**Table 3. Maximum Allowed Overshoot During Transitions for Intel Stratix 10 Devices (for LVDS I/O)—Preliminary**

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The LVDS I/O values are applicable to the V<sub>REFP\_ADC</sub> and V<sub>REFN\_ADC</sub> I/O pins.

Symbol	Description	LVDS I/O (V) <sup>(2)</sup>	Overshoot Duration as % at T <sub>J</sub> = 100°C	Unit
V <sub>i</sub> (AC)	AC input voltage	2.19	100	%
		2.24	60	%
				<i>continued...</i>

<sup>(2)</sup> The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.



Symbol	Description	LVDS I/O (V) <sup>(2)</sup>	Overshoot Duration as % at T <sub>j</sub> = 100°C	Unit
		2.29	30	%
		2.34	20	%
		2.39	10	%
		2.44	6	%
		> 2.44	No overshoot allowed	%

**Table 4. Maximum Allowed Overshoot During Transitions for Intel Stratix 10 Devices (for 3 V I/O)—Preliminary**

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

Symbol	Description	3 V I/O (V)	Overshoot Duration as % at T <sub>j</sub> = 100°C	Unit
V <sub>i</sub> (AC)	AC input voltage	3.80	100	%
		3.85	42	%
		3.90	18	%
		3.95	9	%
		4.00	4	%
		> 4.00	No overshoot allowed	%

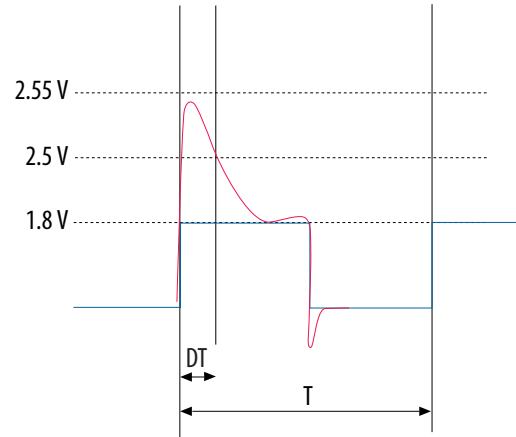
For an overshoot of 2.5 V, the percentage of high time for the overshoot can be as high as 100% over a 10-year period. Percentage of high time is calculated as  $([\Delta T]/T) \times 100$ . This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal.

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(2) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.



Figure 1. Intel Stratix 10 Devices Overshoot Duration



### Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Intel Stratix 10 devices.



## Recommended Operating Conditions

**Table 5. Recommended Operating Conditions for Intel Stratix 10 Devices—Preliminary**

This table lists the steady-state voltage values expected for Intel Stratix 10 devices. Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum <sup>(3)</sup>	Typical	Maximum <sup>(3)</sup>	Unit
V <sub>CC</sub>	Core voltage power supply	-E1V, -I1V, -E2V, -I2V, -E3V, -I3V <sup>(4)</sup>	0.77 – 0.91	0.8 – 0.94	0.83 – 0.97	V
		-E2L, -I2L	0.82	0.85	0.88	V
		-E3X, -I3X	0.77	0.8	0.83	V
V <sub>CCP</sub>	Periphery circuitry and transceiver fabric interface power supply	-E1V, -I1V, -E2V, -I2V, -E3V, -I3V <sup>(4)</sup>	0.77 – 0.91	0.8 – 0.94	0.83 – 0.97	V
		-E2L, -I2L	0.82	0.85	0.88	V
		-E3X, -I3X	0.77	0.8	0.83	V
V <sub>CCIO_SDM</sub>	Configuration pins power supply	1.8 V	1.71	1.8	1.89	V
V <sub>CCPLLDIG_SDM</sub>	Secure Device Manager (SDM) block PLL digital power supply	—	0.87	0.9	0.93	V
V <sub>CCPLL_SDM</sub>	SDM block PLL analog power supply	—	1.71	1.8	1.89	V
V <sub>CCFUSEWR_SDM</sub>	Fuse block writing power supply	—	2.35	2.4	2.45	V
V <sub>CCADC</sub>	ADC voltage sensor power supply	—	1.71	1.8	1.89	V
V <sub>CCERAM</sub>	Embedded memory and digital transceiver power supply	0.9 V	0.87	0.9	0.93	V
V <sub>CCBAT</sub> <sup>(5)</sup>	Battery back-up power supply (For design security volatile key register)	—	1.14	—	1.89	V

*continued...*

<sup>(3)</sup> This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise. Refer to power distribution network (PDN) tool for PCB power distribution network design.

<sup>(4)</sup> SmartVID graded devices require the use of a configurable voltage regulator or system controller to receive the device's settings through the Power Management Bus (PMBus™) or Pulse-Width Modulation (PWM) interface for proper performance.





Symbol	Description	Condition	Minimum <sup>(3)</sup>	Typical	Maximum <sup>(3)</sup>	Unit
V <sub>CCPT</sub>	Power supply for programmable power technology and I/O pre-driver	1.8 V	1.71	1.8	1.89	V
V <sub>CCIO</sub>	I/O buffers power supply	3.0 V (for 3 V I/O only)	2.85	3	3.15	V
		2.5 V (for 3 V I/O only)	2.375	2.5	2.625	V
		1.8 V	1.7	1.8	1.9	V
		1.5 V	1.4	1.5	1.6	V
		1.2 V	1.14	1.2	1.26	V
V <sub>CCIO_UIB</sub>	Power supply for the Universal Interface Bus between the core and embedded HBM2 memory	1.2 V	1.17	1.2	1.23	V
V <sub>CCM_WORD</sub>	Power supply for the embedded HBM2 memory	—	2.375	2.5	2.625	V
V <sub>CCA_PLL</sub>	PLL analog voltage regulator power supply	—	1.71	1.8	1.89	V
V <sub>REFP_ADC</sub>	Precision voltage reference for voltage sensor	—	1.2475	1.25	1.2525	V
V <sub>I</sub> <sup>(6)</sup>	DC input voltage	3 V I/O	-0.3	—	3.6	V
		LVDS I/O	-0.3	—	2.46	V
V <sub>O</sub>	Output voltage	—	0	—	V <sub>CCIO</sub>	V
T <sub>J</sub>	Operating junction temperature	Extended	0	—	100	°C
		Industrial	-40	—	100	°C
t <sub>RAMP</sub> <sup>(7)(8)(9)(10)</sup>	Power supply ramp time	Standard POR	200 μs	—	100 ms	—

- <sup>(3)</sup> This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise. Refer to power distribution network (PDN) tool for PCB power distribution network design.
- <sup>(5)</sup> If you do not use the design security feature in Intel Stratix 10 devices, connect V<sub>CCBAT</sub> to a 1.8 V power supply. Intel Stratix 10 power-on reset (POR) circuitry monitors V<sub>CCBAT</sub>.
- <sup>(6)</sup> The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.



## Transceiver Power Supply Operating Conditions

**Table 6. Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L-Tile Devices in a Non-Bonded Configuration**

Symbol	Description	Datarate	Minimum	Typical	Maximum	Unit
V <sub>CCT_GXB[L,R]</sub> and V <sub>CCR_GXB[L,R]</sub>	Chip-to-chip <sup>(11)</sup>	1.0 Gbps to 26.6 Gbps <sup>(12)</sup> <sup>(13)</sup>	1.1	1.12	1.14	V
		1.0 Gbps to 17.4 Gbps <sup>(12)</sup> <sup>(13)</sup>	1.0	1.03	1.14	V
	Backplane as per IEEE802.3BJ <sup>(14)</sup>	1.0 Gbps to 12.5 Gbps <sup>(12)</sup>	1.0	1.03 <sup>(15)</sup>	1.14	V
V <sub>CCH_GXB[L,R]</sub>	Transceiver high voltage power	—	1.710	1.8	1.890	V

- (7) This is also applicable to HPS power supply. For HPS power supply, refer to  $t_{RAMP}$  specifications for standard POR when HPS\_PORSEL = 0 and  $t_{RAMP}$  specifications for fast POR when HPS\_PORSEL = 1.
- (8)  $t_{RAMP}$  is the ramp time of each individual power supply, not the ramp time of all combined power supplies.
- (9) To support AS fast mode, all power supplies to the Intel Stratix 10 device must be fully ramped-up within 10 ms to the recommended operating conditions.
- (10) To support AS normal mode, V<sub>CCIO\_SDM</sub> of the Intel Stratix 10 device must be fully ramped-up within 10 ms to the recommended operating condition.
- (11) Chip-to-chip refers to transceiver links that are short reach and do not require advanced equalization such as decision feedback equalization (DFE).
- (12) Stratix 10 transceivers can support data rates below 1.0 Gbps through over sampling.
- (13) Bonded channels operating at datarates above 16.0 Gbps require 1.12 V ±20 mV at the pin. For channels that are placed on the same tile as the channels that require 1.12 V ±20 mV, V<sub>CCR\_GXB</sub> and V<sub>CCT\_GXB</sub> = 1.12 V ±20 mV.
- (14) Backplane applications refer to ones which require advanced equalization, such as DFE enabled, to compensate for channel loss.



**Table 7. Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L-Tile Devices in a Bonded Configuration**

Symbol	Description	Datarate	Minimum	Typical	Maximum	Unit
V <sub>CCCT_GXB[L,R]</sub> and V <sub>CCCR_GXB[L,R]</sub>	Chip-to-chip <sup>(11)</sup>	1.0 Gbps to 16.0 Gbps <sup>(12)</sup>	1.0	1.03	1.14	V
		> 16.0 Gbps to 17.4 Gbps <sup>(12) (13)</sup>	1.1	1.12	1.14	V
	Backplane <sup>(14)</sup>	1.0 Gbps to 12.5 Gbps <sup>(12)</sup>	1.0	1.03 <sup>(15)</sup>	1.14	V
V <sub>CCH_GXB[L,R]</sub>	Transceiver high voltage power	—	1.710	1.8	1.890	V

**Table 8. Transceiver Power Supply Operating Conditions for Intel Stratix 10 H-Tile Devices in a Non-Bonded Configuration**

Symbol	Description	Datarate	Minimum	Typical	Maximum	Unit
V <sub>CCCT_GXB[L,R]</sub> and V <sub>CCCR_GXB[L,R]</sub>	Chip-to-chip <sup>(11)</sup> and Backplane <sup>(14)</sup>	1.0 Gbps to 28.3 Gbps (GXT) <sup>(12)</sup>	1.1	1.12	1.14	V
		1.0 Gbps to 17.4 Gbps (GX) <sup>(12)</sup>	1.0	1.03	1.14	V
V <sub>CCH_GXB[L,R]</sub>	Transceiver high voltage power	—	1.710	1.8	1.890	V

**Table 9. Transceiver Power Supply Operating Conditions for Intel Stratix 10 H-Tile Devices in a Bonded Configuration**

Symbol	Description	Datarate	Minimum	Typical	Maximum	Unit
V <sub>CCCT_GXB[L,R]</sub> and V <sub>CCCR_GXB[L,R]</sub>	Chip-to-chip <sup>(11)</sup> and Backplane <sup>(14)</sup>	1.0 Gbps to 16.0 Gbps <sup>(12)</sup>	1.0	1.03	1.14	V
		> 16.0 Gbps to 17.4 Gbps <sup>(12)</sup>	1.1	1.12	1.14	V
		> 17.4 Gbps to 28.3 Gbps <sup>(12)</sup>	N/A	Not supported	N/A	V
V <sub>CCH_GXB[L,R]</sub>	Transceiver high voltage power	—	1.710	1.8	1.890	V

(15) Refer to the Intel Quartus® Prime Pro Edition software for the typical nominal value.



**Table 10. Transceiver Power Supply Operating Conditions for Intel Stratix 10 TX/MX E-Tile Devices—Preliminary**

Symbol	Description	Minimum <sup>(16)</sup>	Typical	Maximum <sup>(16)</sup>	Unit
V <sub>CCERT</sub>	Transceiver power supply	0.87	0.9	0.93	V
V <sub>CCERT_PLL</sub>	Transceiver PLL power supply	0.87	0.9	0.93	V
V <sub>CCEHT</sub>	Analog power supply <sup>(16)</sup>	1.067	1.1	1.133	V
V <sub>CCL</sub>	Periphery circuitry power supply	0.725	0.75	0.775	V
V <sub>CCN2P5V_IO</sub>	LVPECL REFCLK power supply	2.375	2.5	2.625	V
V <sub>CCR</sub>	Transceiver high voltage power supply	1.71	1.8	1.89	V

**Note:** Most V<sub>CCR\_GXB</sub> and V<sub>CCERT\_GXB</sub> pins associated with unused transceiver channels can be grounded on a per-tile basis to minimize power consumption. Refer to the *Intel Stratix 10 GX, MX, and SX Device Family Pin Connection Guidelines* and the Intel Quartus Prime pin report for information about pinning out the package to minimize power consumption for your specific design.

#### Related Links

[Intel Stratix 10 GX, MX, and SX Device Family Pin Connection Guidelines](#)

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<sup>(16)</sup> This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.



## HPS Power Supply Operating Conditions

**Table 11. HPS Power Supply Operating Conditions for Intel Stratix 10 Devices—Preliminary**

This table lists the steady-state voltage and current values expected for Intel Stratix 10 system-on-a-chip (SoC) devices with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to Recommended Operating Conditions for Intel Stratix 10 Devices table for the steady-state voltage values expected from the FPGA portion of the Intel Stratix 10 SoC devices.

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V <sub>CCL_HPS</sub>	HPS core voltage and periphery circuitry power supply	-E2L, -I2L, -E3X, -I3X	0.91	0.94	0.97	V
		-E1V, -I1V, -E2V, -I2V, -E3V, -I3V <sup>(17)</sup>	0.77 - 0.91	0.8 - 0.94	0.83 - 0.97	V
V <sub>CCPLLDIG_HPS</sub>	HPS PLL digital power supply	-E2L, -I2L, -E3X, -I3X	0.91	0.94	0.97	V
		-E1V, -I1V, -E2V, -I2V, -E3V, -I3V <sup>(17)</sup>	0.77 - 0.91	0.8 - 0.94	0.83 - 0.97	V
V <sub>CCPLL_HPS</sub>	HPS PLL analog power supply	1.8 V	1.71	1.8	1.89	V
V <sub>CCIO_HPS</sub>	HPS I/O buffers power supply	1.8 V	1.71	1.8	1.89	V

### Related Links

- [Recommended Operating Conditions](#) on page 8  
Provides the steady-state voltage values for the FPGA portion of the device.
- [HPS Clock Performance - Preliminary](#) on page 56

## DC Characteristics

The pin capacitance specifications will be available in a future release of the *Intel Stratix 10 Device Datasheet*.

## Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Intel Quartus Prime Power Analyzer feature.

<sup>(17)</sup> SmartVID graded devices require the use of a configurable voltage regulator or system controller to receive the device's settings through PMBUS or PWM for proper performance.



Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the usage of the resources.

The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yield very accurate power estimates.

### I/O Pin Leakage Current

**Table 12. I/O Pin Leakage Current for Intel Stratix 10 Devices—Preliminary**

Symbol	Description	Condition	Min	Max	Unit
$I_I$	Input pin	$V_I = 0\text{ V to }V_{CCIO\text{MAX}}$	-80	80	$\mu\text{A}$
$I_{OZ}$	Tri-stated I/O pin	$V_O = 0\text{ V to }V_{CCIO\text{MAX}}$	-80	80	$\mu\text{A}$

### Bus Hold Specifications

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

**Table 13. Bus Hold Parameters for Intel Stratix 10 Devices—Preliminary**

Parameter	Symbol	Condition	$V_{CCIO}$ (V)										Unit
			1.2		1.5		1.8		2.5		3.0		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	$I_{SUSL}$	$V_{IN} > V_{IL}$ (max)	8	—	12	—	30	—	60	—	70	—	$\mu\text{A}$
Bus-hold, high, sustaining current	$I_{SUSH}$	$V_{IN} < V_{IH}$ (min)	-8	—	-12	—	-30	—	-60	—	-70	—	$\mu\text{A}$
Bus-hold, low, overdrive current	$I_{ODL}$	$0\text{ V} < V_{IN} < V_{CCIO}$	—	125	—	175	—	200	—	300	—	500	$\mu\text{A}$
Bus-hold, high, overdrive current	$I_{ODH}$	$0\text{ V} < V_{IN} < V_{CCIO}$	—	-125	—	-175	—	-200	—	-300	—	-500	$\mu\text{A}$
Bus-hold trip point	$V_{TRIP}$	—	0.3	0.9	0.38	1.13	0.68	1.07	0.7	1.7	0.8	2	V



### OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

**Table 14. OCT Calibration Accuracy Specifications for Intel Stratix 10 Devices—Preliminary**

Calibration accuracy for the calibrated on-chip series termination ( $R_S$  OCT) and on-chip parallel termination ( $R_T$  OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			-E1, -I1	-E2, -I2	-E3, -I3	
34- $\Omega$ , 48- $\Omega$ , 60- $\Omega$ , 80- $\Omega$ , 120- $\Omega$ , and 240- $\Omega$ $R_S$	Internal series termination with calibration (34- $\Omega$ , 48- $\Omega$ , 60- $\Omega$ , 80- $\Omega$ , 120- $\Omega$ , and 240- $\Omega$ setting)	$V_{CCIO} = 1.2$	$\pm 15$	$\pm 15$	$\pm 15$	%
34- $\Omega$ and 40- $\Omega$ $R_S$	Internal series termination with calibration (34- $\Omega$ and 40- $\Omega$ setting)	$V_{CCIO} = 1.5, 1.35, 1.25, 1.2$	$\pm 15$	$\pm 15$	$\pm 15$	%
25- $\Omega$ and 50- $\Omega$ $R_S$	Internal series termination with calibration (25- $\Omega$ and 50- $\Omega$ setting)	$V_{CCIO} = 1.8, 1.5, 1.2$	$\pm 15$	$\pm 15$	$\pm 15$	%
34- $\Omega$ , 40- $\Omega$ , 48- $\Omega$ , 60- $\Omega$ , 80- $\Omega$ , 120- $\Omega$ , and 240- $\Omega$ $R_T$	Internal parallel termination with calibration (34- $\Omega$ , 40- $\Omega$ , 48- $\Omega$ , 60- $\Omega$ , 80- $\Omega$ , 120- $\Omega$ , and 240- $\Omega$ setting)	POD12 I/O standard, $V_{CCIO} = 1.2$	$\pm 15$	$\pm 15$	$\pm 15$	%
48- $\Omega$ , 50- $\Omega$ , 60- $\Omega$ , and 120- $\Omega$ $R_T$	Internal parallel termination with calibration (48- $\Omega$ , 50- $\Omega$ , 60- $\Omega$ , and 120- $\Omega$ setting)	$V_{CCIO} = 1.5, 1.2$	-10 to +60	-10 to +60	-10 to +60	%
48- $\Omega$ , 60- $\Omega$ , and 120- $\Omega$ $R_T$	Internal parallel termination with calibration (48- $\Omega$ , 60- $\Omega$ , and 120- $\Omega$ setting)	$V_{CCIO} = 1.25$	-10 to +70	-10 to +70	-10 to +70	%
48- $\Omega$ , 60- $\Omega$ , and 120- $\Omega$ $R_T$	Internal parallel termination with calibration (48- $\Omega$ , 60- $\Omega$ , and 120- $\Omega$ setting)	$V_{CCIO} = 1.35$	-10 to +65	-10 to +65	-10 to +65	%
50- $\Omega$ $R_T$	Internal parallel termination with calibration (50- $\Omega$ setting)	$V_{CCIO} = 1.8$	-10 to +50	-10 to +50	-10 to +50	%



## OCT Without Calibration Resistance Tolerance Specifications

**Table 15. OCT Without Calibration Resistance Tolerance Specifications for Intel Stratix 10 Devices—Preliminary**

This table lists the Intel Stratix 10 OCT without calibration resistance tolerance to PVT changes.

Symbol	Description	Condition (V)	Resistance Tolerance			Unit
			-E1, -I1	-E2, -I2	-E3, -I3	
25-Ω and 50-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω and 50-Ω setting)	V <sub>CCIO</sub> = 3.0, 2.5	-40 to +30	±40	±40	%
		V <sub>CCIO</sub> = 1.8, 1.5, 1.2	-50 to +75	-50 to +75	-50 to +75	%
100-Ω R <sub>D</sub>	Internal differential termination (100-Ω setting)	V <sub>CCIO</sub> = 1.8	±25	±35	±40	%

**Figure 2. Equation for OCT Variation Without Recalibration—Preliminary**

$$R_{OCT} = R_{SCAL} \left( 1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle \right)$$

The definitions for the equation are as follows:

- The R<sub>OCT</sub> value calculated shows the range of OCT resistance with the variation of temperature and V<sub>CCIO</sub>.
- R<sub>SCAL</sub> is the OCT resistance value at power-up.
- ΔT is the variation of temperature with respect to the temperature at power up.
- ΔV is the variation of voltage with respect to the V<sub>CCIO</sub> at power up.
- dR/dT is the percentage change of R<sub>SCAL</sub> with temperature.
- dR/dV is the percentage change of R<sub>SCAL</sub> with voltage.

## Internal Weak Pull-Up Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up. For SDM and HPS, the configuration I/O and peripheral I/O are supported with weak pull-up and weak pull-down options.





**Table 16. Internal Weak Pull-Up Resistor Values for Intel Stratix 10 Devices—Preliminary**

Symbol	Description	Condition (V)	Nominal Value	Unit
R <sub>PU</sub>	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V <sub>CCIO</sub> = 3.0 ±5%	25	kΩ
		V <sub>CCIO</sub> = 2.5 ±5%	25	kΩ
		V <sub>CCIO</sub> = 1.8 ±5%	25	kΩ
		V <sub>CCIO</sub> = 1.5 ±5%	25	kΩ
		V <sub>CCIO</sub> = 1.35 ±5%	25	kΩ
		V <sub>CCIO</sub> = 1.25 ±5%	25	kΩ
		V <sub>CCIO</sub> = 1.2 ±5%	25	kΩ

**Related Links**

[Intel Stratix 10 GX, MX, and SX Device Family Pin Connection Guidelines](#)

Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.

**I/O Standard Specifications**

Tables in this section list the input voltage (V<sub>IH</sub> and V<sub>IL</sub>), output voltage (V<sub>OH</sub> and V<sub>OL</sub>), and current drive characteristics (I<sub>OH</sub> and I<sub>OL</sub>) for various I/O standards supported by Intel Stratix 10 devices.

For minimum voltage values, use the minimum V<sub>CCIO</sub> values. For maximum voltage values, use the maximum V<sub>CCIO</sub> values.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

**Related Links**

[Recommended Operating Conditions](#) on page 8



## Single-Ended I/O Standards Specifications

**Table 17. Single-Ended I/O Standards Specifications for Intel Stratix 10 Devices—Preliminary**

I/O Standard	V <sub>CCIO</sub> (V)			V <sub>IL</sub> (V)		V <sub>IH</sub> (V)		V <sub>OL</sub> (V)	V <sub>OH</sub> (V)	I <sub>OL</sub> <sup>(18)</sup> (mA)	I <sub>OH</sub> <sup>(18)</sup> (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.0-V LVTTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
3.0-V LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.3	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 × V <sub>CCIO</sub>	0.65 × V <sub>CCIO</sub>	V <sub>CCIO</sub> + 0.3	0.45	V <sub>CCIO</sub> - 0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 × V <sub>CCIO</sub>	0.65 × V <sub>CCIO</sub>	V <sub>CCIO</sub> + 0.3	0.25 × V <sub>CCIO</sub>	0.75 × V <sub>CCIO</sub>	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 × V <sub>CCIO</sub>	0.65 × V <sub>CCIO</sub>	V <sub>CCIO</sub> + 0.3	0.25 × V <sub>CCIO</sub>	0.75 × V <sub>CCIO</sub>	2	-2
Schmitt Trigger Input	1.71	1.8	1.89	—	0.35 × V <sub>CCIO</sub>	0.65 × V <sub>CCIO</sub>	—	—	—	—	—

## Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

**Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel Stratix 10 Devices—Preliminary**

I/O Standard	V <sub>CCIO</sub> (V)			V <sub>REF</sub> (V)			V <sub>TT</sub> (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V <sub>REF</sub> - 0.04	V <sub>REF</sub>	V <sub>REF</sub> + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V <sub>CCIO</sub>	0.5 × V <sub>CCIO</sub>	0.51 × V <sub>CCIO</sub>	0.49 × V <sub>CCIO</sub>	0.5 × V <sub>CCIO</sub>	0.51 × V <sub>CCIO</sub>
SSTL-135	1.283	1.35	1.45	0.49 × V <sub>CCIO</sub>	0.5 × V <sub>CCIO</sub>	0.51 × V <sub>CCIO</sub>	0.49 × V <sub>CCIO</sub>	0.5 × V <sub>CCIO</sub>	0.51 × V <sub>CCIO</sub>
SSTL-125	1.19	1.25	1.31	0.49 × V <sub>CCIO</sub>	0.5 × V <sub>CCIO</sub>	0.51 × V <sub>CCIO</sub>	0.49 × V <sub>CCIO</sub>	0.5 × V <sub>CCIO</sub>	0.51 × V <sub>CCIO</sub>

**continued...**

<sup>(18)</sup> To meet the I<sub>OL</sub> and I<sub>OH</sub> specifications, you must set the current strength settings accordingly. For example, to meet the 1.8- V LVCMOS specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the I<sub>OL</sub> and I<sub>OH</sub> specifications in the datasheet.



I/O Standard	V <sub>CCIO</sub> (V)			V <sub>REF</sub> (V)			V <sub>TT</sub> (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-12	1.14	1.2	1.26	0.49 × V <sub>CCIO</sub>	0.5 × V <sub>CCIO</sub>	0.51 × V <sub>CCIO</sub>	0.49 × V <sub>CCIO</sub>	0.5 × V <sub>CCIO</sub>	0.51 × V <sub>CCIO</sub>
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V <sub>CCIO</sub> /2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V <sub>CCIO</sub> /2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 × V <sub>CCIO</sub>	0.5 × V <sub>CCIO</sub>	0.53 × V <sub>CCIO</sub>	—	V <sub>CCIO</sub> /2	—
HSUL-12	1.14	1.2	1.3	0.49 × V <sub>CCIO</sub>	0.5 × V <sub>CCIO</sub>	0.51 × V <sub>CCIO</sub>	—	—	—
POD12	1.16	1.2	1.24	—	Internally calibrated	—	—	V <sub>CCIO</sub>	—

### Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Intel Stratix 10 Devices—Preliminary**

I/O Standard	V <sub>IL(DC)</sub> (V)		V <sub>IH(DC)</sub> (V)		V <sub>IL(AC)</sub> (V)	V <sub>IH(AC)</sub> (V)	V <sub>OL</sub> (V)	V <sub>OH</sub> (V)	I <sub>OL</sub> <sup>(19)</sup> (mA)	I <sub>OH</sub> <sup>(19)</sup> (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-18 Class I	-0.3	V <sub>REF</sub> - 0.125	V <sub>REF</sub> + 0.125	V <sub>CCIO</sub> + 0.3	V <sub>REF</sub> - 0.25	V <sub>REF</sub> + 0.25	V <sub>TT</sub> - 0.603	V <sub>TT</sub> + 0.603	6.7	-6.7
SSTL-18 Class II	-0.3	V <sub>REF</sub> - 0.125	V <sub>REF</sub> + 0.125	V <sub>CCIO</sub> + 0.3	V <sub>REF</sub> - 0.25	V <sub>REF</sub> + 0.25	0.28	V <sub>CCIO</sub> - 0.28	13.4	-13.4
SSTL-15 Class I	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	V <sub>REF</sub> - 0.175	V <sub>REF</sub> + 0.175	0.2 × V <sub>CCIO</sub>	0.8 × V <sub>CCIO</sub>	8	-8
SSTL-15 Class II	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	V <sub>REF</sub> - 0.175	V <sub>REF</sub> + 0.175	0.2 × V <sub>CCIO</sub>	0.8 × V <sub>CCIO</sub>	16	-16
SSTL-135	—	V <sub>REF</sub> - 0.09	V <sub>REF</sub> + 0.09	—	V <sub>REF</sub> - 0.16	V <sub>REF</sub> + 0.16	0.2 × V <sub>CCIO</sub>	0.8 × V <sub>CCIO</sub>	—	—
SSTL-125	—	V <sub>REF</sub> - 0.09	V <sub>REF</sub> + 0.09	—	V <sub>REF</sub> - 0.15	V <sub>REF</sub> + 0.15	0.2 × V <sub>CCIO</sub>	0.8 × V <sub>CCIO</sub>	—	—

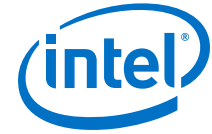
*continued...*

<sup>(19)</sup> To meet the I<sub>OL</sub> and I<sub>OH</sub> specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I<sub>OL</sub> and I<sub>OH</sub> specifications in the datasheet.



I/O Standard	V <sub>IL(DC)</sub> (V)		V <sub>IH(DC)</sub> (V)		V <sub>IL(AC)</sub> (V)	V <sub>IH(AC)</sub> (V)	V <sub>OL</sub> (V)	V <sub>OH</sub> (V)	I <sub>OL</sub> <sup>(19)</sup> (mA)	I <sub>OH</sub> <sup>(19)</sup> (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-12	—	V <sub>REF</sub> - 0.10	V <sub>REF</sub> + 0.10	—	V <sub>REF</sub> - 0.15	V <sub>REF</sub> + 0.15	0.2 × V <sub>CCIO</sub>	0.8 × V <sub>CCIO</sub>	—	—
HSTL-18 Class I	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCIO</sub> - 0.4	8	-8
HSTL-18 Class II	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCIO</sub> - 0.4	16	-16
HSTL-15 Class I	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCIO</sub> - 0.4	8	-8
HSTL-15 Class II	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCIO</sub> - 0.4	16	-16
HSTL-12 Class I	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	V <sub>REF</sub> - 0.15	V <sub>REF</sub> + 0.15	0.25 × V <sub>CCIO</sub>	0.75 × V <sub>CCIO</sub>	8	-8
HSTL-12 Class II	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	V <sub>REF</sub> - 0.15	V <sub>REF</sub> + 0.15	0.25 × V <sub>CCIO</sub>	0.75 × V <sub>CCIO</sub>	16	-16
HSUL-12	—	V <sub>REF</sub> - 0.13	V <sub>REF</sub> + 0.13	—	V <sub>REF</sub> - 0.22	V <sub>REF</sub> + 0.22	0.1 × V <sub>CCIO</sub>	0.9 × V <sub>CCIO</sub>	—	—
POD12	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	V <sub>REF</sub> - 0.15	V <sub>REF</sub> + 0.15	(0.7 - 0.15) × V <sub>CCIO</sub>	(0.7 + 0.15) × V <sub>CCIO</sub>	—	—

<sup>(19)</sup> To meet the I<sub>OL</sub> and I<sub>OH</sub> specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I<sub>OL</sub> and I<sub>OH</sub> specifications in the datasheet.



### Differential SSTL I/O Standards Specifications

**Table 20. Differential SSTL I/O Standards Specifications for Intel Stratix 10 Devices—Preliminary**

I/O Standard	V <sub>CCIO</sub> (V)			V <sub>SWING(DC)</sub> (V)		V <sub>SWING(AC)</sub> (V)		V <sub>X(AC)</sub> (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V <sub>CCIO</sub> + 0.6	0.5	V <sub>CCIO</sub> + 0.6	V <sub>CCIO</sub> /2 - 0.175	—	V <sub>CCIO</sub> /2 + 0.175
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	<sup>(20)</sup>	2(V <sub>IH(AC)</sub> - V <sub>REF</sub> )	2(V <sub>REF</sub> - V <sub>IL(AC)</sub> )	V <sub>CCIO</sub> /2 - 0.15	—	V <sub>CCIO</sub> /2 + 0.15
SSTL-135	1.283	1.35	1.45	0.18	<sup>(20)</sup>	2(V <sub>IH(AC)</sub> - V <sub>REF</sub> )	2(V <sub>IL(AC)</sub> - V <sub>REF</sub> )	V <sub>CCIO</sub> /2 - 0.15	—	V <sub>CCIO</sub> /2 + 0.15
SSTL-125	1.19	1.25	1.31	0.18	<sup>(20)</sup>	2(V <sub>IH(AC)</sub> - V <sub>REF</sub> )	2(V <sub>IL(AC)</sub> - V <sub>REF</sub> )	V <sub>CCIO</sub> /2 - 0.15	—	V <sub>CCIO</sub> /2 + 0.15
SSTL-12	1.14	1.2	1.26	0.16	27	2(V <sub>IH(AC)</sub> - V <sub>REF</sub> )	2(V <sub>IL(AC)</sub> - V <sub>REF</sub> )	V <sub>REF</sub> - 0.15	V <sub>CCIO</sub> /2	V <sub>REF</sub> + 0.15

### Differential HSTL and HSUL I/O Standards Specifications

**Table 21. Differential HSTL and HSUL I/O Standards Specifications for Intel Stratix 10 Devices—Preliminary**

I/O Standard	V <sub>CCIO</sub> (V)			V <sub>DIF(DC)</sub> (V)		V <sub>DIF(AC)</sub> (V)		V <sub>X(AC)</sub> (V)			V <sub>CM(DC)</sub> (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.4	—	0.78	—	1.12	0.78	—	1.12
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.4	—	0.68	—	0.9	0.68	—	0.9
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V <sub>CCIO</sub> + 0.3	0.3	V <sub>CCIO</sub> + 0.48	—	0.5 × V <sub>CCIO</sub>	—	0.4 × V <sub>CCIO</sub>	0.5 × V <sub>CCIO</sub>	0.6 × V <sub>CCIO</sub>
HSUL-12	1.14	1.2	1.3	2(V <sub>IH(DC)</sub> - V <sub>REF</sub> )	2(V <sub>REF</sub> - V <sub>IH(DC)</sub> )	2(V <sub>IH(AC)</sub> - V <sub>REF</sub> )	2(V <sub>REF</sub> - V <sub>IH(AC)</sub> )	0.5 × V <sub>CCIO</sub> - 0.12	0.5 × V <sub>CCIO</sub>	0.5 × V <sub>CCIO</sub> + 0.12	0.4 × V <sub>CCIO</sub>	0.5 × V <sub>CCIO</sub>	0.6 × V <sub>CCIO</sub>

<sup>(20)</sup> The maximum value for V<sub>SWING(DC)</sub> is not defined. However, each single-ended signal needs to be within the respective single-ended limits (V<sub>IH(DC)</sub> and V<sub>IL(DC)</sub>).



## Differential I/O Standards Specifications

**Table 22. Differential I/O Standards Specifications for Intel Stratix 10 Devices—Preliminary**

I/O Standard	V <sub>CCIO</sub> (V)			V <sub>ID</sub> (mV) <sup>(21)</sup>		V <sub>ICM(DC)</sub> (V)			V <sub>OD</sub> (V) <sup>(22) (23)</sup>			V <sub>OCM</sub> (V) <sup>(22)</sup>		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVDS <sup>(24)</sup>	1.71	1.8	1.89	100	—	0.05	Data rate ≤700 Mbps	1.65	0.247	—	0.6	1.125	1.25	1.375
						1	Data rate >700 Mbps	1.6						
RSDS <sup>(25)</sup>	1.71	1.8	1.89	100	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS <sup>(26)</sup>	1.71	1.8	1.89	200	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL <sup>(27)</sup>	1.71	1.8	1.89	300	—	0.6	Data rate ≤700 Mbps	1.7	—	—	—	—	—	—
						1	Data rate >700 Mbps	1.6						

## Switching Characteristics

This section provides the performance characteristics of Intel Stratix 10 core and periphery blocks.

- 
- (21) The minimum V<sub>ID</sub> value is applicable over the entire common mode range, V<sub>CM</sub>.
- (22) R<sub>L</sub> range: 90 ≤ R<sub>L</sub> ≤ 110 Ω.
- (23) The specification is only applicable to default V<sub>OD</sub> setting.
- (24) For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rates above 700 Mbps and 0.05 V to 1.65 V for data rates below 700 Mbps.
- (25) For optimized RSDS receiver performance, the receiver voltage input range must be within 0.3 V to 1.4 V.
- (26) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be within 0.4 V to 1.325 V.
- (27) For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.



## L-Tile Transceiver Performance Specifications

### Transceiver Performance for Intel Stratix 10 GX/SX L-Tile Devices

**Table 23. Intel Stratix 10 GX/SX L-Tile Transmitter and Receiver Datarate Performance**

Symbol/Description	Transceiver Speed Grade		
	-1	-2	-3
Chip-to-chip	N/A	26.6 Gbps 8 channels per tile <sup>(28)</sup>	17.4 Gbps
Backplane	N/A	12.5 Gbps	12.5 Gbps

**Note:** Refer to the *Transceiver Power Supply Operating Conditions* for  $V_{CCR\_GXB}$  and  $V_{CCT\_GXB}$  specifications when using bonded and non-bonded transceiver channels in Intel Stratix 10 L-Tile devices.

**Table 24. L-Tile ATX PLL Performance**

Symbol/Description	Condition	Transceiver Speed Grade 2	Transceiver Speed Grade 3	Unit
Supported Output Frequency	Maximum Frequency	13.3	8.7	GHz
	Minimum Frequency	500		MHz
$t_{LOCK}$ <sup>(29)</sup>	Maximum Frequency	1		ms
$t_{ARESET}$ Required Reset Time <sup>(30)</sup>	—	25		Avalon Clock Cycles

<sup>(28)</sup> Refer to *AN-778: Intel Stratix 10 Transceiver Usage* for more details on channel selection requirements.

<sup>(29)</sup> This specification applies after the ATX PLL, fPLL, or CMU PLL has completed calibration.

<sup>(30)</sup> You must use the Avalon-MM interface to hold the PLLs in reset for the specified cycles by writing to the ATX PLL, fPLL, or CMU PLL `pll_powerdown` register.



**Table 25. L-Tile Fractional PLL Performance**

Symbol/Description	Condition	All Transceiver Speed Grades	Unit
Supported Output Frequency	Maximum Frequency	6.25	GHz
	Minimum Frequency	500	MHz
t <sub>LOCK</sub> <sup>(29)</sup>	Maximum Frequency	1	ms
t <sub>ARESET</sub> Required Reset Time <sup>(30)</sup>	—	25	Avalon Clock Cycles

**Table 26. L-Tile CMU PLL Performance**

Symbol/Description	Condition	All Transceiver Speed Grades	Unit
Supported Output Frequency	Maximum Frequency	5.15625	GHz
	Minimum Frequency	2.450	GHz
t <sub>LOCK</sub> <sup>(29)</sup>	Maximum Frequency	1	ms
t <sub>ARESET</sub> Required Reset Time <sup>(30)</sup>	—	25	Avalon Clock Cycles

**Related Links**

[AN-778: Intel Stratix 10 Transceiver Usage](#)

**Transceiver Specifications for Intel Stratix 10 GX/SX L-Tile Devices**

**Table 27. L-Tile Reference Clock Specifications**

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	Dedicated reference clock pin	CML, Differential LVPECL, LVDS, and HCSL			
	RX reference clock pin	CML, Differential LVPECL, and LVDS			
Input Reference Clock Frequency (CMU PLL)		61	—	800	MHz
Input Reference Clock Frequency (ATX PLL)		100	—	800	MHz

*continued...*





Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Input Reference Clock Frequency (f <sub>PLL</sub> PLL)		50 <sup>(31)</sup>	—	800	MHz
Rise time	20% to 80%	—	—	350	ps
Fall time	80% to 20%	—	—	350	ps
Duty cycle	—	45	—	55	%
Spread-spectrum modulating clock frequency	PCIe	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to -0.5	—	%
On-chip termination resistors	—	—	100	—	Ω
Absolute V <sub>MAX</sub>	Dedicated reference clock pin	—	—	1.6	V
	RX reference clock pin	—	—	1.2	V
Absolute V <sub>MIN</sub>	—	-0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	mV
V <sub>ICM</sub> (AC coupled)	V <sub>CCR_GXB</sub> = 1.03 V	—	0	—	V
V <sub>ICM</sub> (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	mV
Transmitter REFCLK Phase Noise (800 MHz) <sup>(32)</sup>	100 Hz	—	—	-70	dBc/Hz
	1 kHz	—	—	-90	dBc/Hz
	10 kHz	—	—	-100	dBc/Hz
	100 kHz	—	—	-110	dBc/Hz
	≥ 1 MHz	—	—	-120	dBc/Hz

*continued...*

<sup>(31)</sup> The f<sub>MIN</sub> is 29 MHz when the f<sub>PLL</sub> is used as a core PLL.

<sup>(32)</sup> To calculate the REFCLK phase noise requirement at frequencies other than 800 MHz, use the following formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 800 MHz + 20\*log(f/800).



Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Transmitter REFCLK Phase Jitter (100 MHz)	1.5 MHz to 100 MHz (PCIe)	—	—	4.2	ps (rms)
R <sub>REF</sub>	—	2.0 k ±1%	—	2.0 k ±1%	Ω
T <sub>SSC-MAX-PERIOD-SLEW</sub>	Max spread spectrum clocking (SSC) df/dt			0.75	

**Table 28. L-Tile Transceiver Clock Network Maximum Data Rate Specifications**

Clock Network	Maximum Performance <sup>(33)</sup>			Channel Span	Unit
	ATX	fPLL	CMU		
x1	17.4	12.5	10.3125	6 channels	Gbps
x6	17.4	12.5	N/A	6 channels	Gbps
x24	17.4 <sup>(36)</sup>	12.5	N/A	2 banks up and 1 bank down (total 24 channels) or 2 banks down and 1 bank up (total 24 channels)	Gbps
GXT clock lines	26.6	N/A	N/A	4 GXT channels within the same transceiver bank and 2 from the bank above or 2 from the bank below. <sup>(34)</sup>	Gbps

<sup>(33)</sup> The maximum data rate depends on speed grade.

<sup>(34)</sup> If the upper ATX PLL in a bank is used as the main GXT PLL, then the channel span includes two GXT channels from the bank above. If the lower ATX PLL in a bank is used as the main GXT PLL, then the channel span includes two GXT channels from the bank below.



**Table 29. L-Tile Receiver Specifications**

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O, CML, Differential LVPECL, and LVDS			
Absolute $V_{MAX}$ for a receiver pin <sup>(35)</sup>	—	—	—	1.2	V
Absolute $V_{MIN}$ for a receiver pin <sup>(35)</sup>	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p)	$V_{CCR\_GXB} = 1.03\text{ V}$ <sup>(36)</sup>	—	—	2.0	V
Differential on-chip termination resistors	85- $\Omega$ setting	—	$85 \pm 20\%$	—	$\Omega$
	100- $\Omega$ setting	—	$100 \pm 20\%$	—	$\Omega$
$V_{ICM}$ (AC and DC coupled)	$V_{CCR\_GXB} = 1.03\text{ V}$	—	700	—	mV
	$V_{CCR\_GXB} = 1.12\text{ V}$	—	750	—	mV
$t_{LTR}$ <sup>(37)</sup>	—	—	—	1	ms
$t_{LTD}$ <sup>(38)</sup>	—	4	—	—	$\mu\text{s}$
$t_{LTD\_manual}$ <sup>(39)</sup>	—	4	—	—	$\mu\text{s}$

*continued...*

<sup>(35)</sup> The device cannot tolerate prolonged operation at this absolute maximum.

<sup>(36)</sup> Bonded channels operating at data rates above 16 Gbps require  $1.12\text{ V} \pm 20\text{ mV}$  at the pin. For a given L-Tile, if there are channels that need the higher power supply, tie all the channels on that side to the higher power supply.

<sup>(37)</sup>  $t_{LTR}$  is the time required for the receiver CDR to lock to the input reference clock frequency after coming out of reset, or after the CDR's calibration is complete.

<sup>(38)</sup>  $t_{LTD}$  is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedto data` signal goes high.

<sup>(39)</sup>  $t_{LTD\_manual}$  is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedto data` signal goes high when the CDR is functioning in the manual mode.



Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
$t_{LTR\_LTD\_manual}^{(40)}$	—	15	—	—	$\mu s$
Run Length	—	—	—	200	UI
CDR ppm tolerance	PCIe-only	-300	—	300	ppm
	All other protocols	-1000	—	1000	ppm

**Table 30. L-Tile Transmitter Specifications**

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O <sup>(41)</sup>			—
Differential on-chip termination resistors	85- $\Omega$ setting	—	$85 \pm 20\%$	—	$\Omega$
	100- $\Omega$ setting	—	$100 \pm 20\%$	—	$\Omega$
$V_{OCM}$ (AC coupled)	$V_{CCT\_GXB} = 1.03 V$	—	515	—	mV
Rise time <sup>(42)</sup>	20% to 80%	20	—	130	ps
Fall time <sup>(42)</sup>	80% to 20%	20	—	130	ps
Intra-differential pair skew	TX $V_{CM} = 0.5 V$ and slew rate of 15 ps	—	—	15 <sup>(43)</sup>	ps

(40)  $t_{LTR\_LTD\_manual}$  is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedto_ref` signal goes high when the CDR is functioning in the manual mode.

(41) High Speed Differential I/O is the dedicated I/O standard for the transmitter in Intel Stratix 10 transceivers.

(42) The Intel Quartus Prime software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(43) This specification pertains to Hyper Memory Cube.



**Table 31. L-Tile Typical Transmitter V<sub>OD</sub> Settings**

Symbol	V <sub>OD</sub> Setting	V <sub>OD</sub> /V <sub>CCT_GXB</sub> Ratio
V <sub>OD</sub> differential value = V <sub>OD</sub> /V <sub>CCT_GXB</sub> ratio x V <sub>CCT_GXB</sub>	31	1.00
	30	0.97
	29	0.93
	28	0.90
	27	0.87
	26	0.83
	25	0.80
	24	0.77
	23	0.73
	22	0.70
	21	0.67
	20	0.63
	19	0.60
	18	0.57
	17	0.53
	16	0.50
	15	0.47
	14	0.43
13	0.40	
12	0.37	

**Table 32. L-Tile Transmitter Channel-to-channel Skew Specifications**

Mode	Channel Span	Maximum Skew	Unit
x6 Clock	Up to 6 channels in one bank	61	ps
x24 Clock	Up to 24 channels in one tile	500 <sup>(44)</sup>	ps



**Table 33. Transceiver Clocks Specifications for Intel Stratix 10 GX/SX L-Tile Devices**

Clock	Value	Unit
reconfig_clk	≤ 150	MHz
fixed_clk for the RX detect circuit	250 ± 20%	MHz

For OSC\_CLK\_1 specifications, refer to the External Configuration Clock Source Requirements section.

**Related Links**

- [External Configuration Clock Source Requirements](#) on page 86
- [PLLs and Clock Networks](#)

**H-Tile Transceiver Performance Specifications**

**Transceiver Performance for Intel Stratix 10 GX/SX H-Tile Devices**

**Table 34. Intel Stratix 10 GX/SX H-Tile Transmitter and Receiver Datarate Performance—Preliminary**

Symbol	Description	Transceiver Speed Grade		
		-1	-2	-3
GX channels	Chip-to-chip and Backplane	17.4 Gbps		
GXT channels	Chip-to-chip and Backplane	28.3 Gbps	25.8 Gbps	17.4 Gbps

*Note:* Refer to the *Transceiver Power Supply Operating Conditions* for  $V_{CCR\_GXB}$  and  $V_{CCT\_GXB}$  specifications when using bonded and non-bonded transceiver channels in Intel Stratix 10 H-Tile devices.

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(44) 500 ps is not supported for all configurations and depends upon the Master CGB placement.



**Table 35. H-Tile ATX PLL Performance—Preliminary**

Symbol/Description	Condition	Transceiver Speed Grade 1	Transceiver Speed Grade 2	Transceiver Speed Grade 3	Unit
Supported Output Frequency	Maximum Frequency	14.15	12.9	8.7	GHz
	Minimum Frequency	500			MHz
t <sub>LOCK</sub> <sup>(45)</sup>	Maximum Frequency	1			ms
t <sub>ARESET</sub> <sup>(46)</sup>	—	25			Avalon Clock Cycles

**Table 36. H-Tile Fractional PLL Performance—Preliminary**

Symbol/Description	Condition	All Transceiver Speed Grades	Unit
Supported Output Frequency	Maximum Frequency	6.25	GHz
	Minimum Frequency	500	MHz
t <sub>LOCK</sub> <sup>(45)</sup>	Maximum Frequency	1	ms
t <sub>ARESET</sub> <sup>(46)</sup>	—	25	Avalon Clock Cycles

**Table 37. H-Tile CMU PLL Performance—Preliminary**

Symbol/Description	Condition	All Transceiver Speed Grades	Unit
Supported Output Frequency	Maximum Frequency	5.15625	GHz
	Minimum Frequency	2.450	GHz
t <sub>LOCK</sub> <sup>(45)</sup>	Maximum Frequency	1	ms
t <sub>ARESET</sub> <sup>(46)</sup>	—	25	Avalon Clock Cycles

<sup>(45)</sup> This specification applies after the ATX PLL, fPLL, or CMU PLL has completed calibration.

<sup>(46)</sup> You must use the Avalon-MM interface to hold the PLLs in reset for the specified cycles by writing to the ATX PLL, fPLL, or CMU PLL `pll_powerdown` register.



## Transceiver Specifications for Intel Stratix 10 GX/SX H-Tile Devices

**Table 38. H-Tile Reference Clock Specifications—Preliminary**

Symbol/Description	Condition	Min	Typ	Max	Unit
Supported I/O Standards	Dedicated reference clock pin	CML, Differential LVPECL, LVDS, and HCSL			
	RX reference clock pin	CML, Differential LVPECL, and LVDS			
Input Reference Clock Frequency (CMU PLL)		61	—	800	MHz
Input Reference Clock Frequency (ATX PLL)		100	—	800	MHz
Input Reference Clock Frequency (fPLL PLL)		50 <sup>(47)</sup>	—	800	MHz
Rise time	20% to 80%	—	—	350	ps
Fall time	80% to 20%	—	—	350	ps
Duty cycle	—	45	—	55	%
Spread-spectrum modulating clock frequency	PCIe	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to -0.5	—	%
On-chip termination resistors	—	—	100	—	Ω
Absolute $V_{MAX}$	Dedicated reference clock pin	—	—	1.6	V
	RX reference clock pin	—	—	1.2	V
Absolute $V_{MIN}$	—	-0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	mV
$V_{ICM}$ (AC coupled)	$V_{CCR\_GXB} = 1.03$ V	—	1.03	—	V
	$V_{CCR\_GXB} = 1.12$ V	—	1.12	—	V
$V_{ICM}$ (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	mV
Transmitter REFCLK Phase Noise (800 MHz) <sup>(48)</sup>	100 Hz	—	—	-70	dBc/Hz
	1 kHz	—	—	-90	dBc/Hz

*continued...*

(47) The  $f_{MIN}$  is 29 MHz when the fPLL is used as a core PLL.





Symbol/Description	Condition	Min	Typ	Max	Unit
	10 kHz	—	—	-100	dBc/Hz
	100 kHz	—	—	-110	dBc/Hz
	≥ 1 MHz	—	—	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz)	1.5 MHz to 100 MHz (PCIe)	—	—	4.2	ps (rms)
R <sub>REF</sub>	—	—	2.0 k ±1%	—	Ω
T <sub>SSC-MAX-PERIOD-SLEW</sub>	Max SSC df/dt			0.75	

**Table 39. H-Tile Transceiver Clock Network Maximum Data Rate Specifications—Preliminary**

Clock Network	Maximum Performance <sup>(49)</sup>			Channel Span	Unit
	ATX	fPLL	CMU		
x1	17.4	12.5	10.3125	6 channels	Gbps
x6	17.4	12.5	N/A	6 channels	Gbps
x24	17.4 <sup>(53)</sup>	12.5	N/A	2 banks up and 1 bank down (total 24 channels) or 2 banks down and 1 bank up (total 24 channels)	Gbps
GXT clock lines	28.3	N/A	N/A	4 GXT channels within the same transceiver bank and 2 from the bank above or 2 from the bank below. <sup>(50)</sup>	Gbps

<sup>(48)</sup> To calculate the REFCLK phase noise requirement at frequencies other than 800 MHz, use the following formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 800 MHz + 20\*log(f/800).

<sup>(49)</sup> The maximum data rate depends on speed grade.

<sup>(50)</sup> If the upper ATX PLL in a bank is used as the main GXT PLL, then the channel span includes two GXT channels from the bank above. If the lower ATX PLL in a bank is used as the main GXT PLL, then the channel span includes two GXT channels from the bank below.



**Table 40. H-Tile Receiver Specifications—Preliminary**

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O, CML, Differential LVPECL, and LVDS			
Absolute $V_{MAX}$ for a receiver pin <sup>(51)</sup>	—	—	—	1.2	V
Absolute $V_{MIN}$ for a receiver pin <sup>(51)</sup>	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) before device configuration <sup>(52)</sup>	—	—	—	1.6	V
Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) after device configuration <sup>(52)</sup>	$V_{CCR\_GXB} = 1.03\text{ V}, 1.12\text{ V}$ <sup>(53), (55)</sup>	—	—	2.0	V
Differential on-chip termination resistors	85- $\Omega$ setting	—	$85 \pm 20\%$	—	$\Omega$
	100- $\Omega$ setting	—	$100 \pm 20\%$	—	$\Omega$
$V_{ICM}$ (AC and DC coupled) <sup>(54)</sup>	$V_{CCR\_GXB} = 1.03\text{ V}$ <sup>(55)</sup>	—	700	—	mV
	$V_{CCR\_GXB} = 1.12\text{ V}$ <sup>(55)</sup>	—	750	—	mV
$t_{LTR}$ <sup>(56)</sup>	—	—	—	1	ms

*continued...*

- (51) The device cannot tolerate prolonged operation at this absolute maximum.
- (52) DC coupling specifications are pending silicon characterization.
- (53) Bonded channels operating at data rates above 16 Gbps require  $1.12\text{ V} \pm 20\text{ mV}$  at the pin. For channels that are placed in the same H-Tile as the channels that required  $1.12\text{ V} \pm 20\text{ mV}$ ,  $V_{CCR\_GXB} = 1.12\text{ V} \pm 20\text{ mV}$ .
- (54) Intel Stratix 10 devices support DC coupling to other Intel Stratix 10 devices and other devices operating under the Hybrid Memory Cube (HMC) specifications.
- (55) For GXT channels,  $V_{CCR\_GXB}$  must be 1.12 V. For GX channels,  $V_{CCR\_GXB}$  must be 1.03 V.  $V_{CCR\_GXB}$  must be 1.12 V for the transceiver on the same H-Tile when using GX and GXT channels together.



Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
$t_{LTD}^{(57)}$	—	4	—	—	$\mu s$
$t_{LTD\_manual}^{(58)}$	—	4	—	—	$\mu s$
$t_{LTR\_LTD\_manual}^{(59)}$	—	15	—	—	$\mu s$
Run Length	—	—	—	200	UI
CDR ppm tolerance	PCIe-only	-300	—	300	ppm
	All other protocols	-1000	—	1000	ppm

**Table 41. H-Tile Transmitter Specifications—Preliminary**

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O <sup>(60)</sup>			—
Differential on-chip termination resistors	85- $\Omega$ setting	—	$85 \pm 20\%$	—	$\Omega$
	100- $\Omega$ setting	—	$100 \pm 20\%$	—	$\Omega$
$V_{OCM}$ (AC coupled)	$V_{CCT\_GXB} = 1.03 V^{(61)}$	—	515	—	mV
$V_{OCM}$ (AC coupled)	$V_{CCT\_GXB} = 1.12 V^{(61)}$	—	560	—	mV

*continued...*

- (56)  $t_{LTR}$  is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset or after CDR calibration is completed.
- (57)  $t_{LTD}$  is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedto data` signal goes high.
- (58)  $t_{LTD\_manual}$  is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedto data` signal goes high when the CDR is functioning in the manual mode.
- (59)  $t_{LTR\_LTD\_manual}$  is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedto ref` signal goes high when the CDR is functioning in the manual mode.
- (60) High Speed Differential I/O is the dedicated I/O standard for the transmitter in Intel Stratix 10 transceivers.



Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
V <sub>OCM</sub> (DC coupled)	V <sub>CCT_GXB</sub> = 1.03 V <sup>(61)</sup>	—	515	—	mV
V <sub>OCM</sub> (DC coupled)	V <sub>CCT_GXB</sub> = 1.12 V <sup>(61)</sup>	—	560	—	mV
Rise time <sup>(62)</sup>	20% to 80%	20	—	130	ps
Fall time <sup>(62)</sup>	80% to 20%	20	—	130	ps
Intra-differential pair skew	TX V <sub>CM</sub> = 0.5 V and slew rate of 15 ps	—	—	15 <sup>(63)</sup>	ps

**Table 42. H-Tile Typical Transmitter V<sub>OD</sub> Settings—Preliminary**

Symbol	V <sub>OD</sub> Setting	V <sub>OD</sub> /V <sub>CCT_GXB</sub> Ratio
V <sub>OD</sub> differential value = V <sub>OD</sub> /V <sub>CCT_GXB</sub> ratio x V <sub>CCT_GXB</sub>	31	1.00
	30	0.97
	29	0.93
	28	0.90
	27	0.87
	26	0.83
	25	0.80
	24	0.77
	23	0.73
	22	0.70

*continued...*

<sup>(61)</sup> For GXT channels, V<sub>CCT\_GXB</sub> must be 1.12 V. For GX channels, V<sub>CCT\_GXB</sub> must be 1.03 V. V<sub>CCT\_GXB</sub> must be 1.12 V when using GX and GXT channels together within the same H-Tile.

<sup>(62)</sup> The Intel Quartus Prime software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

<sup>(63)</sup> This specification pertains to Hyper Memory Cube.



Symbol	V <sub>OD</sub> Setting	V <sub>OD</sub> /V <sub>CCT_GXB</sub> Ratio
	21	0.67
	20	0.63
	19	0.60
	18	0.57
	17	0.53
	16	0.50
	15	0.47
	14	0.43
	13	0.40
	12	0.37

**Table 43. H-Tile Transmitter Channel-to-channel Skew Specifications—Preliminary**

Mode	Channel Span	Maximum Skew	Unit
x6 Clock	Up to 6 channels in one bank	61	ps
x24 Clock	Up to 24 channels in one bank	500 <sup>(64)</sup>	ps

**Table 44. Transceiver Clocks Specifications for Intel Stratix 10 GX/SX H-Tile Devices—Preliminary**

Clock	Value	Unit
reconfig_clk	≤ 150	MHz
fixed_clk for the RX detect circuit	250 ± 20%	MHz

For OSC\_CLK\_1 specifications, refer to the External Configuration Clock Source Requirements section.

**Related Links**

- [External Configuration Clock Source Requirements](#) on page 86

<sup>(64)</sup> 500 ps is not supported for all configurations and depends upon the Master CGB placement.



- PLLs and Clock Networks

## E-Tile Transceiver Performance Specifications

### Transceiver Performance for Intel Stratix 10 E-Tile Devices

**Table 45. E-Tile Transmitter and Receiver Data Rate Performance Specifications—Preliminary**

Symbol/Description	Condition	Minimum	Typical	Maximum	Unit
Supported datarate <sup>(65)</sup>	NRZ	1		30	Gbps
	PAM-4	2		57.8 <sup>(66)</sup>	Gbps

### Transceiver Reference Clock Specifications

**Table 46. E-Tile Reference Clock Specifications—Preliminary**

Symbol/Description	Condition	Minimum	Typical	Maximum	Unit
I/O standard		LVPECL			
Termination voltage (Vtt)	2.5 V compliant	0.4	0.5	0.6	V
	3.3 V tolerant	1.04	1.3	1.56	V
Termination resistor (Rtt)		40	50	60	ohm
Differential voltage (Vdiff)		0.4	0.8	1.2	V
Input common mode voltage (Vcm)	2.5 V compliant, no internal termination resistor	Vdiff/2		VCCN2P5V_IO-Vdiff/2	V
	2.5 V compliant, internal termination resistor	VCCN2P5V_IO-1.6	VCCN2P5V_IO-1.3	VCCN2P5V_IO-1	V

*continued...*

<sup>(65)</sup> The supported datarate is for chip-to-chip and backplane links.

<sup>(66)</sup> Two channels are combined to support up to 57.8 Gbps.



Symbol/Description	Condition	Minimum	Typical	Maximum	Unit
	3.3 V tolerant, no internal termination resistor	$V_{diff}/2$		$V_{CCN2P5V\_IO}-V_{diff}/2$	V
	3.3 V tolerant, internal termination resistor	1.4	2	2.6	V
Absolute voltage		-0.5		2.8	V

### Transmitter Specifications for Intel Stratix 10 E-Tile Devices

**Table 47. E-Tile Transmitter Specifications—Preliminary**

Symbol/Description	Condition	Minimum	Typical	Maximum	Unit
Transmitter differential output voltage peak-to-peak	No precursor/postcursor de-emphasis		0.965		V
Transmitter common mode voltage			$V_{CCERT}/2$		V

### Receiver Specifications for Intel Stratix 10 E-Tile Devices

**Table 48. E-Tile Receiver Specifications—Preliminary**

Symbol/Description	Condition	Minimum	Typical	Maximum	Unit
Receiver run length <sup>(67)</sup>				100 <sup>(68)</sup>	symbols
DC input impedance		40		60	ohm
DC differential input impedance		80	100	120	ohm
Powered down DC input impedance	Receiver pin impedance when the receiver termination is powered down	100k			ohm

*continued...*

<sup>(67)</sup> No additional transition density requirements apply.

<sup>(68)</sup> The incoming data must be statistically DC-balanced.



Symbol/Description	Condition	Minimum	Typical	Maximum	Unit
Electrical Idle detection voltage	-	65		175	mV
Differential termination	From DC to 100 MHz	80	100	120	ohm
PPM tolerance	Allowed frequency mismatch between REFCLK and RX data			750	ppm

## Core Performance Specifications

### Clock Tree Specifications

Table 49. Clock Tree Performance for Intel Stratix 10 Devices—Preliminary

Parameter	Performance			Unit
	-E1V, -I1V	-E2V, -E2L, -I2V, -I2L	-E3V, -E3X, -I3V, -I3X	
Programmable clock routing	1,100	900	780	MHz

### PLL Specifications

#### Fractional PLL Specifications

Table 50. Fractional PLL Specifications for Intel Stratix 10 Devices—Preliminary

These specifications are applicable when fPLL is used in core mode.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{IN}$	Input clock frequency	—	29	—	800 <sup>(69)</sup>	MHz
$f_{INPFD}$	Input clock frequency to the phase frequency detector (PFD)	—	29	—	700	MHz

*continued...*

<sup>(69)</sup> This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is dependent on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.





Symbol	Parameter	Condition	Min	Typ	Max	Unit
f <sub>VCO</sub>	PLL voltage-controlled oscillator (VCO) operating range for transceiver applications	—	6	—	12.5	GHz
	PLL voltage-controlled oscillator (VCO) operating range for core applications	—	4.3	—	12.5	GHz
t <sub>EINDUTY</sub>	Input clock duty cycle	—	40	—	60	%
f <sub>OUT</sub>	Output frequency for internal clock	—	—	—	1	GHz
f <sub>DYCONFIGCLK</sub>	Dynamic configuration clock for reconfig_clk	—	—	—	125	MHz
t <sub>LOCK</sub>	Time required to lock from end-of-device configuration	—	—	—	1	ms
t <sub>DLOCK</sub>	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
f <sub>CLBW</sub>	PLL closed-loop bandwidth	—	0.3	—	4	MHz
t <sub>PLL_PSERR</sub>	Accuracy of PLL phase shift	SmartVID	—	—	±50	ps
		Non-SmartVID	—	—	±75	ps
t <sub>INCCJ</sub> <sup>(70), (71)</sup>	Input clock cycle-to-cycle jitter	F <sub>REF</sub> ≥ 100 MHz	—	—	0.13	UI (p-p)
		F <sub>REF</sub> < 100 MHz	—	—	±650	ps (p-p)
t <sub>OUTPJ</sub> <sup>(72)</sup>	Period jitter for clock output	F <sub>OUT</sub> ≥ 100 MHz	—	—	600	ps (p-p)
		F <sub>OUT</sub> < 100 MHz	—	—	60	mUI (p-p)
<b>continued...</b>						

<sup>(70)</sup> A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

<sup>(71)</sup> F<sub>REF</sub> is f<sub>IN</sub>/N, specification applies when N = 1.

<sup>(72)</sup> External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specifications for Intel Stratix 10 Devices table.



Symbol	Parameter	Condition	Min	Typ	Max	Unit
t <sub>OUTCJ</sub> <sup>(72)</sup>	Cycle-to-cycle jitter for clock output	F <sub>OUT</sub> ≥ 100 MHz	—	—	600	ps (p-p)
		F <sub>OUT</sub> < 100 MHz	—	—	60	mUI (p-p)
dK <sub>BIT</sub>	Bit number of Delta Sigma Modulator (DSM)	—	—	32	—	bit

### Related Links

[Memory Output Clock Jitter Specifications](#) on page 54

Provides more information about the external memory interface clock output jitter specifications.

## I/O PLL Specifications

**Table 51. I/O PLL Specifications for Intel Stratix 10 Devices—Preliminary**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f <sub>IN</sub>	Input clock frequency	-1 speed grade	10	—	1,100 <sup>(73)</sup>	MHz
		-2 speed grade	10	—	900 <sup>(73)</sup>	MHz
		-3 speed grade	10	—	750 <sup>(73)</sup>	MHz
f <sub>INPFD</sub>	Input clock frequency to the PFD	—	10	—	325	MHz
f <sub>VCO</sub>	PLL VCO operating range	-1 speed grade	600	—	1,600	MHz
		-2 speed grade	600	—	1,434	MHz
		-3 speed grade	600	—	1,250	MHz
f <sub>CLBW</sub>	PLL closed-loop bandwidth	—	0.5	—	10	MHz
t <sub>EINDUTY</sub>	Input clock or external feedback clock input duty cycle	—	40	—	60	%
f <sub>OUT</sub>	Output frequency for internal clock (C counter)	-1 speed grade	—	—	1,100	MHz
		-2 speed grade	—	—	900	MHz

*continued...*

<sup>(73)</sup> This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is dependent on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.



Symbol	Parameter	Condition	Min	Typ	Max	Unit
f <sub>OUT_EXT</sub>	Output frequency for external clock output	-3 speed grade	—	—	750	MHz
		-1 speed grade	—	—	800	MHz
		-2 speed grade	—	—	720	MHz
		-3 speed grade	—	—	650	MHz
t <sub>OUTDUTY</sub>	Duty cycle for dedicated external clock output (when set to 50%)	—	45	50	55	%
t <sub>FCOMP</sub>	External feedback clock compensation time	—	—	—	5	ns
f <sub>DYCONFIGCLK</sub>	Dynamic configuration clock for mgmt_clk and scanclk	—	—	—	200	MHz
t <sub>LOCK</sub>	Time required to lock from end-of-device configuration or deassertion of areset	—	—	—	1	ms
t <sub>DLOCK</sub>	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
t <sub>PLL_PSERR</sub>	Accuracy of PLL phase shift	—	—	—	±50	ps
t <sub>ARESET</sub>	Minimum pulse width on the areset signal	—	10	—	—	ns
t <sub>INCCJ</sub> <sup>(74)(75)</sup>	Input clock cycle-to-cycle jitter	F <sub>REF</sub> ≥ 100 MHz	—	—	0.15	UI (p-p)
		F <sub>REF</sub> < 100 MHz	—	—	±750	ps (p-p)
t <sub>OUTPJ_DC</sub>	Period jitter for dedicated clock output	F <sub>OUT</sub> ≥ 100 MHz	—	—	175	ps (p-p)
		F <sub>OUT</sub> < 100 MHz	—	—	17.5	mUI (p-p)
t <sub>OUTCCJ_DC</sub>	Cycle-to-cycle jitter for dedicated clock output	F <sub>OUT</sub> ≥ 100 MHz	—	—	175	ps (p-p)
		F <sub>OUT</sub> < 100 MHz	—	—	17.5	mUI (p-p)
t <sub>OUTPJ_IO</sub> <sup>(76)</sup>	Period jitter for clock output on the regular I/O	F <sub>OUT</sub> ≥ 100 MHz	—	—	600	ps (p-p)

**continued...**

<sup>(74)</sup> A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

<sup>(75)</sup> F<sub>REF</sub> is f<sub>IN</sub>/N, specification applies when N = 1.



Symbol	Parameter	Condition	Min	Typ	Max	Unit
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
$t_{OUTCC1\_IO}$ <sup>(76)</sup>	Cycle-to-cycle jitter for clock output on the regular I/O	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$	Period jitter for dedicated clock output in cascaded PLLs	$F_{OUT} \geq 100$ MHz	—	—	175	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	17.5	mUI (p-p)

### Related Links

[Memory Output Clock Jitter Specifications](#) on page 54

Provides more information about the external memory interface clock output jitter specifications.

## DSP Block Specifications

**Table 52. DSP Block Performance Specifications for Intel Stratix 10 Devices—Preliminary**

Mode	Performance			Unit
	-E1V, -I1V	-E2V, -E2L, -I2V, -I2L	-E3V, -E3X, -I3V, -I3X	
Fixed-point 18 × 19 multiplication mode	1,000	771	667	MHz
Fixed-point 27 × 27 multiplication mode <sup>(77)</sup>	1,000	771	667	MHz
Fixed-point 18 × 18 multiplier adder mode <sup>(77)</sup>	1,000	771	667	MHz
Fixed-point 18 × 18 multiplier adder summed with 36-bit input mode <sup>(77)</sup>	1,000	771	667	MHz
Fixed-point 18 × 19 systolic mode	1,000	771	667	MHz
<i>continued...</i>				

<sup>(76)</sup> External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specifications for Intel Stratix 10 Devices table.

<sup>(77)</sup> When chainin or chainout is enabled, the performance specifications for the following speed grades are as follows:

- -E1V and -I1V: 750 MHz
- -E2V, -E2L, -I2V, and -I2L: 578 MHz
- -E3V, -E3X, -I3V, and -I3X: 507 MHz



Mode	Performance			Unit
	-E1V, -I1V	-E2V, -E2L, -I2V, -I2L	-E3V, -E3X, -I3V, -I3X	
Complex 18 × 19 multiplication mode	1,000	771	667	MHz
Floating point multiplication mode	750	579	500	MHz
Floating point adder or subtract mode	750	579	500	MHz
Floating point multiplier adder or subtract mode	750	579	500	MHz
Floating point multiplier accumulate mode	750	579	500	MHz
Floating point vector one mode	750	579	500	MHz
Floating point vector two mode	750	579	500	MHz

### Memory Block Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to **50%** output duty cycle. Use the Intel Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in  $f_{MAX}$ .

**Table 53. Memory Block Performance Specifications for Intel Stratix 10 Devices—Preliminary**

Memory	Mode	Performance			Unit
		-E1V, -I1V	-E2V, -E2L, -I2V, -I2L	-E3V, -E3X, -I3V, -I3X	
MLAB	Single port, all supported widths (×16/×32)	1,000	782	667	MHz
	Simple dual-port, all supported widths (×16/×32)	1,000	782	667	MHz
	Simple dual-port with read-during-write option	550	450	400	MHz
	ROM, all supported width (×16/×32)	1,000	782	667	MHz
M20K Block	Single-port, all supported widths	1,000	782	667	MHz
	Simple dual-port, all supported widths	1,000	782	667	MHz
	Simple dual-port, coherent read enabled	1,000	782	667	MHz

*continued...*



Memory	Mode	Performance			Unit
		-E1V, -I1V	-E2V, -E2L, -I2V, -I2L	-E3V, -E3X, -I3V, -I3X	
	Simple dual-port with the read-during-write option set to <b>Old Data</b> , all supported widths	800	640	560	MHz
	Simple dual-port with ECC enabled, 512 × 32	600	480	420	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	1,000	782	667	MHz
	True dual port, all supported widths	600	480	420	MHz
	Simple quad-port, all supported widths	600	480	420	MHz
	ROM, all supported widths	1,000	782	667	MHz
eSRAM	Simple dual-port	500–750	500–700	500–640	MHz

### Internal Temperature Sensing Diode Specifications

**Table 54. Internal Temperature Sensing Diode Specifications for Intel Stratix 10 Devices—Preliminary**

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time
-40 to 125 °C <sup>(78)</sup>	±5 °C	No	1 KSPS	< 1 ms

(78) Temperature range refers to junction temperature.



## External Temperature Sensing Diode Specifications

**Table 55. External Temperature Sensing Diode Specifications for Intel Stratix 10 Devices—Preliminary**

- The typical value is at 25°C.
- Diode accuracy improves with lower injection current.
- Absolute accuracy is dependent on third-party external diode ADC and integration specifics.

Description	Min	Typ	Max	Unit
$I_{bias}$ , diode source current	10	—	100	$\mu$ A
$V_{bias}$ , voltage across diode	0.3	—	0.9	V
Series resistance	—	—	< 1	$\Omega$
Diode ideality factor	—	1.03	—	—

## Internal Voltage Sensor Specifications

**Table 56. Internal Voltage Sensor Specifications for Intel Stratix 10 Devices—Preliminary**

Parameter	Minimum	Typical	Maximum	Unit	
Resolution	—	8	—	Bit	
Sampling rate	—	—	1.0 <sup>(79)</sup>	KSPS	
Differential non-linearity (DNL)	—	—	$\pm 1$	LSB	
Integral non-linearity (INL)	—	—	$\pm 1$	LSB	
Input capacitance	—	—	40	pF	
Clock frequency	—	—	550	MHz	
Unipolar Input Mode	Input signal range for $V_{sigp}$	0	—	1.5	V
	Common mode voltage on $V_{sign}$	0	—	0.25	V
	Input signal range for $V_{sigp} - V_{sign}$	0	—	1.25	V

(79) Pending silicon characterization.



## Peripheral Performance Specifications

This section describes the peripheral performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

## High-Speed I/O Specifications

**Table 57. High-Speed I/O Specifications for Intel Stratix 10 Devices—Preliminary**

When serializer/deserializer (SERDES) factor  $J = 3$  to  $10$ , use the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

Symbol		Condition	-E1V, -I1V			-E2V, -E2L, -I2L, -I2V			-E3V, -E3X, -I3X, -I3V			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\text{HCLK\_in}}$ (input clock frequency) True Differential I/O Standards		Clock boost factor $W = 1$ to $40$ <sup>(80)</sup>	10	—	800	10	—	700	10	—	625	MHz
$f_{\text{HCLK\_in}}$ (input clock frequency) Single-Ended I/O Standards		Clock boost factor $W = 1$ to $40$ <sup>(80)</sup>	10	—	625	10	—	625	10	—	525	MHz
$f_{\text{HCLK\_out}}$ (output clock frequency)		—	—	—	800 <sup>(81)</sup>	—	—	700 <sup>(81)</sup>	—	—	625 <sup>(81)</sup>	MHz
Transmitter	True Differential I/O Standards - $f_{\text{HSDR}}$ (data rate) <sup>(82)</sup>	SERDES factor $J = 4$ to $10$ <sup>(83)(85)</sup> <sup>(84)</sup>	<sup>(85)</sup>	—	1600 <sup>(86)</sup>	<sup>(85)</sup>	—	1434 <sup>(86)</sup>	<sup>(85)</sup>	—	1250 <sup>(86)</sup>	Mbps

*continued...*

<sup>(80)</sup> Clock Boost Factor ( $W$ ) is the ratio between the input data rate and the input clock rate.

<sup>(81)</sup> This is achieved by using the PHY clock network.

<sup>(82)</sup> Requires package skew compensation with PCB trace length.

<sup>(83)</sup> The  $F_{\text{max}}$  specification is based on the fast clock used for serial data. The interface  $F_{\text{max}}$  is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

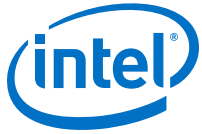




Symbol		Condition	-E1V, -I1V			-E2V, -E2L, -I2L, -I2V			-E3V, -E3X, -I3X, -I3V			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		SERDES factor J = 3 <sup>(83)(85)(84)</sup>	<sup>(85)</sup>	—	1,000 <sup>(86)</sup>	<sup>(85)</sup>	—	1,000 <sup>(86)</sup>	<sup>(85)</sup>	—	938 <sup>(86)</sup>	Mbps
		SERDES factor J = 2, uses DDR registers	<sup>(85)</sup>	—	840 <sup>(86)(87)</sup>	<sup>(85)</sup>	—	<sup>(86)(87)</sup>	<sup>(85)</sup>	—	<sup>(86)(87)</sup>	Mbps
		SERDES factor J = 1, uses DDR registers	<sup>(85)</sup>	—	420 <sup>(86)(87)</sup>	<sup>(85)</sup>	—	<sup>(86)(87)</sup>	<sup>(85)</sup>	—	<sup>(86)(87)</sup>	Mbps
	t <sub>x Jitter</sub> - True Differential I/O Standards	Total jitter for data rate, 600 Mbps - 1.6 Gbps	—	—	160	—	—	200	—	—	250	ps
		Total jitter for data rate, < 600 Mbps	—	—	0.1	—	—	0.12	—	—	0.15	UI
	t <sub>DUTY</sub> <sup>(88)</sup>	TX output clock duty cycle for Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
	t <sub>RISE</sub> & t <sub>FALL</sub> <sup>(84)(89)</sup>	True Differential I/O Standards	—	—	160	—	—	180	—	—	200	ps
TCCS <sup>(88)(82)</sup>	True Differential I/O Standards	—	—	330	—	—	330	—	—	330	ps	

*continued...*

- <sup>(84)</sup> The V<sub>CC</sub> and V<sub>CCP</sub> must be on a combined power layer and a maximum load of 5 pF for chip-to-chip interface.
- <sup>(85)</sup> The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and serializer do not have a minimum toggle rate.
- <sup>(86)</sup> Pending silicon characterization.
- <sup>(87)</sup> The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f<sub>OUT</sub>) provided you can close the design timing and the signal integrity meets the interface requirements.
- <sup>(88)</sup> Not applicable for DIVCLK = 1.
- <sup>(89)</sup> This applies to default pre-emphasis and V<sub>OD</sub> settings only.



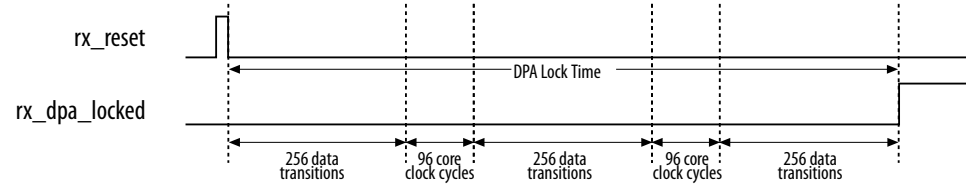
Symbol		Condition	-E1V, -I1V			-E2V, -E2L, -I2L, -I2V			-E3V, -E3X, -I3X, -I3V			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Receiver	True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 to 10 <sup>(83)(85)(84)</sup>	—	—	1600	—	—	1434	—	—	1250	Mbps
		SERDES factor J = 3 <sup>(83)(85)(84)</sup>	—	—	1,000 <sup>(86)</sup>	—	—	1,000 <sup>(86)</sup>	—	—	938 <sup>(86)</sup>	Mbps
	$f_{HSDR}$ (data rate) (without DPA) <sup>(82)</sup>	SERDES factor J = 3 to 10	<sup>(85)</sup>	—	<sup>(90)</sup>	<sup>(85)</sup>	—	<sup>(90)</sup>	<sup>(85)</sup>	—	<sup>(90)</sup>	Mbps
		SERDES factor J = 2, uses DDR registers	<sup>(85)</sup>	—	<sup>(87)</sup>	<sup>(85)</sup>	—	<sup>(87)</sup>	<sup>(85)</sup>	—	<sup>(87)</sup>	Mbps
		SERDES factor J = 1, uses DDR registers	<sup>(85)</sup>	—	<sup>(87)</sup>	<sup>(85)</sup>	—	<sup>(87)</sup>	<sup>(85)</sup>	—	<sup>(87)</sup>	Mbps
DPA (FIFO mode)	DPA run length	—	—	10000	—	—	10000	—	—	10000	UI	
DPA (soft CDR mode)	DPA run length	SGMII/GbE protocol	—	—	5	—	—	5	—	—	5	UI
		All other protocols	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—
Soft CDR mode	Soft-CDR ppm tolerance	—	-300	—	300	-300	—	300	-300	—	300	ppm
Non DPA mode	Sampling Window	—	—	—	330	—	—	330	—	—	330	ps

<sup>(90)</sup> You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.



### DPA Lock Time Specifications

**Figure 3. DPA Lock Time Specifications with DPA PLL Calibration Enabled**

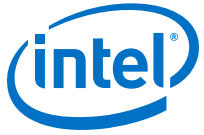


**Table 58. DPA Lock Time Specifications for Intel Stratix 10 Devices—Preliminary**

The specifications are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions <sup>(91)</sup>	Maximum Data Transition
SPI-4	00000000011111111111	2	128	640
Parallel Rapid I/O	00001111	2	128	640
	10010000	4	64	640
Miscellaneous	10101010	8	32	640
	01010101	8	32	640

<sup>(91)</sup> This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.



## LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

Figure 4. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Equal to 1.6 Gbps

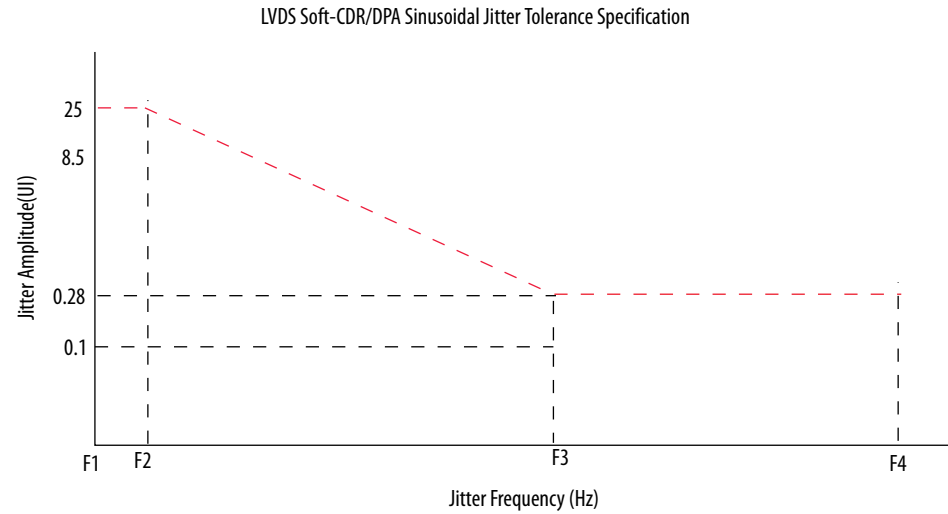
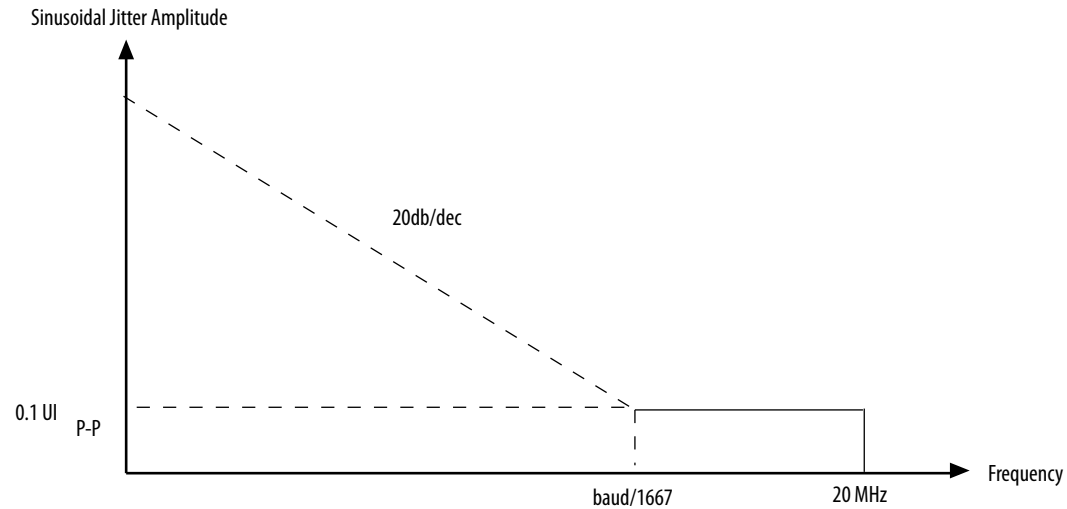


Table 59. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.6 Gbps—Preliminary

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.00
F2	17,565	25.00
F3	1,493,000	0.28
F4	50,000,000	0.28



**Figure 5. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Less than 1.6 Gbps**



### DLL Range Specifications

**Table 60. DLL Frequency Range Specifications for Intel Stratix 10 Devices—Preliminary**

Parameter	Performance (for All Speed Grades)	Unit
DLL operating frequency range	600 – 1,333 <sup>(92)</sup>	MHz
DLL reference clock input	Minimum 600 <sup>(93)</sup>	MHz

<sup>(92)</sup> In the SX device family, if the HPS EMIF is instantiated, the maximum speed for that instantiation is 1,066 MHz.

<sup>(93)</sup> To support interfaces below 600 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range.



## DQS Logic Block Specifications

**Table 61. DQS Phase Shift Error Specifications for DLL-Delayed Clock ( $t_{DQS\_PSERR}$ ) for Intel Stratix 10 Devices—Preliminary**

This error specification is the absolute maximum and minimum error.

Symbol	Performance			Unit
	-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	
$t_{DQS\_PSERR}$	4	6	8	ps

## Memory Output Clock Jitter Specifications

**Table 62. Memory Output Clock Jitter Specifications for Intel Stratix 10 Devices—Preliminary**

The clock jitter specification applies to the memory output clock pins clocked by an I/O PLL, or generated using differential signal-splitter and double data I/O circuits clocked by a PLL output routed on a PHY clock network as specified. Intel recommends using PHY clock networks for better jitter performance.

The memory output clock jitter is applicable when an input jitter of 10 ps peak-to-peak is applied with bit error rate (BER)  $10^{-12}$ , equivalent to 14 sigma.

Clock Network	Parameter	Symbol	Performance			Unit
			-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	
PHY clock	Clock period jitter	$t_{JIT(per)}$	58	58	58	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	58	58	58	ps
	Duty cycle jitter	$t_{JIT(duty)}$	58	58	58	ps

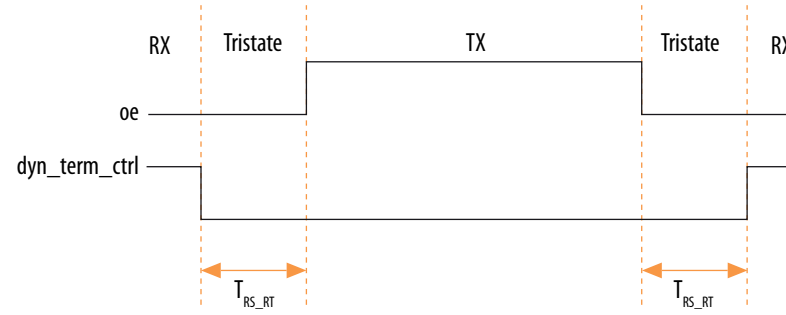
## OCT Calibration Block Specifications

**Table 63. OCT Calibration Block Specifications for Intel Stratix 10 Devices—Preliminary**

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
$T_{OCTCAL}$	Number of OCTUSRCLK clock cycles required for $R_S$ OCT / $R_T$ OCT calibration	> 2000	—	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
$T_{RS\_RT}$	Time required between the <code>dyn_term_ctrl</code> and <code>oe</code> signal transitions in a bidirectional I/O buffer to dynamically switch between $R_S$ OCT and $R_T$ OCT	—	TBD	—	ns



Figure 6. Timing Diagram for on oe and dyn\_term\_ctrl Signals





## HPS Performance Specifications - Preliminary

This section provides hard processor system (HPS) specifications and timing for Intel Stratix 10 devices.

### HPS Clock Performance - Preliminary

Table 64. Maximum HPS Clock Frequencies for Intel Stratix 10 Devices

Performance	VCCL_HPS (V)	MPU Frequency (MHz)	SDRAM Interconnect Frequency <sup>(94)</sup> (MHz)	L3 Interconnect Frequency (MHz)
-E1V, -I1V	SmartVID	1200	533	400
	0.9	1200	533	400
	0.94	TBD	533	400
-E2V, -I2V	SmartVID	1000	467	400
	0.9	1000	467	400
	0.94	1000	467	400
-E3V, -I3V	SmartVID	800	400	333
	0.9	800	400	333
	0.94	1000	400	400
-E2L, -I2L <sup>(95)</sup>	0.9	1200	467	400
	0.94	TBD	467	400
-E3X, -I3X <sup>(95)</sup>	0.9	1200	400	400
	0.94	TBD	400	400

#### Related Links

##### [External Memory Interface Spec Estimator](#)

Provides the specific details of the maximum allowed SDRAM operating frequency, which is twice the frequency of hmc\_free\_clk.

<sup>(94)</sup> hmc\_free\_clk

<sup>(95)</sup> Note that V<sub>CCL\_HPS</sub> can not be connected to SmartVID for -E2L, -I2L, -E3X, and -I3X devices.





## HPS PLL Specifications - Preliminary

### HPS PLL Input Requirements - Preliminary

**Table 65. HPS PLL Input Requirements for Intel Stratix 10 Devices**

The main HPS PLL receives its clock signals from the HPS\_OSC\_CLK pin. Refer to the *Intel Stratix 10 GX, MX, and SX Device Family Pin Connection Guidelines* for information about assigning this pin.

Description	Min	Typ	Max	Unit
Clock input range	25	—	125	MHz
Clock input accuracy	TBD	—	50	PPM
Clock input duty cycle	45	50	55	%

### HPS PLL Performance - Preliminary

**Table 66. HPS PLL Performance for Intel Stratix 10 Devices**

Description	Min	Max	Unit
Main PLL VCO output	—	3000	MHz
Peripheral PLL VCO output	—	3000	MHz
h2f_user0_clk <sup>(96)</sup>	—	500	MHz
h2f_user1_clk <sup>(96)</sup>	—	500	MHz

<sup>(96)</sup> The HPS PLL provides this clock to the FPGA fabric.



## HPS SPI Timing Characteristics - Preliminary

**Table 67. SPI Master Timing Requirements for Intel Stratix 10 Devices**

You can adjust the input delay timing by programming the `rx_sample_dly` register.

Symbol	Description	Min	Typ	Max	Unit
$T_{spi\_ref\_clk}$	The period of the SPI internal reference clock, sourced from <code>l4_main_clk</code>	5	—	—	ns
$T_{clk}$	SPIM_CLK clock period	16.67	—	—	ns
$T_{dutycycle}$	SPIM_CLK duty cycle	45	50	55	%
$T_{ck\_jitter}$	SPIM_CLK output jitter	—	—	2	%
$T_{dio}$	Master-out slave-in (MOSI) output skew	-3	—	2	ns
$T_{dssrst}^{(97)}$	SPI_SS_N asserted to first SPIM_CLK edge	$(1.5 \times T_{spi\_ref\_clk}) - \frac{2}{2}$	—	—	ns
$T_{dsslst}^{(97)}$	Last SPIM_CLK edge to SPI_SS_N deasserted	$T_{spi\_ref\_clk} - 2$	—	—	ns
$T_{su}^{(98)}$	SPIM_MISO setup time with respect to SPIM_CLK capture edge	$4.5 - (rx\_sample\_dly \times T_{spi\_ref\_clk})^{(99)}$	—	—	ns
$T_h^{(98)}$	Input hold in respect to SPIM_CLK capture edge	$1.3 + (rx\_sample\_dly \times T_{spi\_ref\_clk})$	—	—	ns

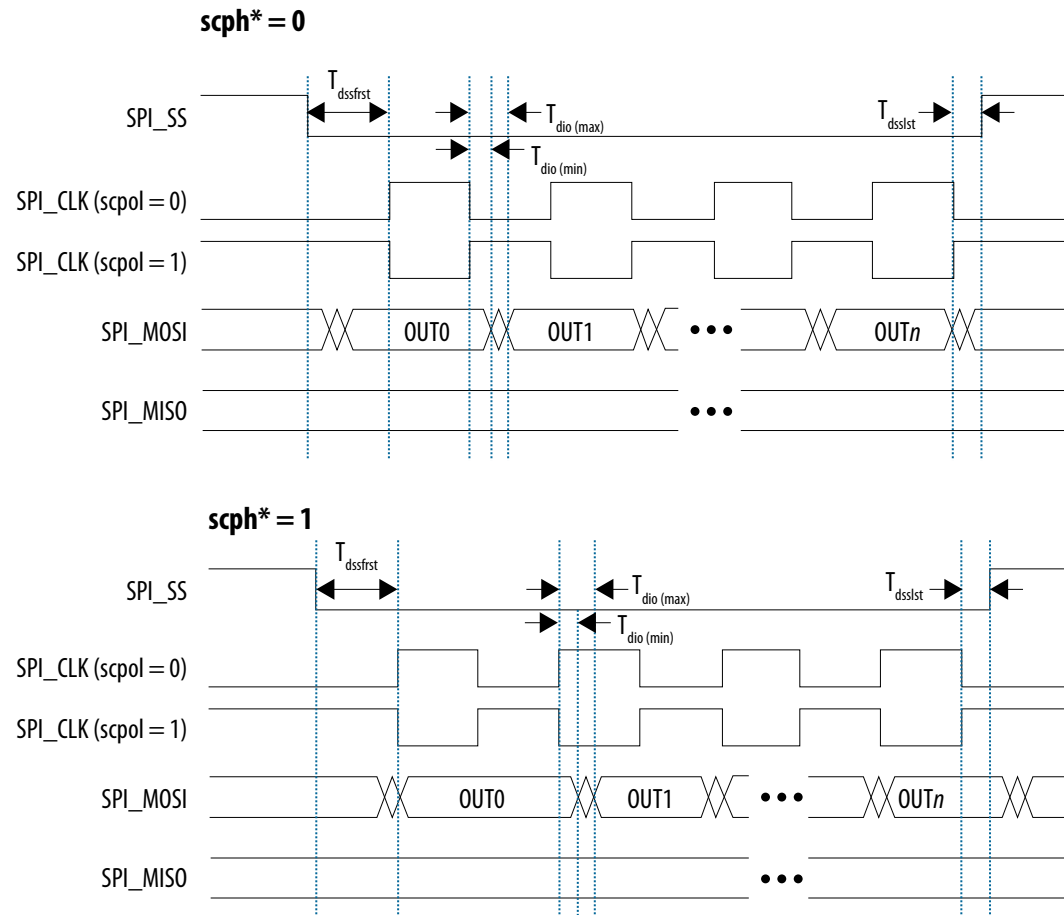
(97) SPI\_SS\_N behavior differs depending on Motorola SPI, TI SSP or Microwire operational mode.

(98) The capture edge differs depending on the operational mode. For Motorola SPI, the capture edge can be the rising or falling edge depending on the `scpol` register bit; for TI SSP, the capture edge is the falling edge; for Microwire, the capture edge is the rising edge.

(99) Valid values of `rx_sample_dly` range from 1 to 64 (units are in  $T_{spi\_ref\_clk}$  steps)

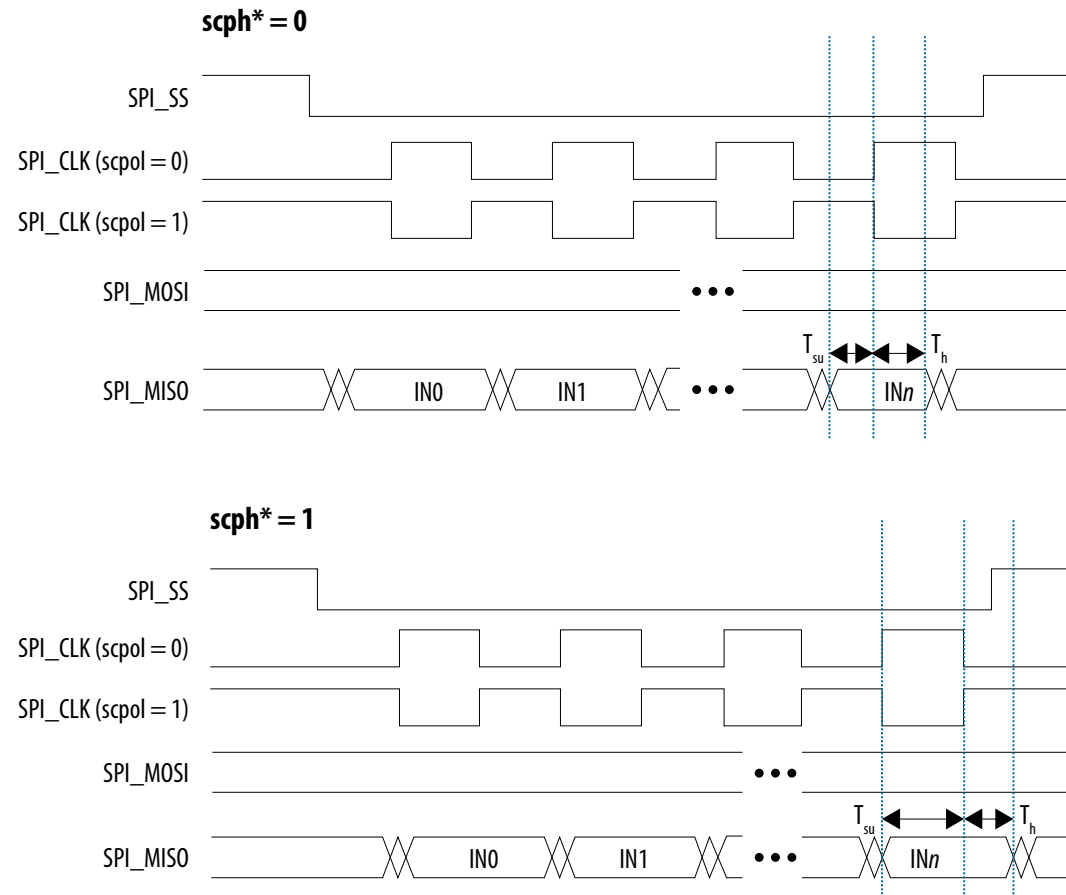


Figure 7. SPI Master Output Timing Diagram

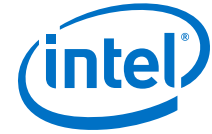


\*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Figure 8. SPI Master Input Timing Diagram



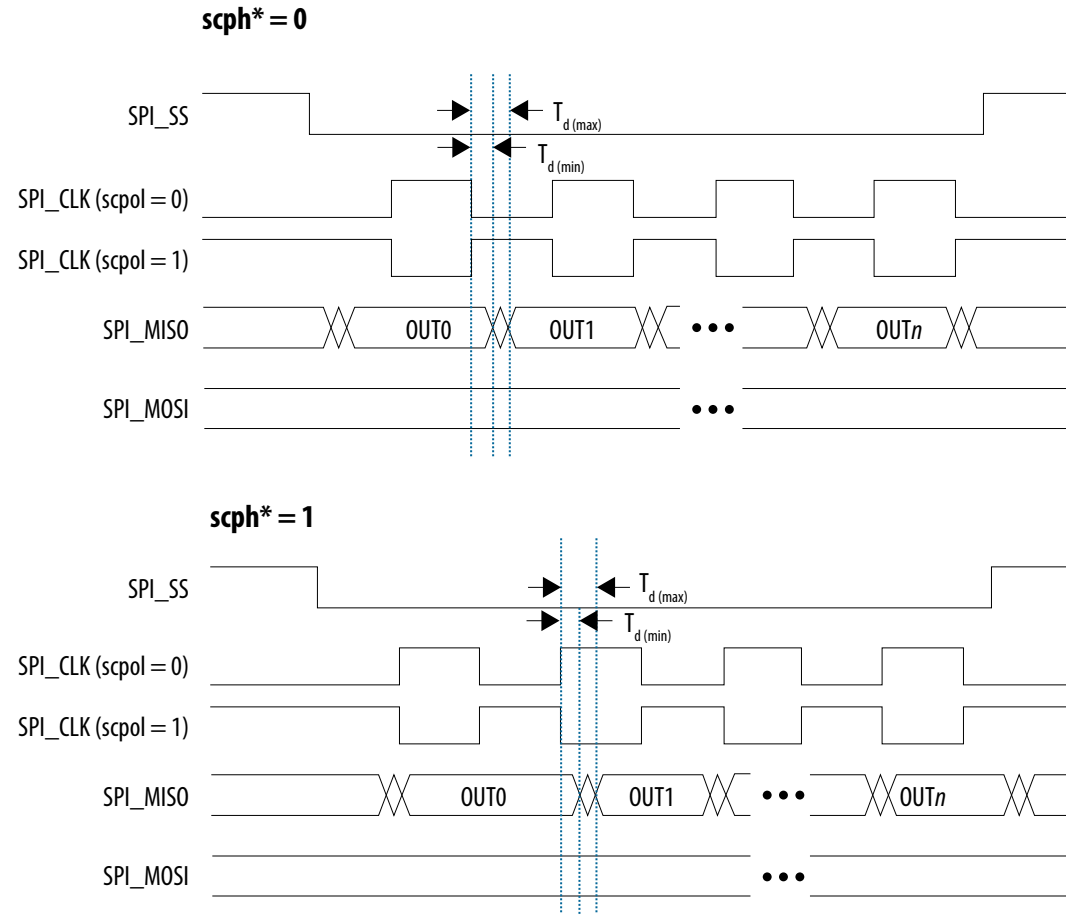
\*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register



**Table 68. SPI Slave Timing Requirements for Intel Stratix 10 Devices**

Symbol	Description	Min	Typ	Max	Unit
T <sub>spi_ref_clk</sub>	The period of the SPI internal reference clock, sourced from 14_main_clk	5	—	—	ns
T <sub>clk</sub>	SPIM_CLK clock period	30	—	—	ns
T <sub>dutycycle</sub>	SPIM_CLK duty cycle	45	50	55	%
T <sub>d</sub>	Master-in slave-out (MISO) output skew	$(2 \times T_{spi\_ref\_clk}) + 3$	—	$(3 \times T_{spi\_ref\_clk}) + 11$	ns
T <sub>su</sub>	Master-out slave-in (MOSI) setup time	4	—	—	ns
T <sub>h</sub>	Master-out slave-in (MOSI) hold time	0	—	—	ns
T <sub>ssuss</sub>	SPI_SS_N asserted to first SPIM_CLK edge	T <sub>spi_ref_clk</sub> + 4	—	—	ns
T <sub>hss</sub>	Last SPIM_CLK edge to SPI_SS_N deasserted	T <sub>spi_ref_clk</sub> + 4	—	—	ns

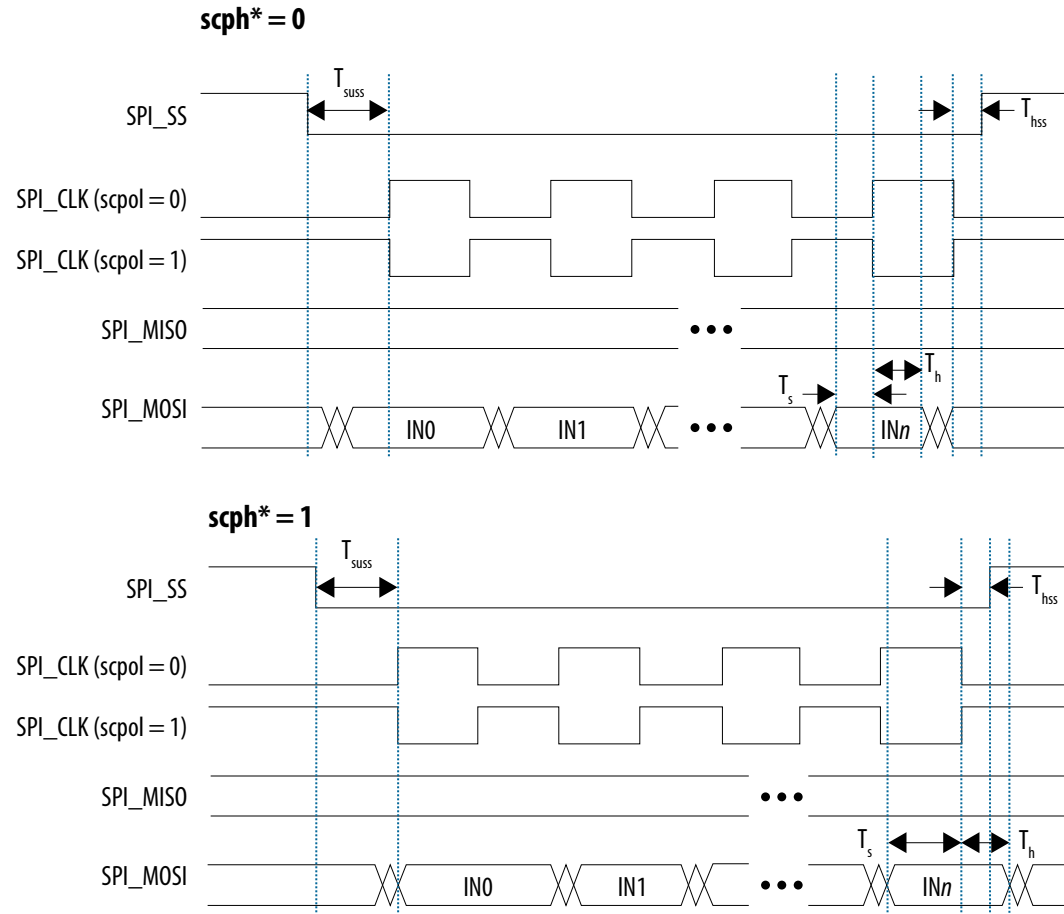
Figure 9. SPI Slave Output Timing Diagram



\*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register



Figure 10. SPI Slave Input Timing Diagram



\*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register



### **Related Links**

#### [SPI Controller](#)

For more information about the SPI controller and timing, refer to the *SPI Controller* chapter in the *Stratix 10 Hard Processor System Technical Reference Manual*





## HPS SD/MMC Timing Characteristics - Preliminary

**Table 69. Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Intel Stratix 10 Devices**

These timings apply to SD, MMC, and embedded MMC (eMMC) cards operating at 1.8 V.

Symbol	Description	Min	Typ	Max	Unit
T <sub>sdmmc_cclk</sub>	SDMMC_CCLK clock period (Identification mode)	2500	—	—	ns
	SDMMC_CCLK clock period (SDR12)	40	—	—	ns
	SDMMC_CCLK clock period (SDR25)	20	—	—	ns
T <sub>dutycycle</sub>	SDMMC_CCLK duty cycle	45	50	55	%
T <sub>sdmmc_cclk_jitter</sub>	SDMMC_CCLK output jitter	—	—	2	%
T <sub>sdmmc_clk</sub>	Internal reference clock before division by 4. Sourced by l4_mp_clk	5	—	—	ns
T <sub>d</sub>	SDMMC_CMD/SDMMC_DATA[7:0] output delay <sup>(100)</sup>	$T_{sdmmc\_clk} \times \text{drvsel}/2$ <sup>(101)</sup>	—	$3 + (T_{sdmmc\_clk} \times \text{drvsel}/2)$ <sup>(101)</sup>	ns
T <sub>su</sub>	SDMMC_CMD/SDMMC_DATA[7:0] input setup <sup>(102)</sup>	$6 - (T_{sdmmc\_clk} \times \text{smp1sel}/2)$	—	—	ns
T <sub>h</sub>	SDMMC_CMD/SDMMC_DATA[7:0] input hold <sup>(102)</sup>	$0.5 + (T_{sdmmc\_clk} \times \text{smp1sel}/2)$	—	—	ns

None of the HPS I/Os supports 3 V mode, while SD/MMC cards must operate at 3 V at power on. eMMC devices can operate at 1.8 V at power on.

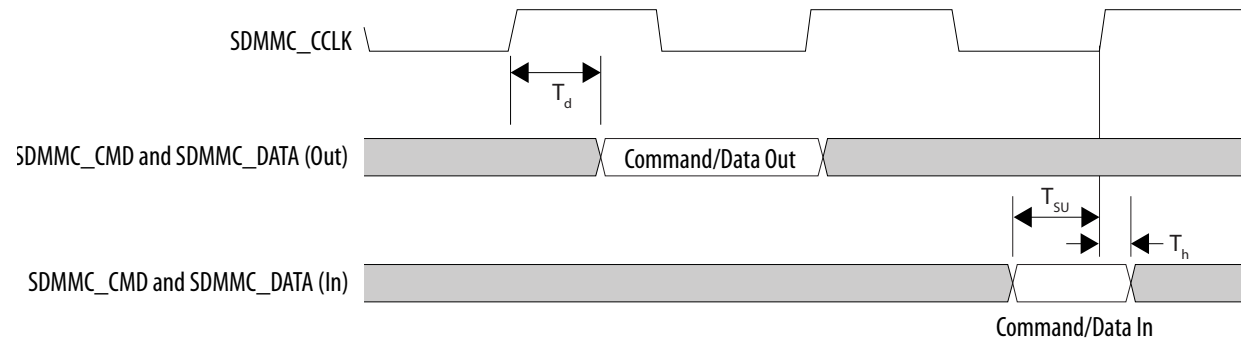
**Note:** SD cards power up at 3 V. To support SD, your design must include a level shifter between the SD card and the HPS SD/MMC interface.

<sup>(100)</sup> When the `drvsel` bitfield in the `sdmmc` register is set to 3 (in the system manager) and the reference clock (`l4_mp_clk`) is 200 MHz ) for example, the output delay time is 7.5 to 10.5 ns.

<sup>(101)</sup> `sdmmc_clk`, sourced from `l4_mp_clk`, is the SD/MMC controller reference clock.

<sup>(102)</sup> When the `smp1sel` bitfield in the `sdmmc` register is set to 2 (in the system manager) and the reference clock (`l4_mp_clk`) is 200 ) MHz for example, the setup time is 1 ns and the hold time is 5.5 ns.

Figure 11. SD/MMC Timing Diagram



### Related Links

#### [SD/MMC Controller](#)

For more information about the SD/MMC controller and timing, refer to the *SD/MMC Controller* chapter in the *Stratix 10 Hard Processor System Technical Reference Manual*

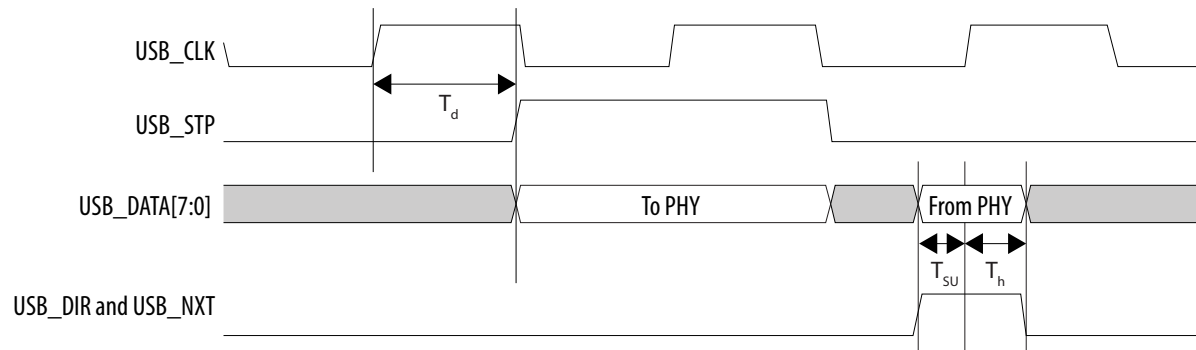


## HPS USB UPLI Timing Characteristics - Preliminary

**Table 70. USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) Timing Requirements for Intel Stratix 10 Devices**

Symbol	Description	Min	Typ	Max	Unit
$T_{usb\_clk}$	USB_CLK clock period	—	16.667	—	ns
$T_d$	Clock to USB_STP/USB_DATA[7:0] output delay	1.5	—	7	ns
$T_{su}$	Setup time for USB_DIR/USB_NXT/USB_DATA[7:0]	3.5	—	—	ns
$T_h$	Hold time for USB_DIR/USB_NXT/USB_DATA[7:0]	0.5	—	—	ns

**Figure 12. USB ULPI Timing Diagram**



**Note:** The USB interface supports single data rate (SDR) timing only.

### Related Links

#### [USB 2.0 OTG Controller](#)

For more information about the USB 2.0 OTG controller and timing, refer to the *USB 2.0 OTG Controller* chapter in the *Stratix 10 Hard Processor System Technical Reference Manual*

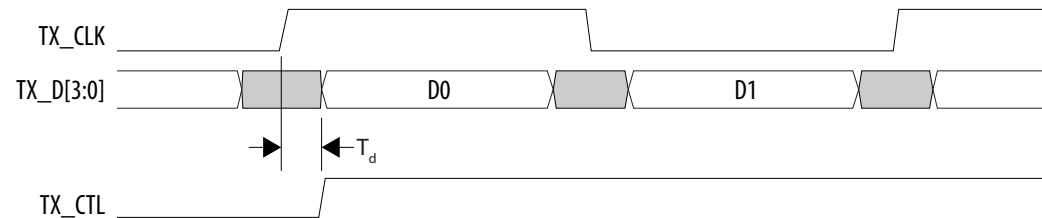


## HPS Ethernet Media Access Controller (EMAC) Timing Characteristics - Preliminary

**Table 71. Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Intel Stratix 10 Devices**

Symbol	Description	Min	Typ	Max	Unit
$T_{clk}$ (1000Base-T)	TX_CLK clock period	8 - 50 PPM	8	8 + 50 PPM	ns
$T_{clk}$ (100Base-T)	TX_CLK clock period	40 - 50 PPM	40	40 + 50 PPM	ns
$T_{clk}$ (10Base-T)	TX_CLK clock period	400 - 50 PPM	400	400 + 50 PPM	ns
$T_{duty\ cycle}$ (1000Base-T)	TX_CLK duty cycle	45	50	55	%
$T_{duty\ cycle}$ (10/100Base-T)	TX_CLK duty cycle	40	50	60	%
$T_d$ <sup>(103)</sup> (104)	TXD/TX_CTL to TX_CLK output skew	-0.5	—	0.5	ns

**Figure 13. RGMII TX Timing Diagram**



**Table 72. RGMII RX Timing Requirements for Intel Stratix 10 Devices**

Symbol	Description	Min	Typ	Max	Unit
$T_{clk}$ (1000Base-T)	RX_CLK clock period	8 - 50 PPM	8	8 + 50 PPM	ns
$T_{clk}$ (100Base-T)	RX_CLK clock period	40 - 50 PPM	40	40 + 50 PPM	ns

*continued...*

<sup>(103)</sup> Rise and fall times depend on the I/O standard, drive strength, and loading. Intel recommends simulating your configuration.  
)

<sup>(104)</sup> If you connect a PHY that does not implement clock-to-data skew, you can delay TX\_CLK by 1.5–2.0 ns with the HPS I/O programmable delay, to meet the PHY's 1-ns data-to-clock skew requirement.  
)



Symbol	Description	Min	Typ	Max	Unit
$T_{clk}$ (10Base-T)	RX_CLK clock period	400 - 50 PPM	400	400 + 50 PPM	ns
$T_{duty\ cycle}(1000\text{Base-T})$	RX_CLK duty cycle	45	50	55	%
$T_{duty\ cycle}(10/100\text{Base-T})$	RX_CLK duty cycle	40	50	60	%
$T_{su}$	RX_D/RX_CTL to RX_CLK setup time	1	—	—	ns
$T_h^{(105)}$	RX_CLK to RX_D/RX_CTL hold time	1	—	—	ns

Figure 14. RGMII RX Timing Diagram

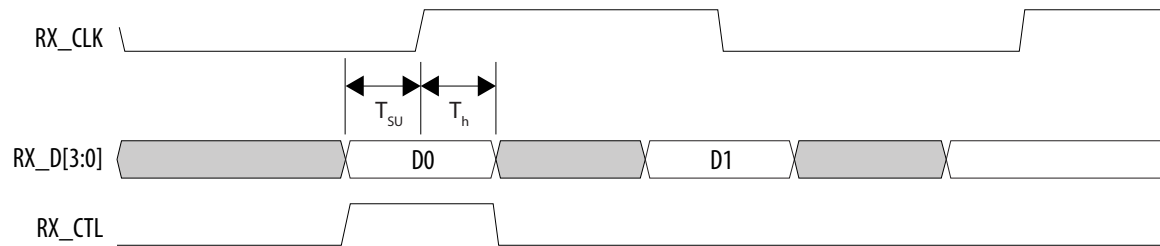


Table 73. Reduced Media Independent Interface (RMII) Clock Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Min	Typ	Max	Unit
$T_{clk}$	REF_CLK clock period, sourced by HPS TX_CLK	20 - 50 PPM	20	20 + 50 PPM	ns
	REF_CLK clock period, sourced by external clock source	20 - 50 PPM	20	20 + 50 PPM	ns
$T_{duty\ cycle\_int}$	Clock duty cycle, REF_CLK sourced by TX_CLK	35	50	65	%
$T_{duty\ cycle\_ext}$	Clock duty cycle, REF_CLK sourced by external clock source	35	50	65	%

Table 74. RMII TX Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Min	Typ	Max	Unit
$T_d$	TX_CLK to TXD/TX_CTL output data delay	2	—	10	ns

<sup>(105)</sup> If you connect a PHY that does not implement clock-to-data skew, you can meet the HPS EMAC's 1 ns setup time by delaying RX\_CLK by 1.5-2 ns, using the HPS I/O programmable delay.



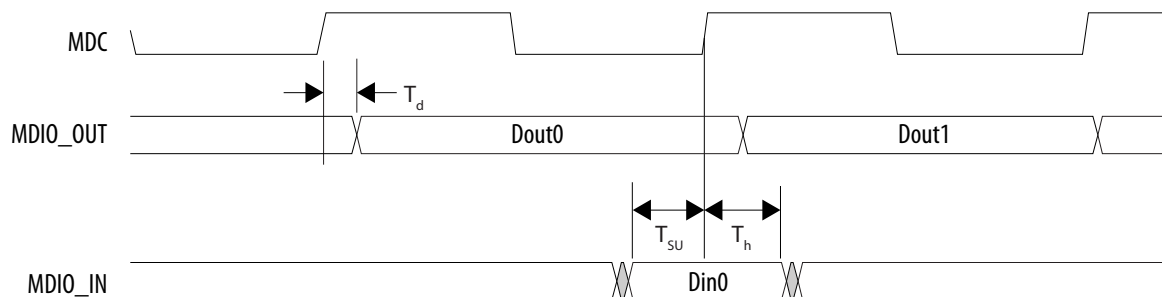
**Table 75. RMII RX Timing Requirements for Intel Stratix 10 Devices**

Symbol	Description	Min	Typ	Max	Unit
$T_{su}$	RX_D/RX_CTL setup time	2	—	—	ns
$T_h$	RX_D/RX_CTL hold time	1	—	—	ns

**Table 76. Management Data Input/Output (MDIO) Timing Requirements for Intel Stratix 10 Devices**

Symbol	Description	Min	Typ	Max	Unit
$T_{clk}$	MDC clock period	—	400	—	ns
$T_d$	MDC to MDIO output data delay	10	—	20	ns
$T_{su}$	Setup time for MDIO data	10	—	—	ns
$T_h$	Hold time for MDIO data	0	—	—	ns

**Figure 15. MDIO Timing Diagram**



**Related Links**

[Ethernet Media Access Controller](#)

For more information about the Ethernet MAC and timing, refer to the *Ethernet Media Access Controller* chapter in the *Stratix 10 Hard Processor System Technical Reference Manual*



## HPS I<sup>2</sup>C Timing Characteristics - Preliminary

**Table 77. I<sup>2</sup>C Timing Requirements for Intel Stratix 10 Devices**

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T <sub>clk</sub>	Serial clock (SCL) clock period	10	—	2.5	—	µs
T <sub>clk_jitter</sub>	I2C clock output jitter	—	2	—	2	%
T <sub>HIGH</sub> <sup>(106)</sup>	SCL high period	4 <sup>(107)</sup>	—	0.6 <sup>(108)</sup>	—	µs
T <sub>LOW</sub> <sup>(109)</sup>	SCL low period	4.7 <sup>(110)</sup>	—	1.3 <sup>(111)</sup>	—	µs
T <sub>SU;DAT</sub>	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1	—	µs
T <sub>HD;DAT</sub> <sup>(112)</sup>	Hold time for SCL to SDA data	0	3.15	0	0.6	µs
T <sub>VD;DAT</sub> and T <sub>VD;ACK</sub> <sup>(113)</sup>	SCL to SDA output data delay	—	3.45 <sup>(114)</sup>	—	0.9 <sup>(115)</sup>	µs

*continued...*

<sup>(106)</sup> You can adjust T<sub>high</sub> using the `ic_ss_scl_hcnt` or `ic_fs_scl_hcnt` register.  
)

<sup>(107)</sup> The recommended minimum setting for `ic_ss_scl_hcnt` is 440.  
)

<sup>(108)</sup> The recommended minimum setting for `ic_fs_scl_hcnt` is 71.  
)

<sup>(109)</sup> You can adjust T<sub>low</sub> using the `ic_ss_scl_lcnc` or `ic_fs_scl_lcnc` register.  
)

<sup>(110)</sup> The recommended minimum setting for `ic_ss_scl_lcnc` is 500.  
)

<sup>(111)</sup> The recommended minimum setting for `ic_fs_scl_lcnc` is 141.  
)

<sup>(112)</sup> T<sub>HD;DAT</sub> is affected by the rise and fall time.  
)



Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T <sub>SU;STA</sub>	Setup time for a repeated start condition	4.7	—	0.6	—	μs
T <sub>HD;STA</sub>	Hold time for a repeated start condition	4	—	0.6	—	μs
T <sub>SU;STO</sub>	Setup time for a stop condition	4	—	0.6	—	μs
T <sub>BUF</sub>	SDA high pulse duration between STOP and START	4.7	—	1.3	—	μs
T <sub>scl:r</sub> <sup>(116)</sup>	SCL rise time	—	1000	20	300	ns
T <sub>scl:f</sub> <sup>(116)</sup>	SCL fall time	—	300	6.54	300	ns
T <sub>sda:r</sub> <sup>(116)</sup>	SDA rise time	—	1000	20	300	ns
T <sub>sda:f</sub> <sup>(116)</sup>	SDA fall time	—	300	6.54	300	ns

<sup>(113)</sup> T<sub>V<sub>D</sub>;DAT</sub> and T<sub>V<sub>D</sub>;ACK</sub> are affected by the rise and fall time, as well as the SDA hold time (set by adjusting the ic\_sda\_hold register).

<sup>(114)</sup> Use maximum SDA\_HOLD = 240 to be within the specification.

<sup>(115)</sup> Use maximum SDA\_HOLD = 60 to be within the specification.

<sup>(116)</sup> Rise and fall time parameters vary depending on external factors such as the characteristics of the IO driver, pull-up resistor value, and total capacitance on the transmission line.



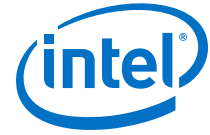
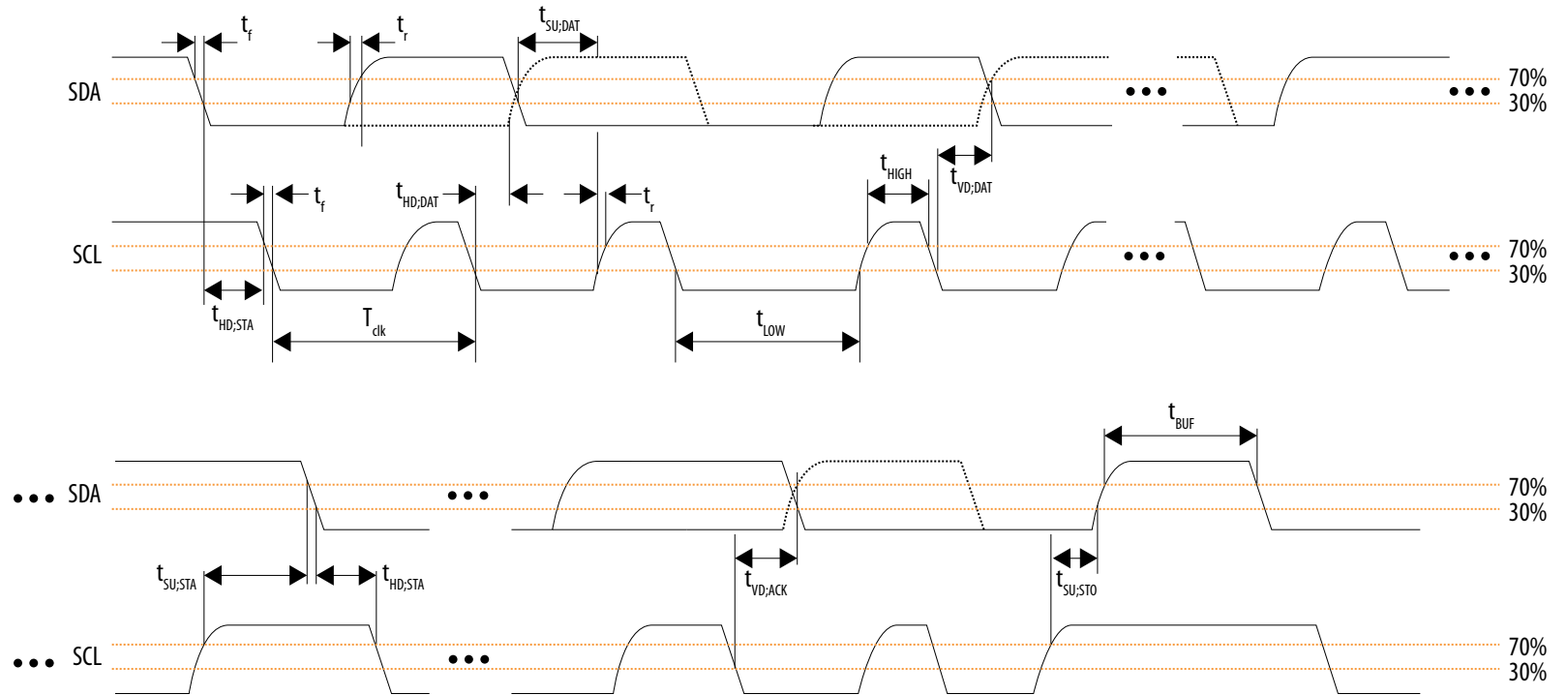


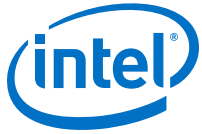
Figure 16. I<sup>2</sup>C Timing Diagram



**Related Links**

**I<sup>2</sup>C Controller**

For more information about the I<sup>2</sup>C controller and timing, refer to the *I<sup>2</sup>C Controller* chapter in the *Stratix 10 Hard Processor System Technical Reference Manual*



## HPS NAND Timing Characteristics - Preliminary

**Table 78. NAND ONFI 1.0 Timing Requirements for Intel Stratix 10 Devices**

Symbol	Description	Min	Max	Unit
T <sub>WP</sub> <sup>(117)</sup>	Write enable pulse width	10	—	ns
T <sub>WH</sub> <sup>(117)</sup>	Write enable hold time	7	—	ns
T <sub>RP</sub> <sup>(117)</sup>	Read enable pulse width	10	—	ns
T <sub>REH</sub> <sup>(117)</sup>	Read enable hold time	7	—	ns
T <sub>CLS</sub> <sup>(117)</sup>	Command latch enable to write enable setup time	10	—	ns
T <sub>CLH</sub> <sup>(117)</sup>	Command latch enable to write enable hold time	5	—	ns
T <sub>CS</sub> <sup>(117)</sup>	Chip enable to write enable setup time	15	—	ns
T <sub>CH</sub> <sup>(117)</sup>	Chip enable to write enable hold time	5	—	ns
T <sub>ALS</sub> <sup>(117)</sup>	Address latch enable to write enable setup time	10	—	ns
T <sub>ALH</sub> <sup>(117)</sup>	Address latch enable to write enable hold time	5	—	ns
T <sub>DS</sub> <sup>(117)</sup>	Data to write enable setup time	7	—	ns
T <sub>DH</sub> <sup>(117)</sup>	Data to write enable hold time	5	—	ns
T <sub>WB</sub> <sup>(117)</sup>	Write enable high to R/B low	—	200	ns
T <sub>CEA</sub>	Chip enable to data access time	—	100	ns
T <sub>REA</sub>	Read enable to data access time	—	40	ns
T <sub>RHZ</sub>	Read enable to data high impedance	—	200	ns
T <sub>RR</sub>	Ready to read enable low	20	—	ns

<sup>(117)</sup> This timing is software programmable. Refer to the *NAND Flash Controller* chapter in the *Stratix 10 Hard Processor System Technical Reference Manual* for more information about software-programmable timing in the NAND flash controller.

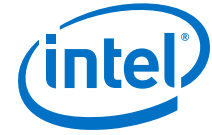


Figure 17. NAND Command Latch Timing Diagram

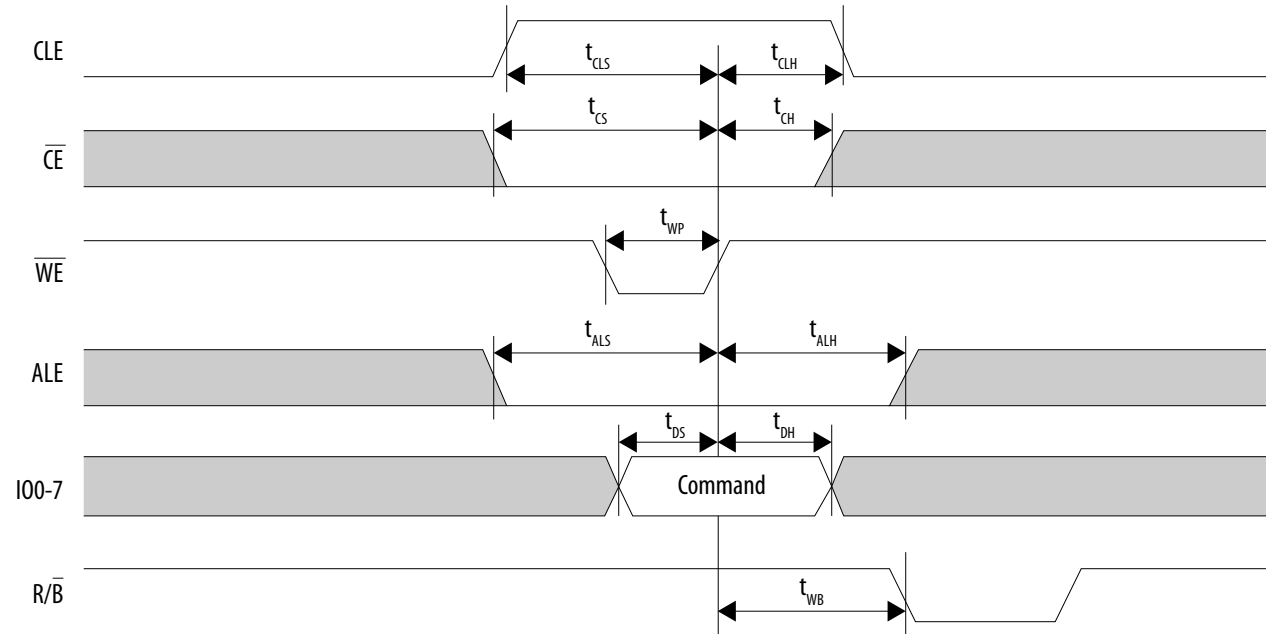
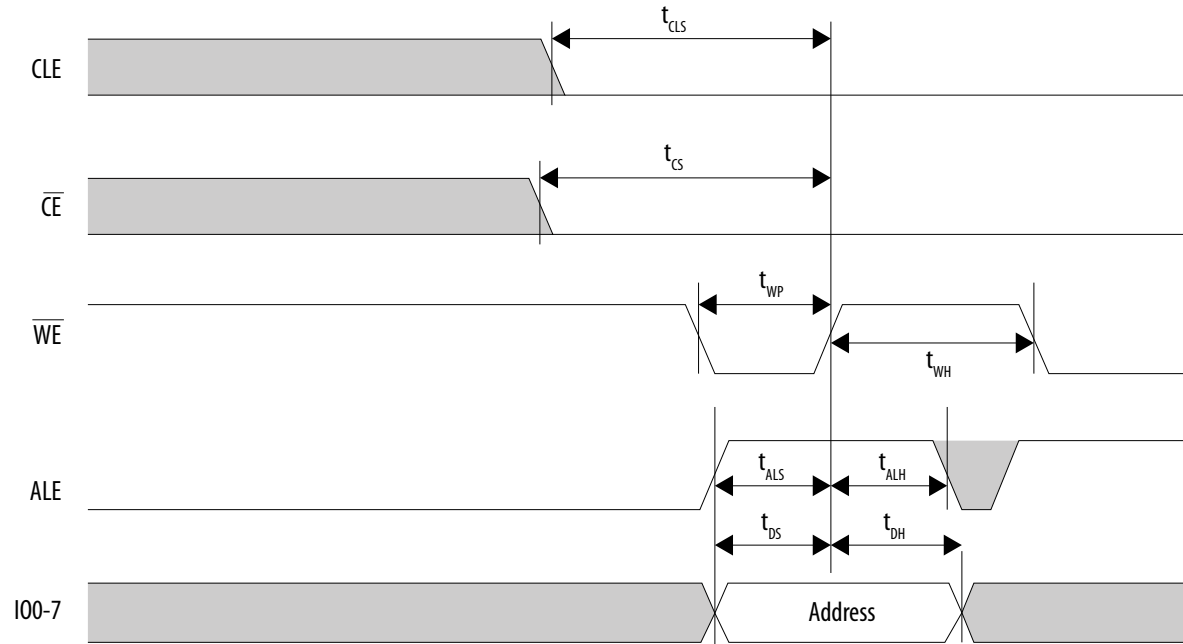


Figure 18. NAND Address Latch Timing Diagram



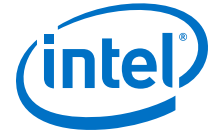


Figure 19. NAND Data Output Cycle Timing Diagram

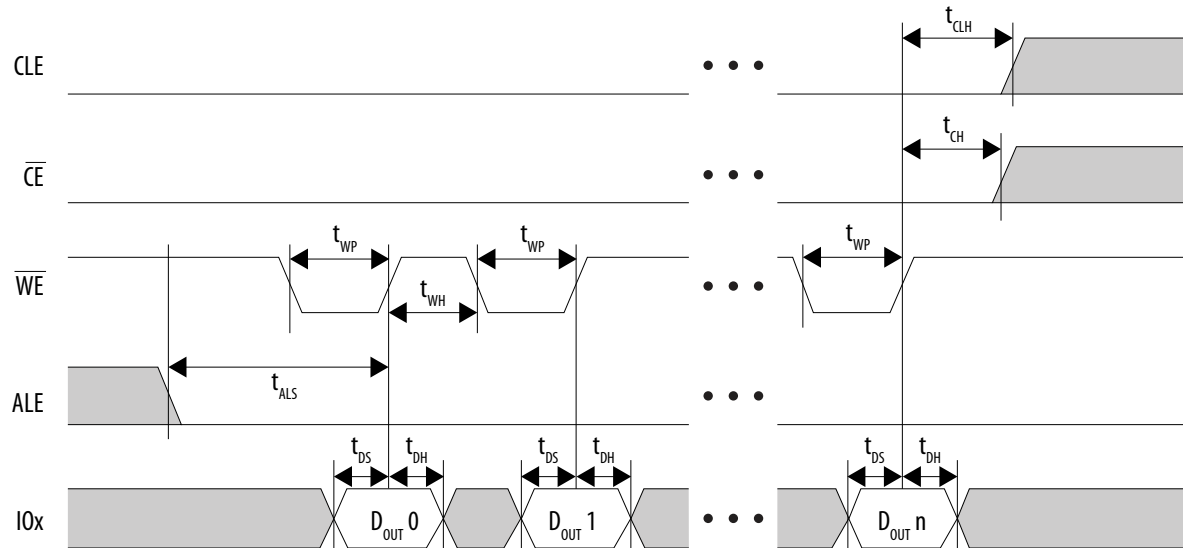


Figure 20. NAND Data Input Cycle Timing Diagram

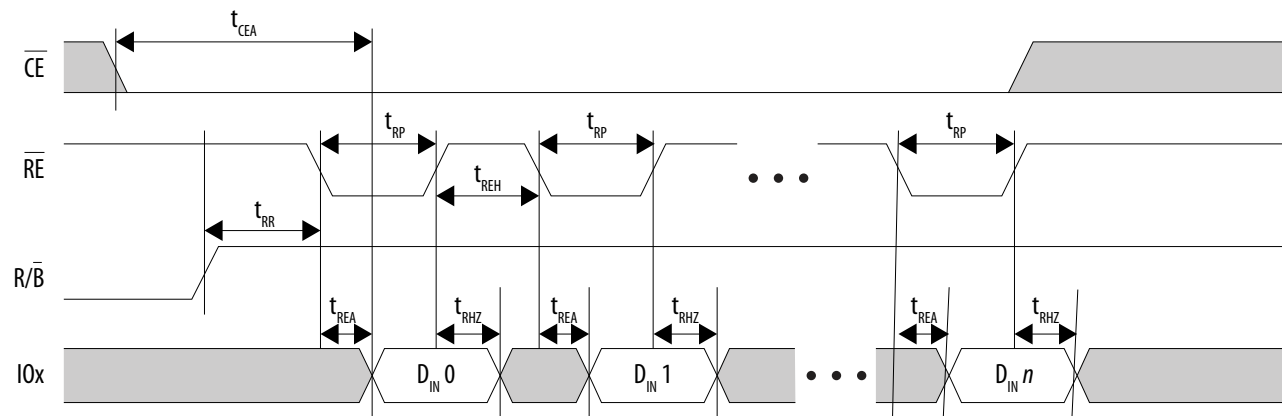
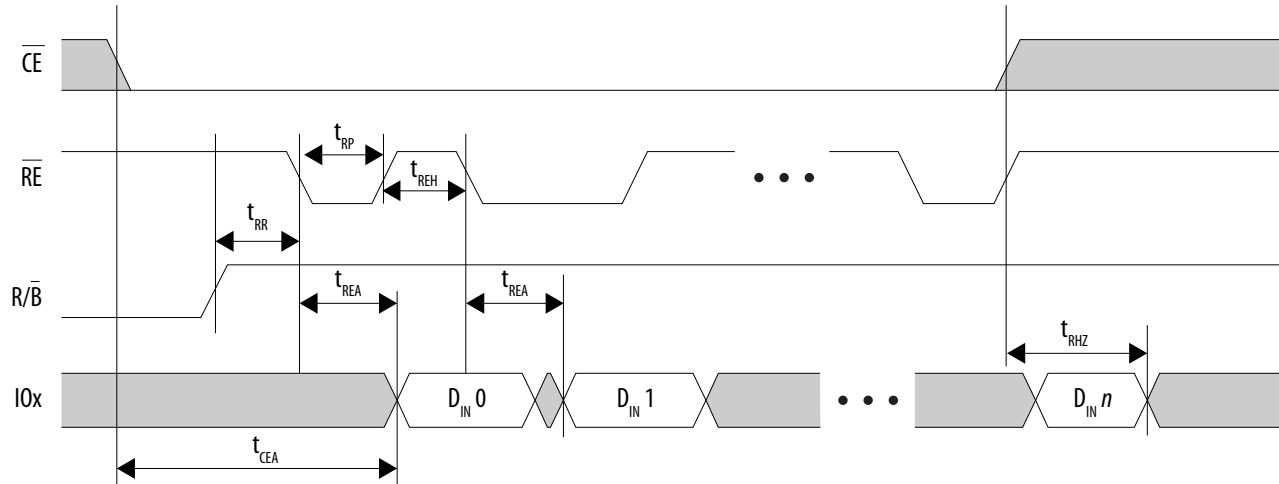




Figure 21. NAND Data Input Timing Diagram for Extended Data Output (EDO) Cycle



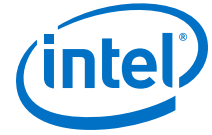


Figure 22. NAND Read Status Timing Diagram

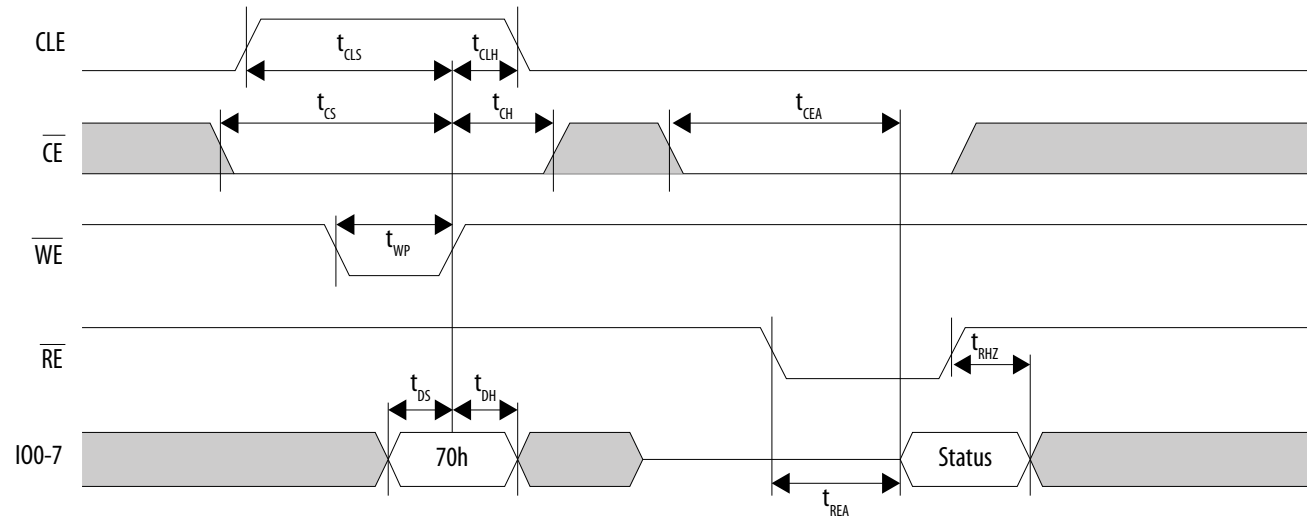
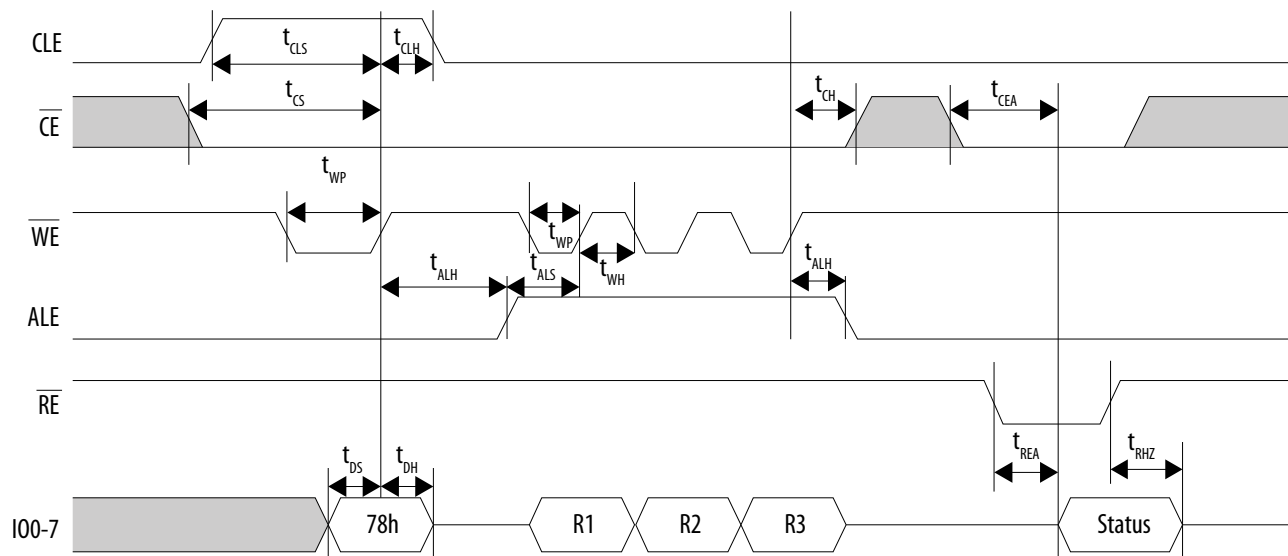


Figure 23. NAND Read Status Enhanced Timing Diagram



### Related Links

#### NAND Flash Controller

Refer to the *NAND Flash Controller* chapter in the *Stratix 10 Hard Processor System Technical Reference Manual* for more information about the NAND flash controller and timing, particularly software-programmable timing.





## HPS Trace Timing Characteristics - Preliminary

**Table 79. Trace Timing Requirements for Intel Stratix 10 Devices**

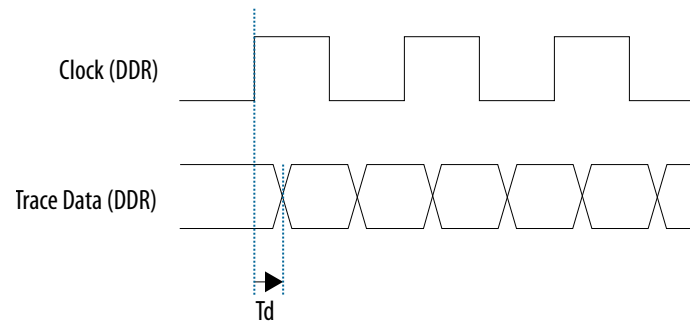
To increase the trace bandwidth, Intel recommends routing the trace interface to the FPGA in the HPS Platform Designer (Standard) component. The FPGA trace interface offers a 64-bit single data rate path that can be converted to double data rate to minimize FPGA I/O usage.

Depending on the trace module that you connect to the HPS trace interface, you may need to include board termination to achieve the maximum sampling speed possible. Refer to your trace module datasheet for termination recommendations.

Most trace modules implement programmable clock and data skew, to improve trace data timing margins. Alternatively, you can change the clock-to-data timing relationship with the HPS programmable I/O delay.

Symbol	Description	Min	Typ	Max	Unit
$T_{clk}$	Trace clock period	6.667	—	—	ns
$T_{clk\_jitter}$	Trace clock output jitter	—	—	2	%
$T_{dutycycle}$	Trace clock maximum duty cycle	45	50	55	%
$T_d$	$T_{clk}$ to D0–D15 output data delay	0	—	1.8	ns

**Figure 24. Trace Timing Diagram**





## **HPS GPIO Interface - Preliminary**

The general-purpose I/O (GPIO) interface has debounce circuitry included to remove signal glitches. The debounce clock frequency ranges from 125 Hz to 32 kHz. The minimum pulse width is 1 debounce clock cycle and the minimum detectable GPIO pulse width is 62.5  $\mu$ s (at 32 kHz). Any pulses shorter than 2 debounce clock cycles are filtered by the GPIO peripheral.

If the external signal is driven into the GPIO for less than one clock cycle, the external signal is filtered. If the external signal is between one and two clock cycles, the external signal may or may not be filtered depending on the phase of the signal. If the external signal is more than two clock cycles, the external signal is not filtered.

### **Related Links**

#### [General-Purpose I/O Interface](#)

For more information about the GPIO interface and timing, refer to the *General-Purpose I/O Interface* chapter in the *Stratix 10 Hard Processor System Technical Reference Manual*



## HPS JTAG Timing Characteristics - Preliminary

**Table 80. HPS JTAG Timing Requirements for Intel Stratix 10 Devices**

Symbol	Description	Min	Typ	Max	Unit
t <sub>JCP</sub>	TCK clock period	41.66	—	—	ns
t <sub>JCH</sub>	TCK clock high time	20	—	—	ns
t <sub>JCL</sub>	TCK clock low time	20	—	—	ns
t <sub>JPSU (TDI)</sub>	TDI JTAG port setup time	5	—	—	ns
t <sub>JPSU (TMS)</sub>	TMS JTAG port setup time	5	—	—	ns
t <sub>JPH</sub>	JTAG port hold time	0	—	—	ns
t <sub>JPCO</sub>	JTAG port clock to output	0	—	8	ns
t <sub>JPZX</sub>	JTAG port high impedance to valid output	—	—	10	ns
t <sub>JPXZ</sub>	JTAG port valid output to high impedance	—	—	10	ns



## HPS Programmable I/O Timing Characteristics - Preliminary

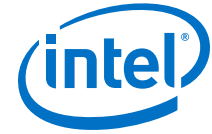
Table 81. Programmable I/O Delay for Intel Stratix 10 Device

Programmable Delay	Description	Min	Typ <sup>(118)</sup>	Max	Unit
0	Delay Step 1	TBD	TBD	TBD	ps
1	Delay Step 2	TBD	TBD	TBD	ps
2	Delay Step 3	TBD	TBD	TBD	ps
3	Delay Step 4	TBD	TBD	TBD	ps
4	Delay Step 5	TBD	TBD	TBD	ps
5	Delay Step 6	TBD	TBD	TBD	ps
6	Delay Step 7	TBD	TBD	TBD	ps
7	Delay Step 8	TBD	TBD	TBD	ps
8	Delay Step 9	TBD	TBD	TBD	ps
9	Delay Step 10	TBD	TBD	TBD	ps
10	Delay Step 11	TBD	TBD	TBD	ps
11	Delay Step 12	TBD	TBD	TBD	ps
12	Delay Step 13	TBD	TBD	TBD	ps
13	Delay Step 14	TBD	TBD	TBD	ps
14	Delay Step 15	TBD	TBD	TBD	ps
15	Delay Step 16	TBD	TBD	TBD	ps

You can program the number of delay steps by adjusting the I/O Delay register (io0\_delay through io47\_delay for I/Os 0 through 47).

---

<sup>(118)</sup> Each delay step is approximately 150 ps.  
)



## Configuration Specifications

### General Configuration Timing Specifications

**Table 82. General Configuration Timing Specifications for Intel Stratix 10 Devices—Preliminary**

Symbol	Description		Requirement			Unit
			Min	Typ	Max	
$t_{CF12ST1}^{(119)}$	nCONFIG high to nSTATUS high		—	10	—	ms
$t_{CF02ST0}$	nCONFIG low to nSTATUS low	Device is empty or not yet configured	—	10	100	ms
		Device configured with Device Security Feature (Zeroization) OFF	—	200	400	ms
		Device configured with Device Security Feature (Zeroization) ON	—	500	1,000	ms
$t_{ST0}$	nSTATUS low pulse during configuration error		0.5	—	1.5	ms
$t_{CD2UM}^{(120)}$	CONF_DONE high to user mode		—	—	2	ms

### POR Specifications

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.

<sup>(119)</sup> The maximum time does not exceed 2× of the typical value.

<sup>(120)</sup> This specification is the initialization time that indicates the time from CONF\_DONE signal goes high to INIT\_DONE signal goes high.



**Table 83. POR Delay Specification for Intel Stratix 10 Devices**

POR Delay	Minimum	Maximum	Unit
AS (Normal mode), AVST ×8, AVST ×16, AVST ×32, NAND, SD/MMC	12	20	ms
AS (Fast mode)	2	6.5	ms

## External Configuration Clock Source Requirements

**Table 84. External Configuration Clock Source (OSC\_CLK\_1) Clock Input Requirements—Preliminary**

Description	External Clock Source	Min	Typ	Max	Unit
Clock input frequency <sup>(121)</sup>	Powered by V <sub>CCIO_SDM</sub>	25/100/125			MHz
Clock input jitter tolerance		—	—	2	%
Clock input duty cycle		45	50	55	%

## JTAG Configuration Timing

**Table 85. JTAG Timing Parameters and Values for Intel Stratix 10 Devices—Preliminary**

Symbol	Description	Requirement		Unit
		Minimum	Maximum	
t <sub>JCP</sub>	TCK clock period	30, 167 <sup>(122)</sup>	—	ns
t <sub>JCH</sub>	TCK clock high time	14	—	ns
t <sub>JCL</sub>	TCK clock low time	14	—	ns
t <sub>JPSU (TDI)</sub>	TDI JTAG port setup time	2	—	ns

*continued...*

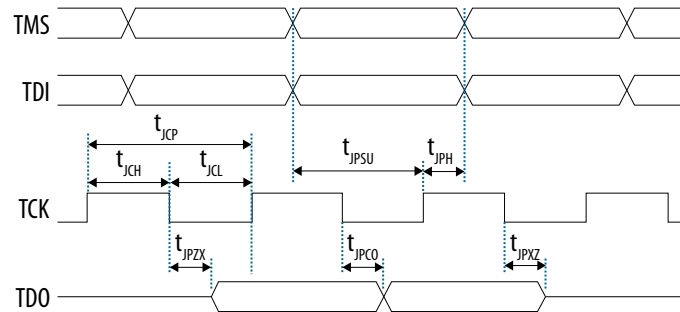
<sup>(121)</sup> The acceptable clock frequencies are 25 MHz, 100 MHz, and 125 MHz only. Other frequencies in the range are not supported.  
)

<sup>(122)</sup> The minimum TCK clock period is 167 ns if V<sub>CCBAT</sub> is within the range 1.2 V – 1.8 V when you perform the volatile key programming.  
)



Symbol	Description	Requirement		Unit
		Minimum	Maximum	
$t_{JPSU}$ (TMS)	TMS JTAG port setup time	3	—	ns
$t_{JPH}$	JTAG port hold time	5	—	ns
$t_{JPCO}$	JTAG port clock to output	—	7	ns
$t_{JPZX}$	JTAG port high impedance to valid output	—	14	ns
$t_{JPXZ}$	JTAG port valid output to high impedance	—	14	ns

Figure 25. JTAG Timing Diagram



## AS Configuration Timing

Table 86. AS Timing Parameters for Intel Stratix 10 Devices—Preliminary

Intel recommends performing trace length matching for nCS0 and AS\_DATA pins to AS\_CLK to minimize the skew. The maximum tolerance for skew between nCS0 and AS\_CLK is less than 200 ps. The tolerance for skew between AS\_DATA and AS\_CLK ranges between 200 ps – 400 ps.

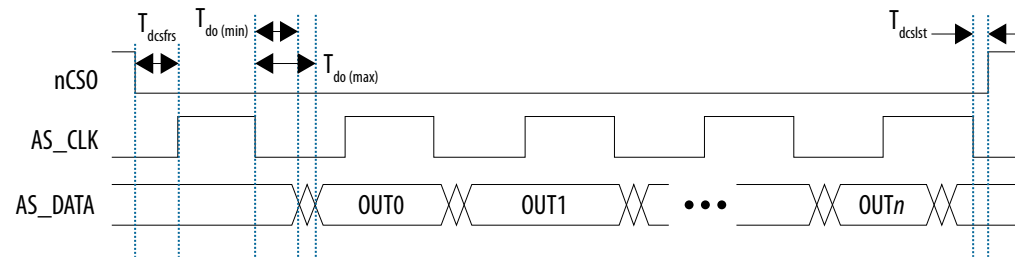
Symbol	Description	Minimum	Typical	Maximum	Unit
$T_{clk}$	AS_CLK clock period	7.52	—	—	ns
$T_{duty}$	AS_CLK duty cycle	45	50	55	%
$T_{dcfrs}$	AS_nCS0[3:0] asserted to first AS_CLK edge	4.21 <sup>(123)</sup>	—	6.05 <sup>(123)</sup>	ns
$T_{dcslst}$	Last AS_CLK edge to AS_nCS0[3:0] deasserted	5.18 <sup>(123)</sup>	—	7.03 <sup>(123)</sup>	ns

*continued...*



Symbol	Description	Minimum	Typical	Maximum	Unit
$T_{do}$	AS_DATA0 output delay	-1	—	1.31	ns
$T_{ext\_delay}^{(124)}$	Total external propagation delay on AS signals	0	—	15	ns
$T_{ext\_skew}$	Skew delay for AS_DATA signals	—	—	2	ns
$T_{dcsb2b}$	Minimum delay of slave select deassertion between two back-to-back transfers	1	—	—	AS_CLK

Figure 26. AS Configuration Serial Output Timing Diagram



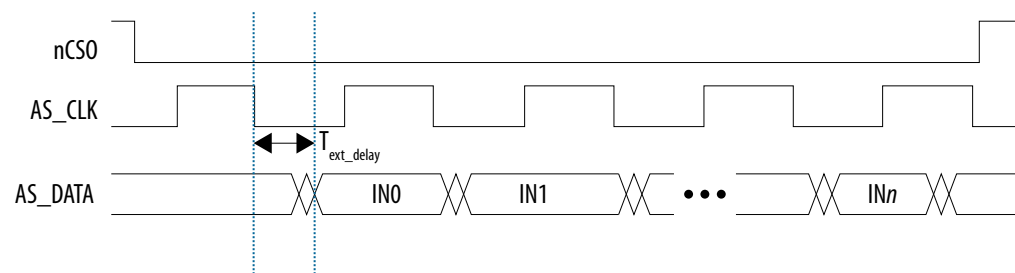
<sup>(123)</sup> AS operating at maximum clock frequency = 133 MHz. The delay is larger when operating at AS clock frequency lower than 133 MHz.

<sup>(124)</sup>  $T_{ext\_delay} = T_{bd\_clk} + T_{co} + T_{bd\_data} + T_{add}$   
 $T_{bd\_clk}$ : Propagation delay for AS\_CLK between FPGA and flash device.  
 $T_{co}$ : Output hold time of flash device.  
 $T_{bd\_data}$ : Propagation delay for AS\_DATA bus between FPGA and flash device.  
 $T_{add}$ : Propagation delay for active/passive components on AS\_DATA interfaces.





Figure 27. AS Configuration Serial Input Timing Diagram



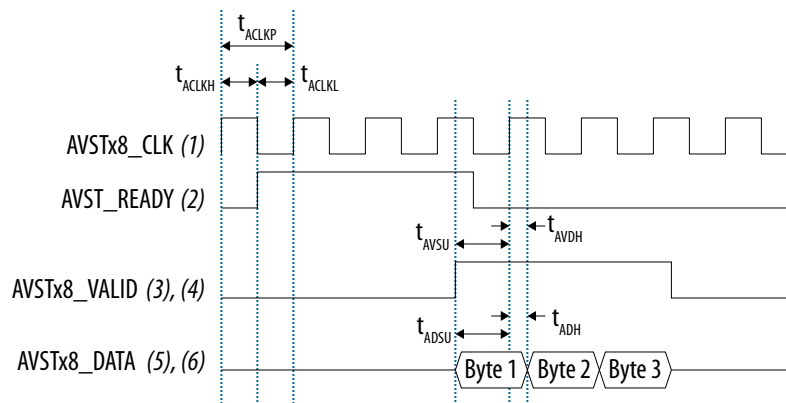
### Avalon-ST Configuration Timing

Table 87. Avalon-ST Timing Parameters for ×8, ×16, and ×32 Configurations in Intel Stratix 10 Devices—Preliminary

Symbol	Description	Minimum	Maximum	Unit
$t_{ACLKH}$	AVST_CLK high time	3.6	—	ns
$t_{ACLKL}$	AVST_CLK low time	3.6	—	ns
$t_{ACLKP}$	AVST_CLK period	8	—	ns
$t_{ADSU}^{(125)}$	AVST_DATA setup time before rising edge of AVST_CLK	5.5	—	ns
$t_{ADH}^{(125)}$	AVST_DATA hold time after rising edge of AVST_CLK	0	—	ns
$t_{AVSU}$	AVST_VALID setup time before rising edge of AVST_CLK	5.5	—	ns
$t_{AVDH}$	AVST_VALID hold time after rising edge of AVST_CLK	0	—	ns

<sup>(125)</sup> Data sampled by the FPGA (sink) at the next rising clock edge.

Figure 28. Avalon-ST Configuration Timing Diagram



Notes:

1. For Avalon-ST x16 and x32, this signal is AVST\_CLK. These clocks must be running throughout the configuration (until CONF\_DONE goes high).
2. AVST\_READY is valid only when nSTATUS is high. AVST\_READY is an asynchronous signal to AVSTx8\_CLK.
3. For Avalon-ST x16 and x32, this signal is AVST\_VALID.
4. The waveforms shows the interface signals with a host which uses ready latency = 2. The AVSTx8\_VALID signal is delayed from AVST\_READY signal by 2 clock cycles.
5. For Avalon-ST x16 and x32, this signal is AVST\_DATA[15:0] and AVST\_DATA[31:0] respectively.
6. Host may send up to 6 more data after AVST\_READY has de-asserted.

## NAND Configuration Timing

Table 88. NAND ONFI 1.0 Mode 0-5 Timing Requirements for Intel Stratix 10 Devices—Preliminary

This table shows Mode 5 timing.

Symbol	Description	Minimum	Maximum	Unit
$t_{WP}$	Write enable pulse width	10	—	ns
$t_{WH}$	Write enable hold time	7	—	ns

*continued...*



Symbol	Description	Minimum	Maximum	Unit
t <sub>RP</sub>	Read enable pulse width	10	—	ns
t <sub>REH</sub>	Read enable hold time	7	—	ns
t <sub>CLS</sub>	Command latch enable to write enable setup time	10	—	ns
t <sub>CLH</sub>	Command latch enable to write enable hold time	5	—	ns
t <sub>CS</sub>	Chip enable to write enable setup time	15	—	ns
t <sub>CH</sub>	Chip enable to write enable hold time	5	—	ns
t <sub>ALS</sub>	Address latch enable to write enable setup time	10	—	ns
t <sub>ALH</sub>	Address latch enable to write enable hold time	5	—	ns
t <sub>DS</sub>	Data to write enable setup time	7	—	ns
t <sub>DH</sub>	Data to write enable hold time	5	—	ns
t <sub>CEA</sub>	Chip enable to data access time	—	100	ns
t <sub>REA</sub>	Read enable to data access time	—	40	ns
t <sub>RHZ</sub>	Read enable to data high impedance	—	200	ns
t <sub>RR</sub>	Ready to read enable low	20	—	ns
t <sub>WB</sub>	Write enable high to R/B low	—	200	ns

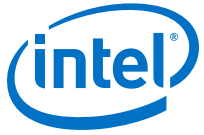
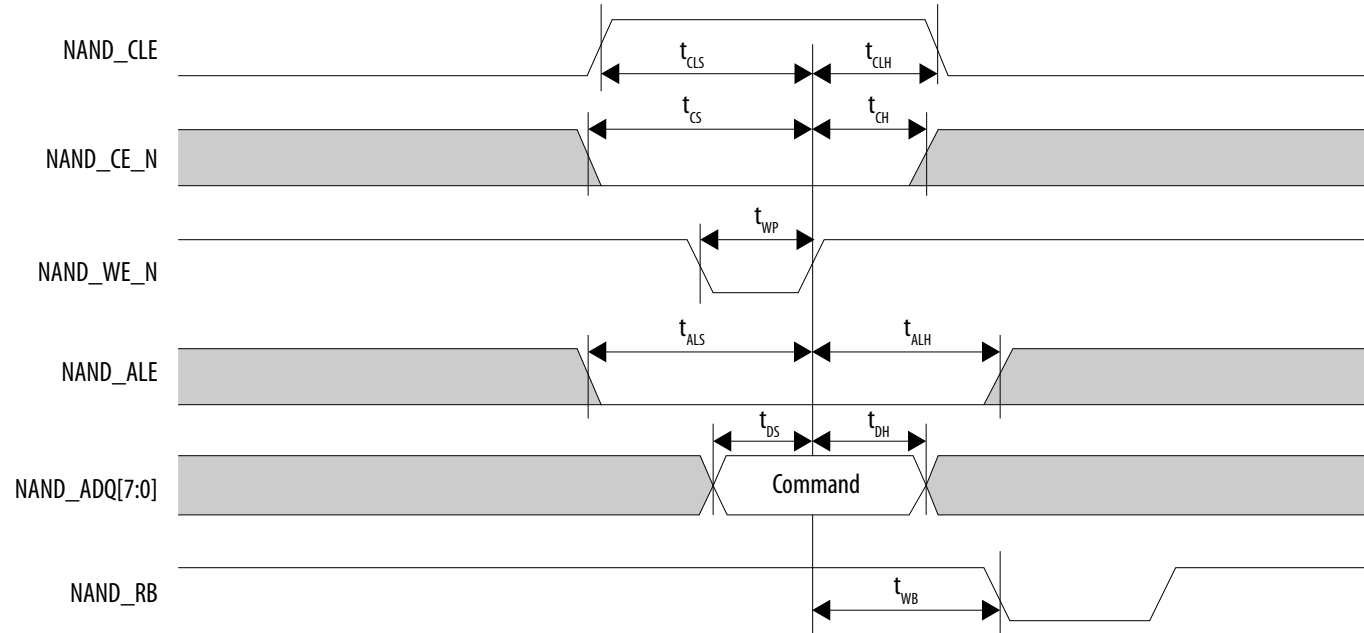


Figure 29. NAND Command Latch Timing Diagram



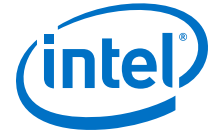


Figure 30. NAND Address Latch Timing Diagram

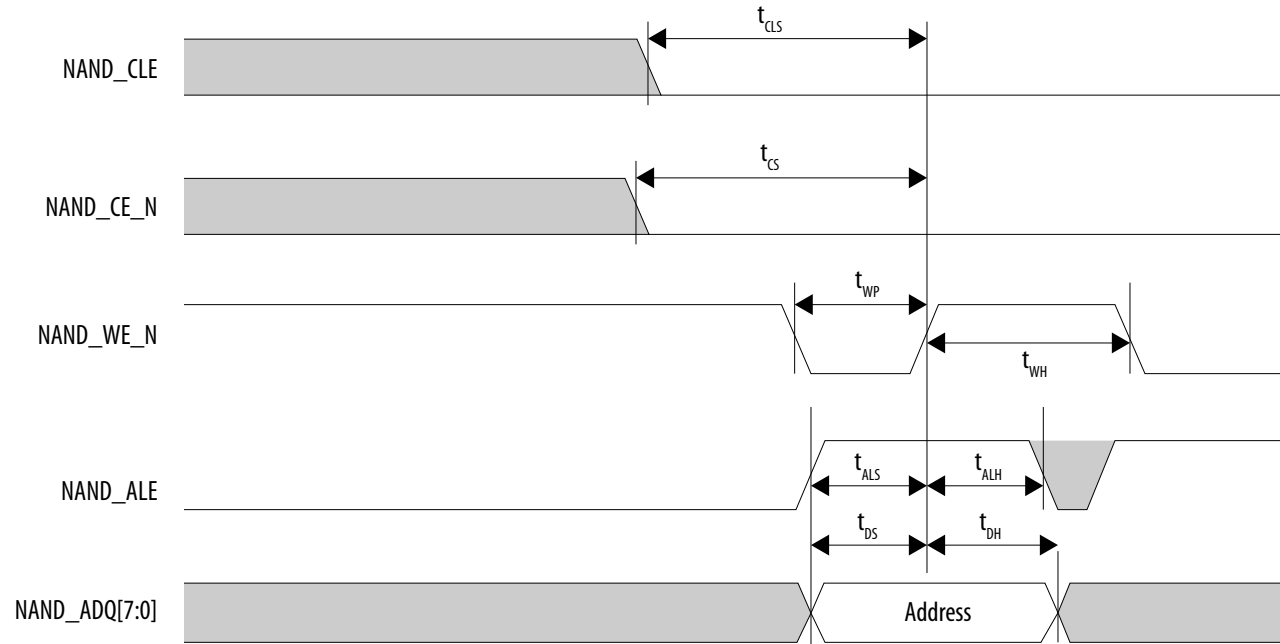


Figure 31. NAND Data Output Cycle Timing Diagram

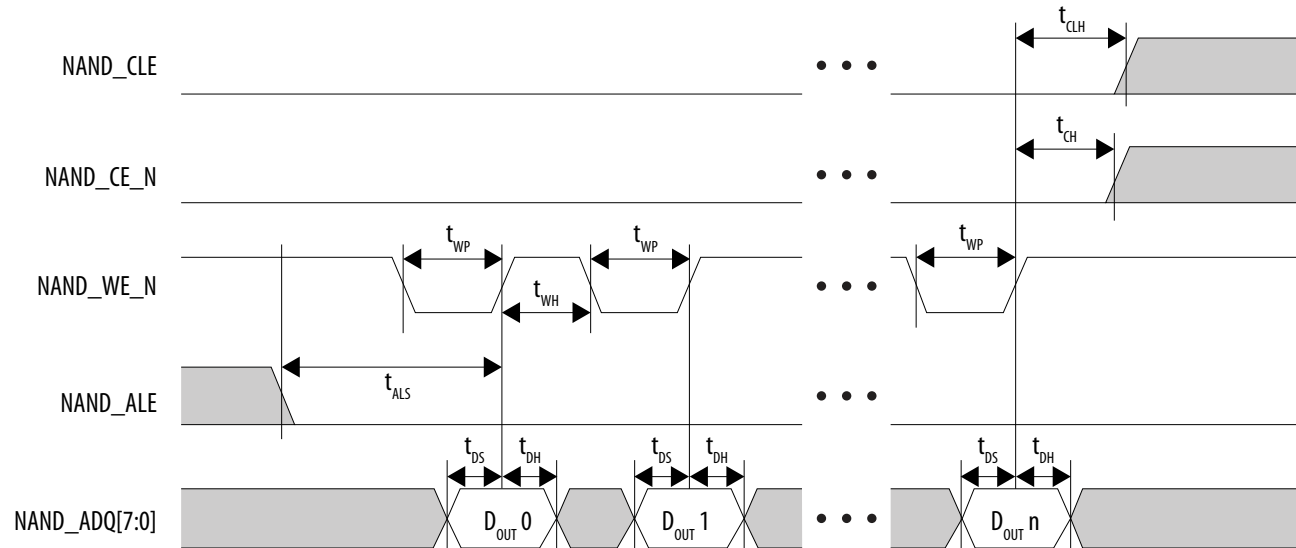


Figure 32. NAND Data Input Cycle Timing Diagram

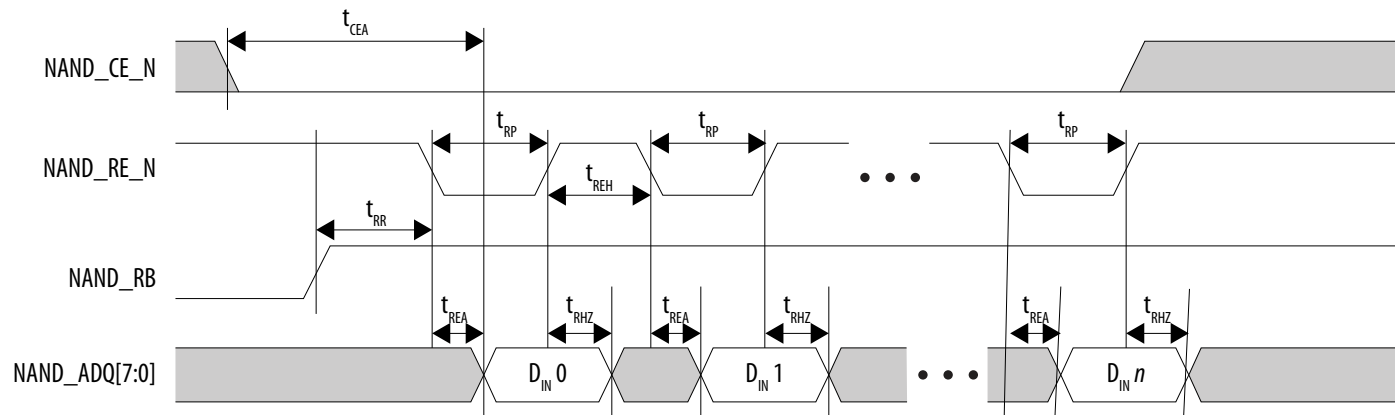




Figure 33. NAND Data Input Timing Diagram for Extended Data Output (EDO) Cycle

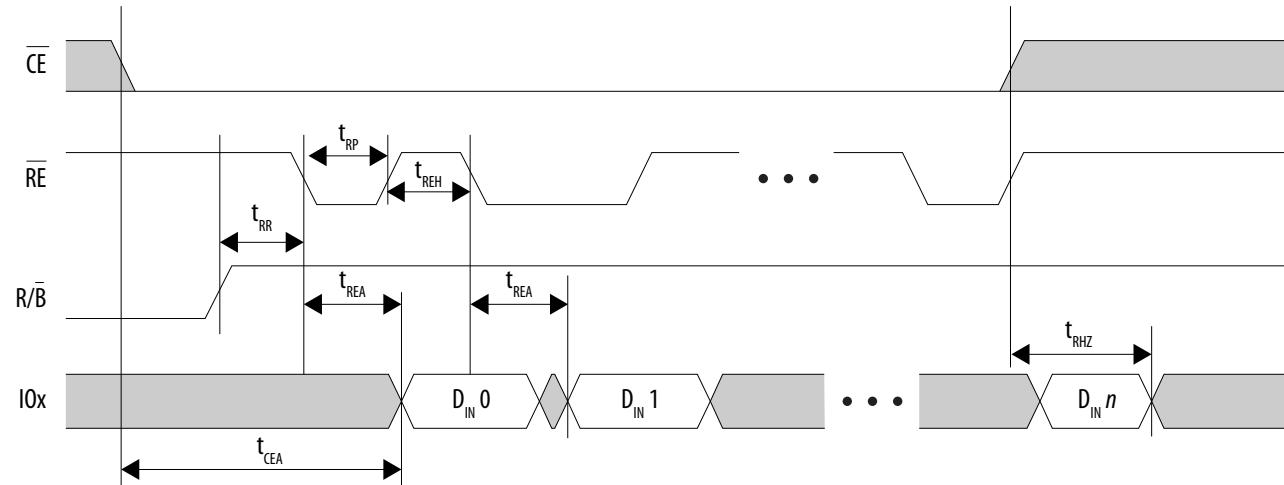




Figure 34. NAND Read Status Timing Diagram

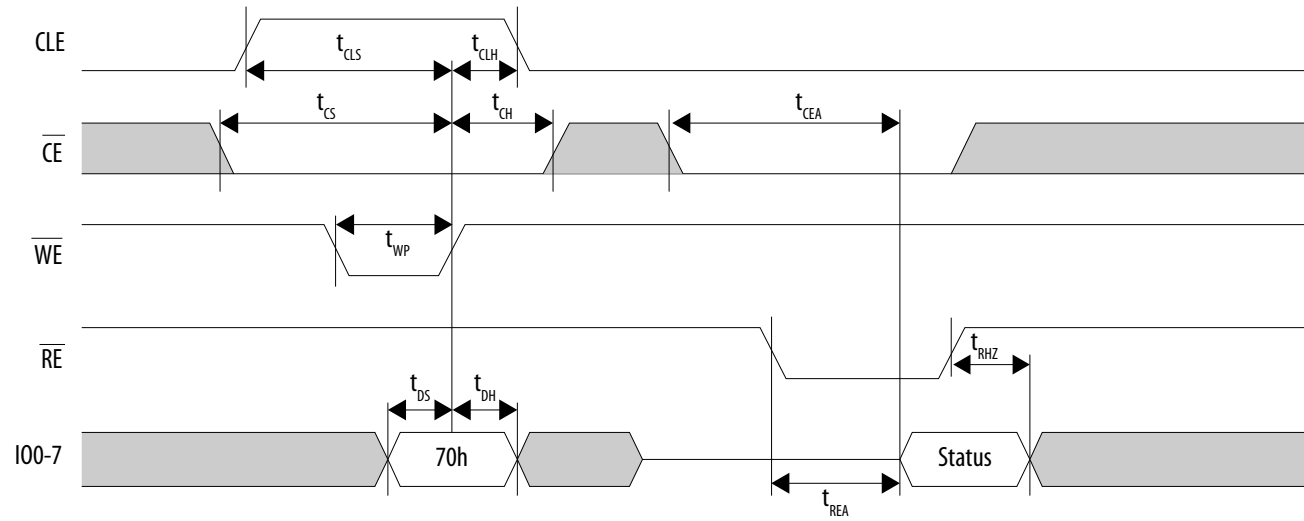
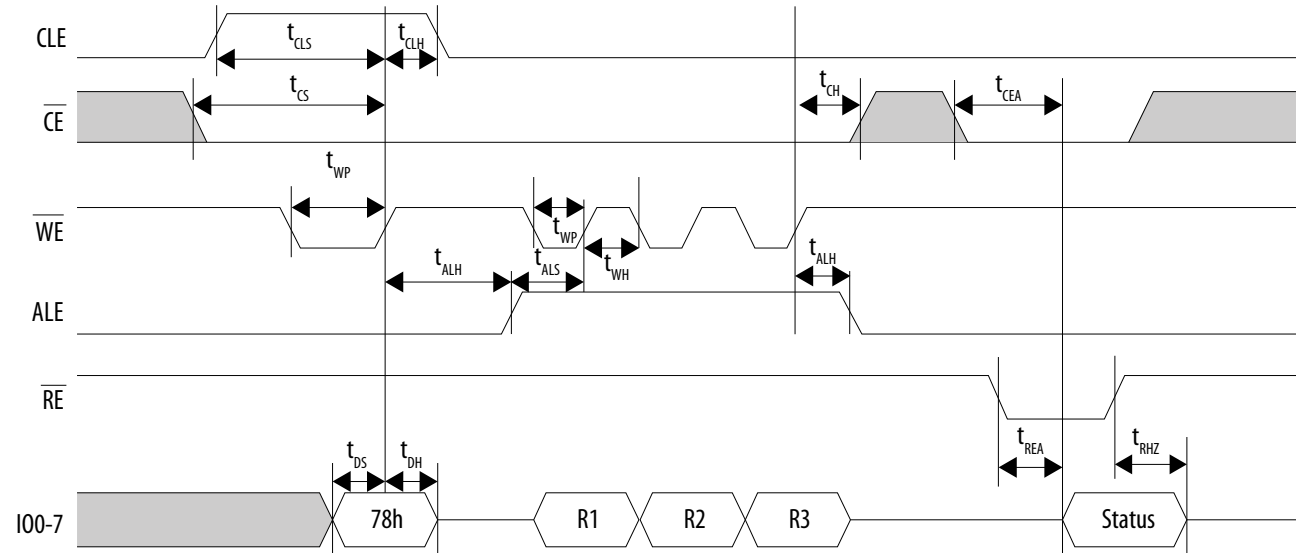






Figure 35. NAND Read Status Enhanced Timing Diagram

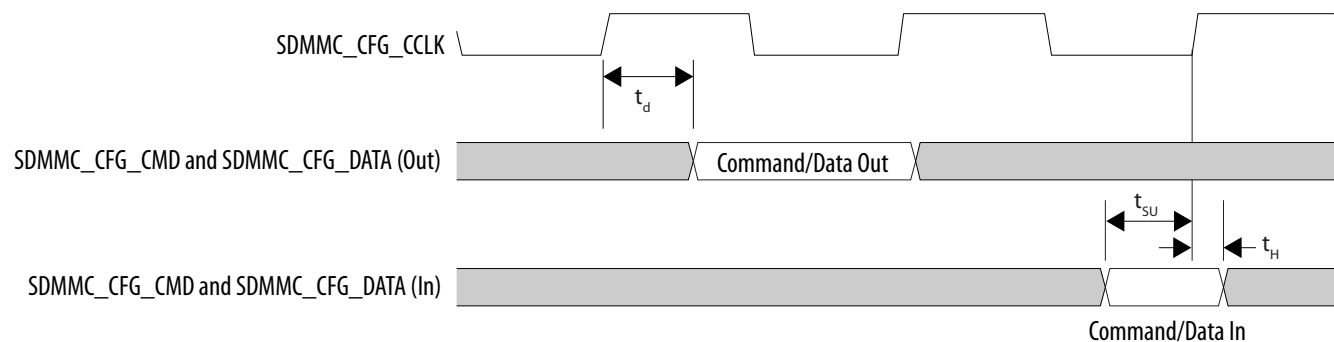


## SD/MMC Configuration Timing

Table 89. SD/MMC Timing Parameters for Intel Stratix 10 Devices—Preliminary

Symbol	Description	Minimum	Typical	Maximum	Unit
$t_{SDCLKP}$	SDMMC_CFG_CCLK clock period (Identification mode)	2,500	—	—	ns
	SDMMC_CFG_CCLK clock period (Standard SD mode)	40	—	—	ns
	SDMMC_CFG_CCLK clock period (High-speed SD mode)	20	—	—	ns
$t_{DUTYCYCLE}$	SDMMC_CFG_CCLK duty cycle	45	50	55	%
$t_d$	SDMMC_CFG_CMD/SDMMC_CFG_DATA output delay	7.3	—	10.1	ns
$t_{SU}$	SDMMC_CFG_CMD/SDMMC_CFG_DATA input setup	4.37	—	—	ns
$t_H$	SDMMC_CFG_CMD/SDMMC_CFG_DATA input hold	-1	—	—	ns

Figure 36. SD/MMC Timing Diagram



## Configuration Bit Stream Sizes

Table 90. Configuration Bit Stream Sizes for Intel Stratix 10 Devices—Preliminary

This table shows the estimated configuration bit stream sizes of the EPCQ-L serial configuration device or external flash size before design compilation. The sizes are for compressed bit stream. The actual sizes may vary based on your design. The actual sizes may be equal or smaller than the bit stream sizes in this table.

Variant	Product Line	Compressed Configuration Bit Stream Size (Mbits)	IOCSR Bit Stream Size (Mbits)
Intel Stratix 10 GX, SX, TX, and MX	GX 400, GX 650, SX 400, SX 650	79	0.140
	GX 850, GX 1100, SX 850, SX 1100, MX 1100	133	0.200
	GX 1650, GX 2100, SX 1650, SX 2100, TX 1650, TX 2100, MX 1650, MX 2100	227	0.297
	GX 2500, GX 2800, SX 2500, SX 2800, TX 2500, TX 2800	336	0.433
	GX 4500, GX 5500, SX 4500, SX 5500	448	0.567

## Minimum Configuration Time Estimation

Hyper Initialization is an option that can be enabled or disabled through the setting in the Intel Quartus Prime software to initialize or reset the Intel Hyperflex™ registers to a known state at device configuration.

Maximum configuration time does not exceed 2× of the minimum configuration time.



**Table 91. Minimum Configuration Time Estimation for Intel Stratix 10 Devices (JTAG and Avalon-ST)—Preliminary**

Variant	Product Line	Minimum Configuration Time (ms) [Hyper Initialization Off/Hyper Initialization On]							
		JTAG		AVST ×8 <sup>(126)</sup>		AVST ×16 <sup>(126)</sup>		AVST ×32 <sup>(126)</sup>	
		170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)
Intel Stratix 10 GX, SX, TX, and MX	GX 400, GX 650, SX 400, SX 650	3000/3100	3000/3100	137/167	91/111	77/108	51/72	60/92	40/61
	GX 850, GX 1100, SX 850, SX 1100, MX 1100	5300/5600	5300/5600	228/284	152/189	123/179	82/119	95/150	63/100
	GX 1650, GX 2100, SX 1650, SX 2100, TX 1650, TX 2100, MX 1650, MX 2100	9000/9500	9000/9500	377/426	251/284	197/248	131/165	107/158	71/105
	GX 2500, GX 2800, SX 2500, SX 2800, TX 2500, TX 2800	13300/14000	13300/14000	551/620	367/413	284/354	189/236	150/221	100/147
	GX 4500, GX 5500, SX 4500, SX 5500	17600/18700	17600/18700	723/831	482/554	371/480	247/320	194/303	129/202

<sup>(126)</sup> ) The minimum configuration time does not include the time incurred from external storage and control logic.



**Table 92. Minimum Configuration Time Estimation for Intel Stratix 10 Devices (AS, NAND, and SD/MMC)—Preliminary**

Variant	Product Line	Minimum Configuration Time (ms) [Hyper Initialization Off/Hyper Initialization On]					
		AS x4		NAND		SD/MMC	
		170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)
Intel Stratix 10 GX, SX, TX, and MX	GX 400, GX 650, SX 400, SX 650	284/315	189/210	495/527	330/351	366/396	244/264
	GX 850, GX 1100, SX 850, SX 1100, MX 1100	450/506	300/337	828/884	552/589	597/653	398/435
	GX 1650, GX 2100, SX 1650, SX 2100, TX 1650, TX 2100, MX 1650, MX 2100	716/767	477/511	1361/1460	907/973	966/1017	644/678
	GX 2500, GX 2800, SX 2500, SX 2800, TX 2500, TX 2800	1029/1100	686/733	1950/2100	1300/1400	1403/1472	935/981
	GX 4500, GX 5500, SX 4500, SX 5500	1338/1449	892/966	2550/2700	1700/1800	1800/1950	1200/1300

## I/O Timing

The Intel Quartus Prime Timing Analyzer provides accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

The I/O Timing specifications will be available in a future release of the *Intel Stratix 10 Device Datasheet*.



## Programmable IOE delay

**Table 93. Programmable IOE Delay for Intel Stratix 10 Devices—Preliminary**

For the exact values for each setting, use the latest version of the Intel Quartus Prime software. The values in the table show the delay of programmable IOE delay chain with maximum offset settings after excluding the intrinsic delay (delay at minimum offset settings).

Programmable IOE delay settings are only applicable for I/O buffers and do not apply for any other delay elements in the Stratix 10 Intel FPGA PHYLite for Parallel Interfaces IP core.

Parameter <sup>(127)</sup>	Maximum Offset	Minimum Offset <sup>(128)</sup>	Fast Model	Slow Model		Unit
			Industrial/Extended	-I2V, -E2V	-I3V, -E3V	
Input Delay Chain (IO_IN_DLY_CHN)	63	0	1.7725	3.0155	3.1475	ns
Output Delay Chain (IO_OUT_DLY_CHN)	15	0	0.4165	0.734	0.7315	ns

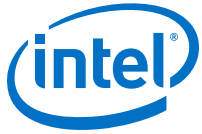
## Glossary

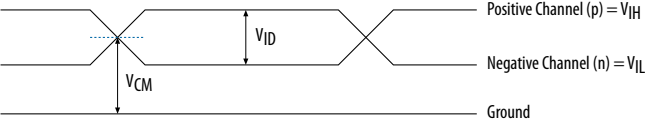

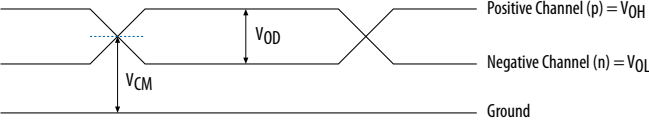
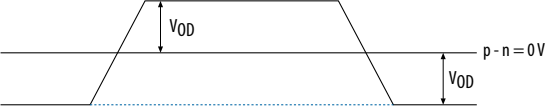
**Table 94. Glossary**

Term	Definition
Differential I/O Standards	Receiver Input Waveforms
<i>continued...</i>	

<sup>(127)</sup> You can set this value in the Intel Quartus Prime software by selecting **Input Delay Chain Setting** or **Output Delay Chain Setting** in the **Assignment Name** column.

<sup>(128)</sup> Minimum offset does not include the intrinsic delay.



Term	Definition
	<p><b>Single-Ended Waveform</b></p>  <p>Positive Channel (p) = <math>V_{IH}</math> Negative Channel (n) = <math>V_{IL}</math> Ground</p> <p><b>Differential Waveform</b></p>  <p>p - n = 0 V</p> <p><b>Transmitter Output Waveforms</b></p> <p><b>Single-Ended Waveform</b></p>  <p>Positive Channel (p) = <math>V_{OH}</math> Negative Channel (n) = <math>V_{OL}</math> Ground</p> <p><b>Differential Waveform</b></p>  <p>p - n = 0 V</p>
$f_{HSCLK}$	I/O PLL input clock frequency.
$f_{HSDR}$	High-speed I/O block—Maximum/minimum LVDS data transfer rate ( $f_{HSDR} = 1/TUI$ ), non-DPA.
$f_{HSDRDPA}$	High-speed I/O block—Maximum/minimum LVDS data transfer rate ( $f_{HSDRDPA} = 1/TUI$ ), DPA.
J	High-speed I/O block—Deserialization factor (width of parallel data bus).
JTAG Timing Specifications	JTAG Timing Specifications:

*continued...*



Term	Definition
$R_L$	Receiver differential input discrete resistor (external to the Intel Stratix 10 device).
Sampling window (SW)	<p>Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown:</p>
Single-ended voltage referenced I/O standard	<p>The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing.</p> <p>Single-Ended Voltage Referenced I/O Standard</p>

*continued...*



Term	Definition
$t_c$	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
$t_{DUTY}$	High-speed I/O block—Duty cycle on high-speed transmitter output clock.
$t_{FALL}$	Signal high-to-low transition time (80–20%).
$t_{INCCJ}$	Cycle-to-cycle jitter tolerance on the PLL clock input.
$t_{OUTPJ\_IO}$	Period jitter on the GPIO driven by a PLL.
$t_{OUTPJ\_DC}$	Period jitter on the dedicated clock output driven by a PLL.
$t_{RISE}$	Signal low-to-high transition time (20–80%).
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = $1/(\text{Receiver Input Clock Frequency Multiplication Factor}) = t_c/w$ ).
$V_{CM(DC)}$	DC Common mode input voltage.
$V_{ICM}$	Input Common mode voltage—The common mode of the differential signal at the receiver.
$V_{ICM(DC)}$	$V_{CM(DC)}$ DC Common mode input voltage.
$V_{ID}$	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
<i>continued...</i>	





Term	Definition
V <sub>IH</sub>	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
V <sub>IH(AC)</sub>	High-level AC input voltage.
V <sub>IH(DC)</sub>	High-level DC input voltage.
V <sub>IL</sub>	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
V <sub>IL(AC)</sub>	Low-level AC input voltage.
V <sub>IL(DC)</sub>	Low-level DC input voltage.
V <sub>OCM</sub>	Output Common mode voltage—The common mode of the differential signal at the transmitter.
V <sub>OD</sub>	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter.
V <sub>SWING</sub>	Differential input voltage.
V <sub>IX</sub>	Input differential cross point voltage.
V <sub>OX</sub>	Output differential cross point voltage.
V <sub>X(AC)</sub>	V <sub>IX</sub> Input differential cross point voltage.
W	High-speed I/O block—Clock Boost Factor.

## Document Revision History for Intel Stratix 10 Device Datasheet

Date	Version	Changes
December 2017	2017.12.15	<ul style="list-style-type: none"> <li>Added the <i>Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L-Tile Devices in a Non-Bonded Configuration</i> table.</li> <li>Added the <i>Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L-Tile Devices in a Bonded Configuration</i> table.</li> <li>Added the <i>Transceiver Power Supply Operating Conditions for Intel Stratix 10 H-Tile Devices in a Non-Bonded Configuration</i> table.</li> <li>Added the <i>Transceiver Power Supply Operating Conditions for Intel Stratix 10 H-Tile Devices in a Bonded Configuration</i> table.</li> <li>Removed the <i>Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L- and H-Tile Devices</i> table.</li> <li>Removed the <i>L-Tile Transmitter and Receiver Data Rate Performance, VCCR_GXB and VCCT_GXB Specifications</i> table.</li> <li>Added the <i>Intel Stratix 10 GX/SX L-Tile Transmitter and Receiver Datarate Performance</i> table.</li> <li>Added the <i>Intel Stratix 10 GX/SX H-Tile Transmitter and Receiver Datarate Performance</i> table.</li> </ul>

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Date	Version	Changes
		<ul style="list-style-type: none"> <li>• Removed the <i>H-Tile Transmitter and Receiver Data Rate Performance, VCCR_GXB and VCCT_GXB Specifications</i> table</li> <li>• Added note to the <i>Maximum</i> column in the <i>Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L- and H-Tile Devices—Preliminary</i> table.</li> <li>• Removed the Minimum differential eye opening at receiver serial input pins specification from the "L-Tile Receiver Specifications" table.</li> <li>• Updated <i>Absolute Maximum Ratings for Intel Stratix 10 Devices</i> table.               <ul style="list-style-type: none"> <li>— Updated <math>T_{STG}</math> minimum specifications from <math>-65^{\circ}\text{C}</math> to <math>-55^{\circ}\text{C}</math>.</li> <li>— Added <math>V_I</math> specifications.</li> </ul> </li> <li>• Added -2 transceiver speed grade, the <math>t_{ARESET}</math>, and the <math>t_{LOCK}</math> specification to the "L-Tile ATX PLL Performance" table.</li> <li>• Added the <math>t_{ARESET}</math> and <math>t_{LOCK}</math> specifications to the "L-Tile Fractional PLL Performance" table.</li> <li>• Added the <math>t_{ARESET}</math> and <math>t_{LOCK}</math> specifications to the "L-Tile CMU PLL Performance" table.</li> <li>• Changed the Channel Span definition in the "L-Tile Transceiver Clock Network Maximum Data Rate Specifications" table.</li> <li>• Removed the VOCM (DC coupled) specification from the "L-Tile Transmitter Specifications" table.</li> <li>• Added the xN clock mode to the "L-Tile Transmitter Channel-to-channel Skew Specifications" table.</li> <li>• Added the xN clock mode to the "H-Tile Transmitter Channel-to-channel Skew Specifications" table.</li> <li>• Added the <math>t_{LOCK}</math> and <math>t_{ARESET}</math> specifications to the "H-Tile ATX PLL Performance" table.</li> <li>• Added the <math>t_{LOCK}</math> and <math>t_{ARESET}</math> specifications to the "H-Tile Fractional PLL Performance" table.</li> <li>• Added the <math>t_{LOCK}</math> and <math>t_{ARESET}</math> specifications to the "H-Tile CMU PLL Performance" table.</li> <li>• Removed the Minimum differential eye opening at receiver serial input pins specification from the "H-Tile Receiver Specifications" table.</li> <li>• Split LVDS I/O and 3 V I/O specifications in <i>Maximum Allowed Overshoot During Transitions for Intel Stratix 10 Devices</i> table into two separate tables. Updated the LVDS I/O specifications.</li> <li>• Added <i>Intel Stratix 10 Devices Overshoot Duration</i> figure and description.</li> <li>• Updated <i>Recommended Operating Conditions for Intel Stratix 10 Devices</i> table.               <ul style="list-style-type: none"> <li>— Updated <math>V_{CCIO\_UIB}</math> specifications.</li> <li>— Updated note to minimum and maximum columns.</li> <li>— Changed the symbol from <math>V_{CCM}</math> to <math>V_{CCM\_WORD}</math>.</li> </ul> </li> <li>• Added specifications for <math>V_{CCIO} = 2.5\text{ V}</math> in the following tables:               <ul style="list-style-type: none"> <li>— <i>Bus Hold Parameters for Intel Stratix 10 Devices</i></li> <li>— <i>Internal Weak Pull-Up Resistor Values for Intel Stratix 10 Devices</i></li> </ul> </li> <li>• Updated specifications in <i>OCT Calibration Accuracy Specifications for Intel Stratix 10 Devices</i> table.</li> <li>• Updated specifications in <i>OCT Without Calibration Resistance Tolerance Specifications for Intel Stratix 10 Devices</i> table.               <ul style="list-style-type: none"> <li>— Added specifications for <math>V_{CCIO} = 3.0, 2.5</math></li> <li>— Updated specifications for <math>V_{CCIO} = 1.8, 1.5, 1.2</math></li> </ul> </li> <li>• Added the following specifications in <i>Single-Ended I/O Standards Specifications for Intel Stratix 10 Devices</i> table.               <ul style="list-style-type: none"> <li>— 2.5 V I/O standard</li> <li>— Schmitt trigger input</li> </ul> </li> </ul>

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Date	Version	Changes
		<ul style="list-style-type: none"> <li>• Updated SSTL-125 and SSTL-135 I/O standards in <i>Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel Stratix 10 Devices</i> table.</li> <li>• Added specifications for SSTL-12 I/O standard in the following tables: <ul style="list-style-type: none"> <li>– <i>Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel Stratix 10 Devices</i></li> <li>– <i>Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Intel Stratix 10 Devices</i></li> <li>– <i>Differential SSTL I/O Standards Specifications for Intel Stratix 10 Devices</i></li> </ul> </li> <li>• Updated the <i>Fractional PLL Specifications for Intel Stratix 10 Devices</i> table. <ul style="list-style-type: none"> <li>– Updated <math>t_{PLL\_PSERR}</math> specifications.</li> <li>– Updated <math>t_{LOCK}</math> description.</li> <li>– Removed <math>t_{ARESET}</math> specifications.</li> </ul> </li> <li>• Updated <math>t_{OUTDUTY}</math> in the <i>I/O PLL Specifications for Intel Stratix 10 Devices</i> table.</li> <li>• Updated <i>Internal Temperature Sensing Diode Specifications for Intel Stratix 10 Devices</i> table. <ul style="list-style-type: none"> <li>– Added note for temperature range.</li> <li>– Updated conversion time from &lt; 5 ms to &lt; 1 ms.</li> <li>– Removed "Resolution" and "Minimum Resolution with no Missing Codes" specifications.</li> </ul> </li> <li>• Updated <i>High-Speed I/O Specifications for Intel Stratix 10 Devices</i> table. <ul style="list-style-type: none"> <li>– Updated Transmitter—TCCS specifications from 150 ps to 330 ps.</li> <li>– Updated Sampling Window specifications from 300 ps to 330 ps.</li> <li>– Updated SERDES factor <math>J = 3</math> maximum data rate for transmitter and receiver.</li> </ul> </li> <li>• Updated from 0.35 to 0.28 for the following: <ul style="list-style-type: none"> <li>– <i>LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Equal to 1.6 Gbps</i></li> <li>– <i>LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.6 Gbps</i></li> </ul> </li> <li>• Updated DLL reference clock input specifications in <i>DLL Frequency Range Specifications for Intel Stratix 10 Devices</i> table.</li> <li>• Updated <math>T_{do}</math> minimum specification from 0 ns to -1 ns in <i>AS Timing Parameters for Intel Stratix 10 Devices</i> table.</li> <li>• Updated minimum specifications for <math>t_H</math> from 0 ns to -1 ns in <i>SD/MMC Timing Parameters for Intel Stratix 10 Devices</i> table.</li> </ul>

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Date	Version	Changes
		<ul style="list-style-type: none"> <li>• Updated <i>Configuration Bit Stream Sizes for Intel Stratix 10 Devices</i> table.               <ul style="list-style-type: none"> <li>– Added IOCSR bit stream sizes.</li> <li>– Added specifications for Intel Stratix 10 TX and MX devices.</li> </ul> </li> <li>• Updated <i>Minimum Configuration Time Estimation for Intel Stratix 10 Devices</i> tables.               <ul style="list-style-type: none"> <li>– Added note to AVST ×8, AVST ×16, and AVST ×32.</li> <li>– Updated specifications for NAND.</li> <li>– Added specifications for Intel Stratix 10 TX and MX devices.</li> </ul> </li> <li>• Added the following tables:               <ul style="list-style-type: none"> <li>– <i>External Temperature Sensing Diode Specifications for Intel Stratix 10 Devices</i></li> <li>– <i>General Configuration Timing Specifications for Intel Stratix 10 Devices</i> <ul style="list-style-type: none"> <li>• Moved <math>t_{ST0}</math> specifications from <i>Avalon-ST Timing Parameters for ×8, ×16, and ×32 Configurations in Intel Stratix 10 Devices</i> table.</li> <li>• Moved the specifications from <i>Initialization Time for Intel Stratix 10 Devices</i> table.</li> </ul> </li> <li>– <i>Programmable IOE Delay for Intel Stratix 10 Devices</i></li> </ul> </li> </ul>
August 2017	2017.08.04	<ul style="list-style-type: none"> <li>• Clarified DLL operating frequency range in "DLL Range Specifications"</li> <li>• Clarified reference clock specifications in "HPS SPI Timing Characteristics"</li> </ul>
May 2017	2017.05.08	<ul style="list-style-type: none"> <li>• Updated description for <math>V_{CCERAM}</math> in Absolute Maximum Ratings for Intel Stratix 10 Devices table.</li> <li>• Added Maximum Allowed Overshoot During Transitions for Intel Stratix 10 Devices table.</li> <li>• Updated Recommended Operating Conditions for Intel Stratix 10 Devices table.               <ul style="list-style-type: none"> <li>– Updated <math>V_{CC}</math>, <math>V_{CCIO}</math>, and <math>V_{CCBAT}</math> specifications.</li> <li>– Updated symbol from <math>V_{CCPFUSE\_SDM}</math> to <math>V_{CCFUSEWR\_SDM}</math>.</li> <li>– Updated description for <math>V_{CCERAM}</math> and <math>V_{CCIO\_UIB}</math>.</li> <li>– Added <math>V_{CCM}</math> specifications.</li> <li>– Added footnotes to <math>t_{RAMP}</math> and V suffix speed grades.</li> </ul> </li> <li>• Removed table: Temperature Compensation for SmartVID for Intel Stratix 10 Devices. Moved the table to the Intel Stratix 10 Power Management User Guide.</li> <li>• Updated the note in the "Transceiver Power Supply Operating Conditions" section.</li> <li>• Updated HPS Power Supply Operating Conditions for Intel Stratix 10 Devices table.               <ul style="list-style-type: none"> <li>– Updated <math>V_{CCL\_HPS}</math> and <math>V_{CCPLLDIG\_HPS}</math> specifications.</li> <li>– Added footnote for SmartVID.</li> </ul> </li> <li>• Updated footnote to <math>I_{OL}</math> and <math>I_{OH}</math> in Single-Ended I/O Standards Specifications for Intel Stratix 10 Devices table.</li> <li>• Updated Differential I/O Standards Specifications for Intel Stratix 10 Devices table.               <ul style="list-style-type: none"> <li>– Changed <math>D_{MAX}</math> to data rate.</li> <li>– Added a note to <math>V_{OD}</math>.</li> </ul> </li> <li>• Updated <math>t_{OUTPJ\_DC}</math> and <math>t_{OUTCCJ\_DC}</math> specifications in I/O PLL Specifications for Intel Stratix 10 Devices.</li> <li>• Changed the units of measure for the minimum frequency in the "L-Tile CMU PLL Performance" table.</li> </ul>

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Date	Version	Changes
		<ul style="list-style-type: none"> <li>• Changed the units of measure for the minimum frequency in the "H-Tile CMU PLL Performance" table.</li> <li>• Updated <math>t_{INCC}</math> specification for <math>F_{REF} &lt; 100</math> MHz in the following tables: <ul style="list-style-type: none"> <li>— Fractional PLL Specifications for Intel Stratix 10 Devices</li> <li>— I/O PLL Specifications for Intel Stratix 10 Devices</li> </ul> </li> <li>• Added footnote to the following modes in DSP Block Performance Specifications for Intel Stratix 10 Devices table: <ul style="list-style-type: none"> <li>— Fixed-point <math>27 \times 27</math> multiplication mode</li> <li>— Fixed-point <math>18 \times 18</math> multiplier adder mode</li> <li>— Fixed-point <math>18 \times 18</math> multiplier adder summed with 36-bit input mode</li> </ul> </li> <li>• Updated soft CDR mode specifications in High-Speed I/O Specifications for Intel Stratix 10 Devices table.</li> <li>• Added POR specifications.</li> <li>• Updated <math>T_{do}</math> maximum specification in AS Timing Parameters for Intel Stratix 10 Devices table.</li> <li>• Updated notes in Avalon-ST Configuration Timing Diagram.</li> <li>• Added description in NAND ONFI 1.0 Mode 0-5 Timing Requirements for Intel Stratix 10 Devices table.</li> <li>• Updated <math>t_{SU}</math>, <math>t_H</math>, and <math>t_d</math> specifications in SD/MMC Timing Parameters for Intel Stratix 10 Devices table.</li> <li>• Updated table title from "Initialization Clock Source Option and the Maximum Frequency for Intel Stratix 10 Devices" to "Initialization Time for Intel Stratix 10 Devices".</li> <li>• Updated description in Configuration Bit Stream Sizes for Intel Stratix 10 Devices to mention that the actual sizes may be equal or smaller than the bit stream sizes in this table.</li> <li>• Updated description in Minimum Configuration Time Estimation section.</li> <li>• Removed AS <math>\times 1</math> specifications in Minimum Configuration Time Estimation for Intel Stratix 10 Devices (AS, NAND, and SD/MMC) table.</li> <li>• Added Glossary.</li> <li>• Removed PowerPlay text from tool name.</li> </ul>
February 2017	2017.02.17	<p>Made the following changes:</p> <ul style="list-style-type: none"> <li>• Added the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX E-Tile Devices" table.</li> <li>• Added the "E-Tile Transceiver Performance Specifications" section.</li> <li>• Added the "Transceiver Performance for Intel Stratix 10 E-Tile Devices" section.</li> <li>• Added the "Transceiver Reference Clock Specifications" section.</li> <li>• Added the "Transmitter Specifications for Intel Stratix 10 E-Tile Devices" section.</li> <li>• Added the "Receiver Specifications for Intel Stratix 10 E-Tile Devices" section.</li> <li>• Updated the "AS Timing Parameters for Intel Stratix 10 Devices" table. <ul style="list-style-type: none"> <li>— Updated <math>T_{dcfrs}</math> and <math>T_{dcslst}</math>.</li> <li>— Added <math>T_{ext\_delay}</math> and <math>T_{ext\_skew}</math>.</li> <li>— Removed <math>T_{SU}</math> and <math>T_H</math>.</li> </ul> </li> <li>• Updated AS Configuration Serial Input Timing Diagram.</li> </ul>
December 2016	2016.12.09	<p>Made the following changes:</p>

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Date	Version	Changes
		<ul style="list-style-type: none"><li>• Changed the max <math>t_{LTR}</math> value and unit of measure in the "L-Tile Receiver Specifications" table.</li><li>• Made the following changes to the "Transceiver Clocks Specifications for Stratix 10 GX/SX L-Tile Devices" table:<ul style="list-style-type: none"><li>— Changed the value of the <code>reconfig_clk</code> signal</li><li>— Added a new footnote to the GX channel</li><li>— Changed the minimum values for the GXT channel</li></ul></li><li>• Changed the max <math>t_{LTR}</math> value and unit of measure in the "H-Tile Receiver Specifications" table.</li><li>• Removed the QPI footnote from the "H-Tile Transmitter Specifications" table.</li><li>• Changed the value of the <code>reconfig_clk</code> signal in the "Transceiver Clocks Specifications for Stratix 10 GX/SX H-Tile Devices" table.</li><li>• Changed the minimum value of <math>f_{INPFD}</math> in the "Fractional PLL Specifications for Stratix 10 Devices" table.</li></ul>
October 2016	2016.10.31	Initial release.