Load Switch with Level-Shift

PRODUCT SUMMARY		
V_{IN} (V_{DS2}) (V)	$R_{DS(on)}$ (Ω) Max.	I_D (A)
1.8 to 12	0.200 at V_{IN} = 4.5 V	1.1
	0.300 at V_{IN} = 2.5 V	0.9
	0.508 at V_{IN} = 1.8 V	0.7

DESCRIPTION

The Si1865DDL includes a p- and n-channel MOSFET in a single SC70-6 package. The low on-resistance p-channel TrenchFET is tailored for use as a load switch. The n-channel, with an external resistor, can be used as a level-shift to drive the p-channel load-switch. The n-channel MOSFET has internal ESD protection and can be driven by logic signals as low as 1.5 V. The Si1865DDL operates on supply lines from 1.8 V to 12 V, and can drive loads up to 1.1 A.

FEATURES

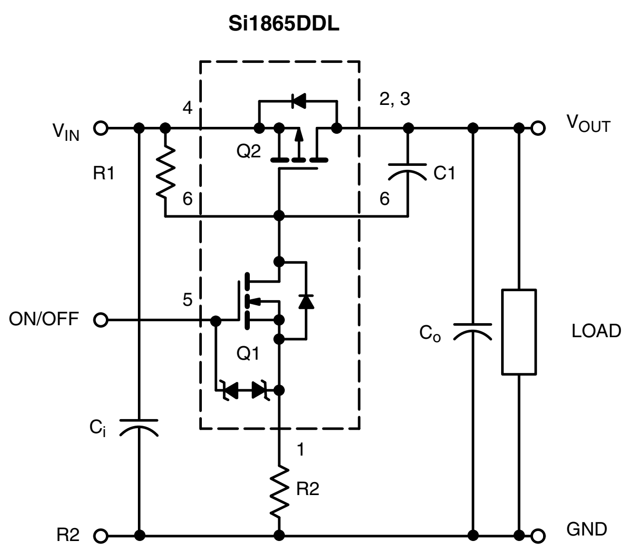
- Low $R_{DS(on)}$ TrenchFET®
- 1.8 V to 12 V Input
- 1.5 V to 8 V Logic Level Control
- Low Profile, Small Footprint SC70-6 Package
- 2000 V ESD Protection On Input Switch, $V_{ON/OFF}$
- Adjustable Slew-Rate
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

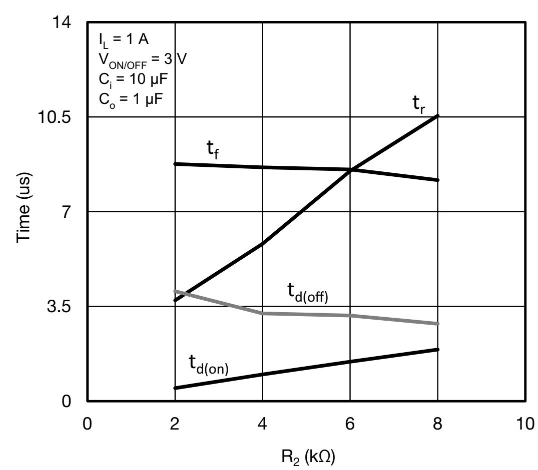
Pb-free
RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load Switch with Level-Shift
- Slew-rate Control
- Portable/Consumer Devices

APPLICATION CIRCUITS





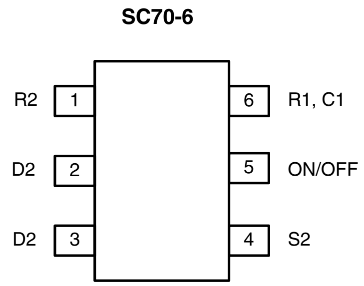
Switching Variation R2 at V_{IN} = 2.5 V, R1 = 20 kΩ

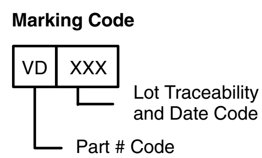
COMPONENTS		
R1	Pull-Up Resistor	Typical 10 kΩ to 1 MΩ[a]
R2	Optional Slew-Rate Control	Typical 0 to 100 kΩ[a]
C1	Optional Slew-Rate Control	Typical 1000 pF

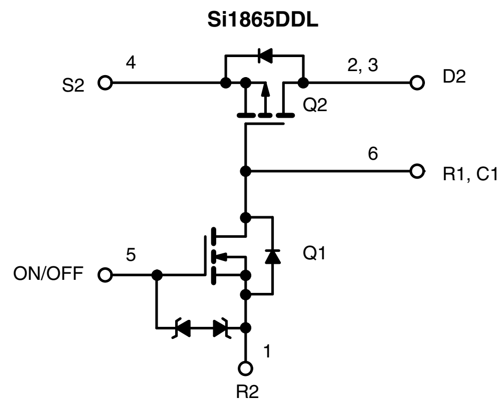
Note:
a. Minimum R1 value should be at least 10 x R2 to ensure Q1 turn-on.

The Si1865DDL is ideally suited for high-side load switching in portable applications. The integrated n-channel level-shift device saves space by reducing external components. The slew rate is set externally so that rise-times can be tailored to different load types.

FUNCTIONAL BLOCK DIAGRAM







Ordering Information: Si1865DDL-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Input Voltage		$V_{IN}(V_{DS2})$	12	V
On/Off Voltage		$V_{ON/OFF}$	8	
Load Current	Continuous[a, b]	I_L	± 1.1	A
	Pulsed[b, c]		± 5	
Continuous Intrinsic Diode Conduction[a]		I_S	- 0.3	
Maximum Power Dissipation[a]		P_D	0.357	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
ESD Rating, MIL-STD-883D Human Body Model (100 pF, 1500 Ω)		ESD	2	kV

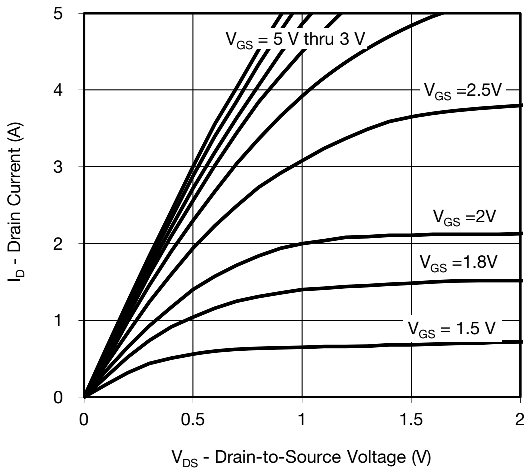
THERMAL RESISTANCE RATINGS				
Parameter	**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient (continuous current)[a]	R_{thJA}	290	350	°C/W
Maximum Junction-to-Foot (Q2)	R_{thJF}	250	300	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Off Characteristics						
Reverse Leakage Current	I_{FL}	V_{IN} = 12 V, $V_{ON/OFF}$ = 0 V			1	µA
Diode Forward Voltage	V_{SD}	I_S = - 0.8 A		- 0.84	- 1.2	V
On Characteristics						
Input Voltage Range	V_{IN}		1.8		12	V
On-Resistance (P-Channel)	$R_{DS(on)}$	$V_{ON/OFF}$ = 1.5 V, V_{IN} = 4.5 V, I_D = 1.1 A		0.165	0.200	Ω
		$V_{ON/OFF}$ = 1.5 V, V_{IN} = 2.5 V, I_D = 0.9 A		0.250	0.300	
		$V_{ON/OFF}$ = 1.5 V, V_{IN} = 1.8 V, I_D = 0.2 A		0.376	0.508	
On-State (P-Channel) Drain-Current	$I_{D(on)}$	$V_{IN-OUT} \leq 0.2$ V, V_{IN} = 5 V, $V_{ON/OFF}$ = 1.5 V	1			A
		$V_{IN-OUT} \leq 0.3$ V, V_{IN} = 3 V, $V_{ON/OFF}$ = 1.5 V	1			

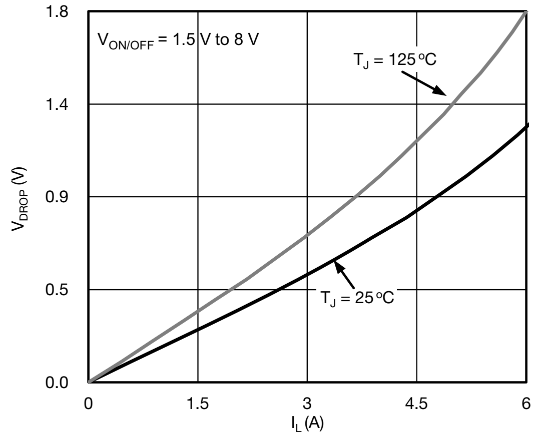
Notes:
a. Surface mounted on FR4 board.
b. V_{IN} = 12 V, $V_{ON/OFF}$ = 8 V, T_A = 25 °C.
c. Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2 %.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

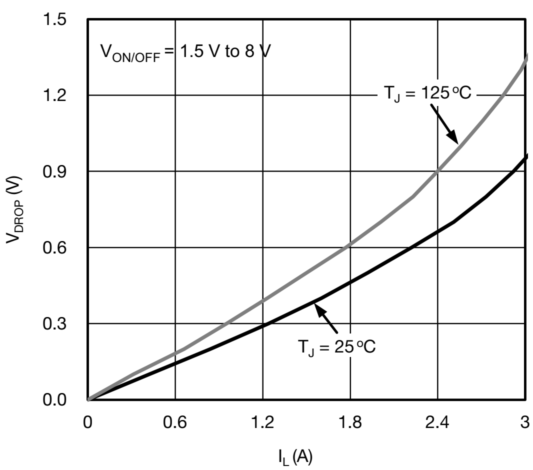
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



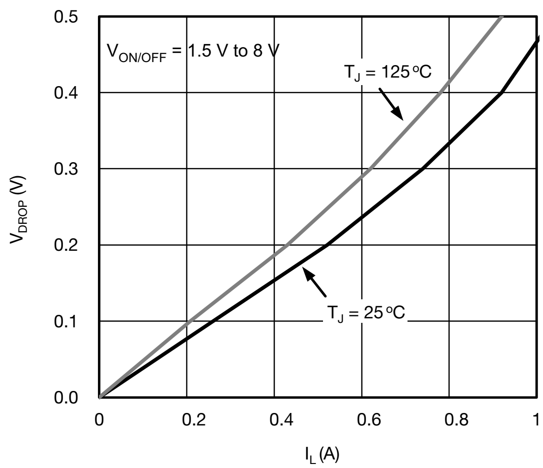
Output Characteristics



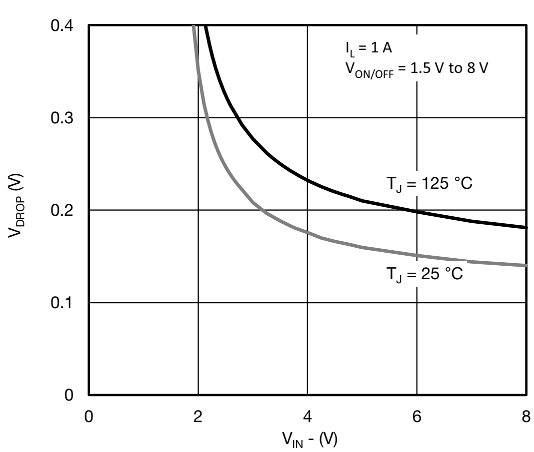
V_{DROP} vs. I_L at V_{IN} = 4.5 V



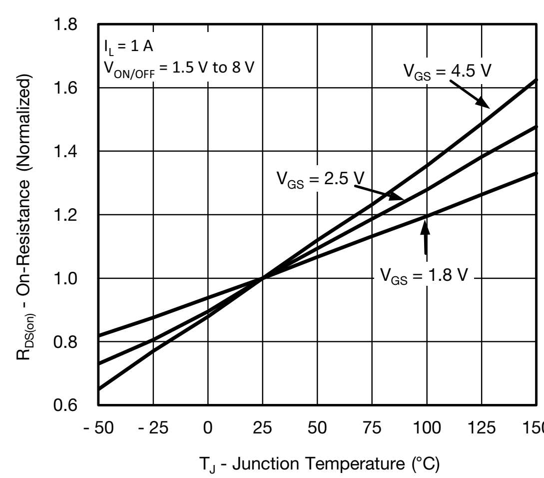
V_{DROP} vs. I_L at V_{IN} = 2.5 V



V_{DROP} vs. I_L at V_{IN} = 1.8 V

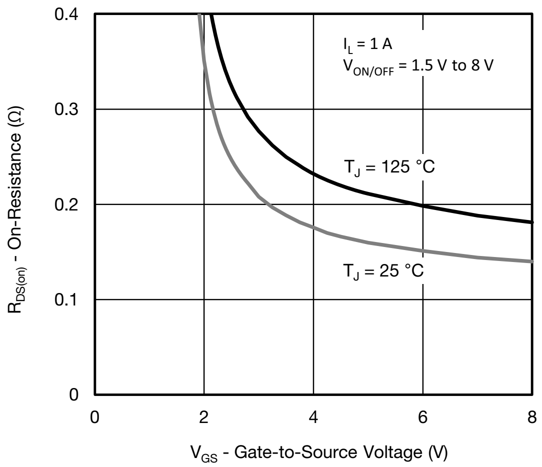


V_{DROP} vs. V_{IN} at I_L = 1 A

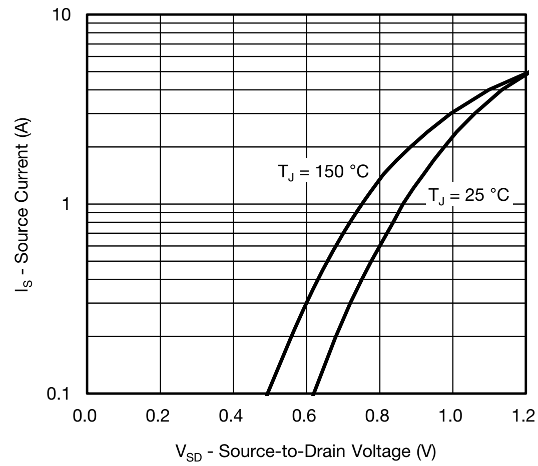


Normalized On-Resistance vs. Junction Temperature

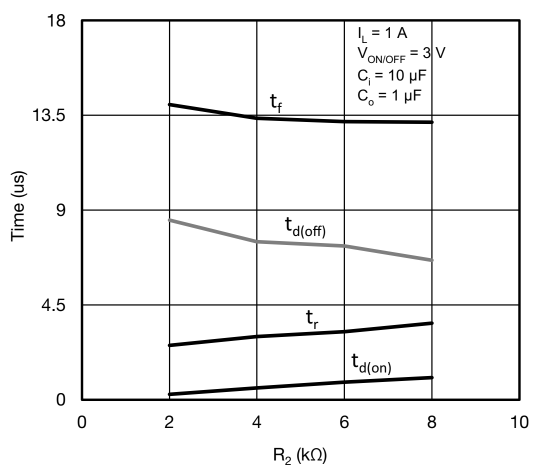
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



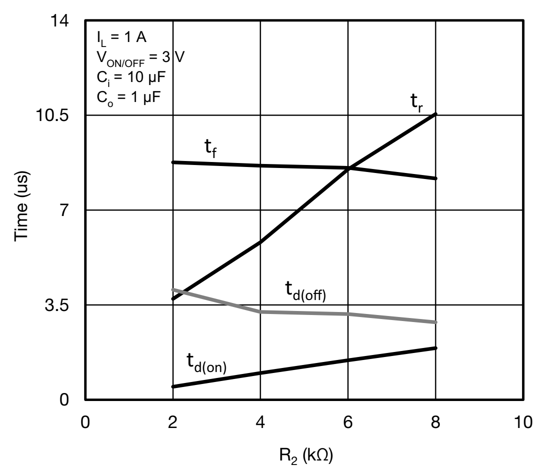
On-Resistance vs. Input Voltage



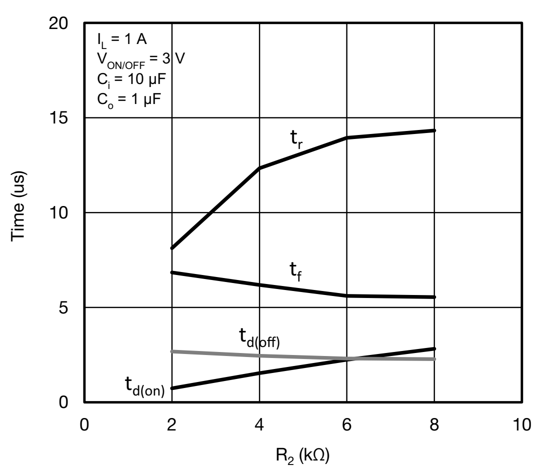
Source-Drain Diode Forward Voltage



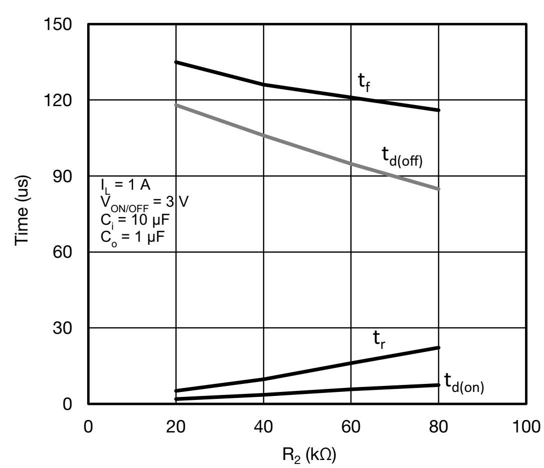
Switching Variation R2 at V_{IN} = 4.5 V, R1 = 20 kΩ



Switching Variation R2 at V_{IN} = 2.5 V, R1 = 20 kΩ

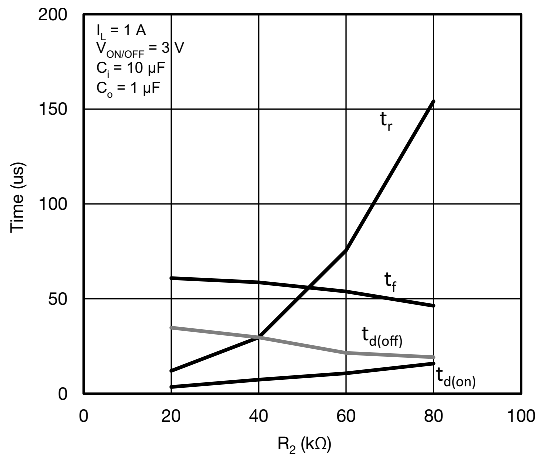


Switching Variation R2 at V_{IN} = 1.8 V, R1 = 20 kΩ

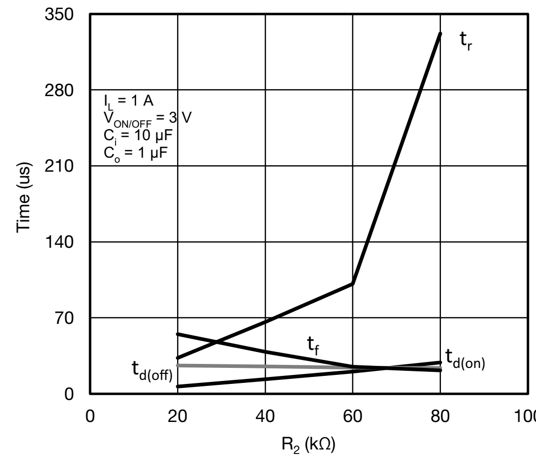


Switching Variation R2 at V_{IN} = 4.5 V, R1 = 300 kΩ

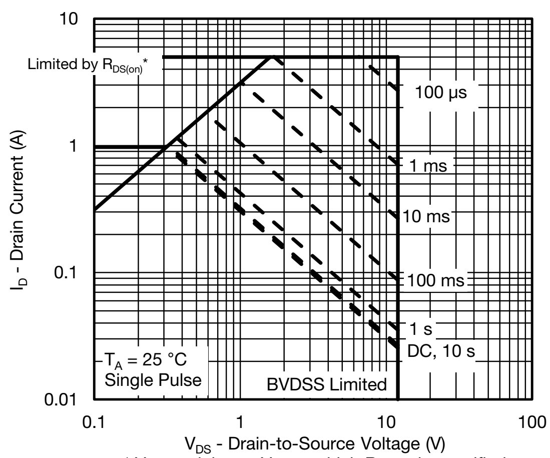
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Switching Variation R2 at V_{IN} = 2.5 V, R1 = 300 kΩ

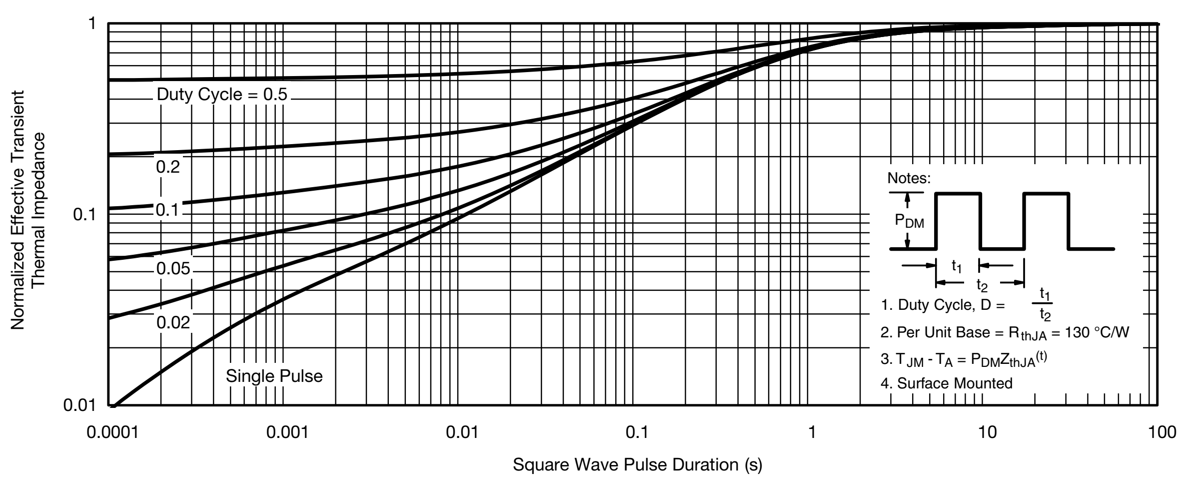


Switching Variation R2 at V_{IN} = 1.8 V, R1 = 300 kΩ



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

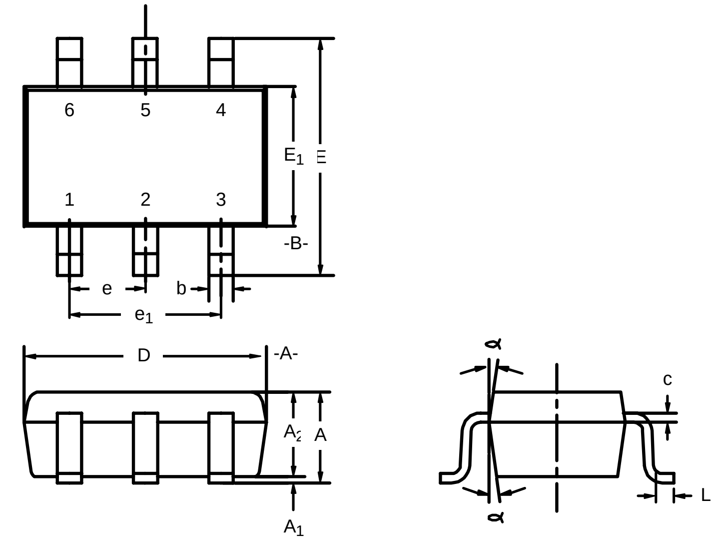
Safe Operating Area, Junction-to-Foot



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62888.

SC-70: 6-LEADS



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	–	1.10	0.035	–	0.043
A_1	–	–	0.10	–	–	0.004
A_2	0.80	–	1.00	0.031	–	0.039
b	0.15	–	0.30	0.006	–	0.012
c	0.10	–	0.25	0.004	–	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E_1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e_1	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5550

Dual-Channel LITTLE FOOT® SC-70 6-Pin MOSFET Recommended Pad Pattern and Thermal Performance

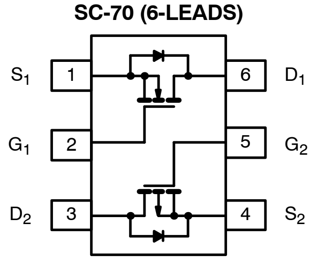
INTRODUCTION

This technical note discusses the pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for dual-channel LITTLE FOOT power MOSFETs in the SC-70 package. These new Vishay Siliconix devices are intended for small-signal applications where a miniaturized package is needed and low levels of current (around 250 mA) need to be switched, either directly or by using a level shift configuration. Vishay provides these devices with a range of on-resistance specifications in 6-pin versions. The new 6-pin SC-70 package enables improved on-resistance values and enhanced thermal performance.

PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the dual-channel SC-70 device in the 6-pin configuration.

SOT-363
SC-70 (6-LEADS)



Top View

FIGURE 1.

For package dimensions see outline drawing SC-70 (6-Leads) (http://www.vishay.com/doc?71154)

BASIC PAD PATTERNS

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/doc?72286) for the 6-pin SC-70. This basic pad pattern is sufficient for the low-power applications for which this package is intended. For the 6-pin device, increasing the pad patterns yields a reduction in thermal resistance on the order of 20% when using a 1-inch square with full copper on both sides of the printed circuit board (PCB).

EVALUATION BOARDS FOR THE DUAL SC70-6

The 6-pin SC-70 evaluation board (EVB) measures 0.6 inches by 0.5 inches. The copper pad traces are the same as described in the previous section, *Basic Pad Patterns*. The board allows interrogation from the outer pins to 6-pin DIP connections permitting test sockets to be used in evaluation testing.

The thermal performance of the dual SC-70 has been measured on the EVB with the results shown below. The minimum recommended footprint on the evaluation board was compared with the industry standard 1-inch square FR4 PCB with copper on both sides of the board.

THERMAL PERFORMANCE

Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the dual SC-70 6-pin package measured as junction-to-foot thermal resistance is 300°C/W typical, 350°C/W maximum. The "foot" is the drain lead of the device as it connects with the body. Note that these numbers are somewhat higher than other LITTLE FOOT devices due to the limited thermal performance of the Alloy 42 lead-frame compared with a standard copper lead-frame.

Junction-to-Ambient Thermal Resistance (dependent on PCB size)

The typical $R\theta_{JA}$ for the dual 6-pin SC-70 is 400°C/W steady state. Maximum ratings are 460°C/W for the dual. All figures based on the 1-inch square FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the dual 6-pin SC-70 package at two different ambient temperatures.

SC-70 (6-PIN)	
Room Ambient 25 °C	**Elevated Ambient 60 °C**
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$
$P_D = \frac{150^oC - 25^oC}{400^oC/W}$	$P_D = \frac{150^oC - 60^oC}{400^oC/W}$
$P_D = 312\ mW$	$P_D = 225\ mW$

NOTE: Although they are intended for low-power applications, devices in the 6-pin SC-70 will handle power dissipation in excess of 0.2 W.

Testing

To aid comparison further, Figure 2 illustrates the dual-channel SC-70 thermal performance on two different board sizes and two different pad patterns. The results display the thermal performance out to steady state. The measured steady state values of $R\theta_{JA}$ for the dual 6-pin SC-70 are as follows:

LITTLE FOOT SC-70 (6-PIN)	
1) Minimum recommended pad pattern (see Figure 2) on the EVB of 0.5 inches x 0.6 inches.	518°C/W
2) Industry standard 1” square PCB with maximum copper both sides.	413°C/W

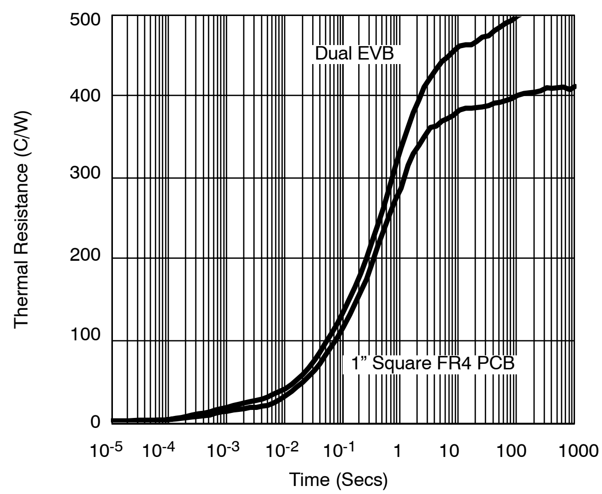


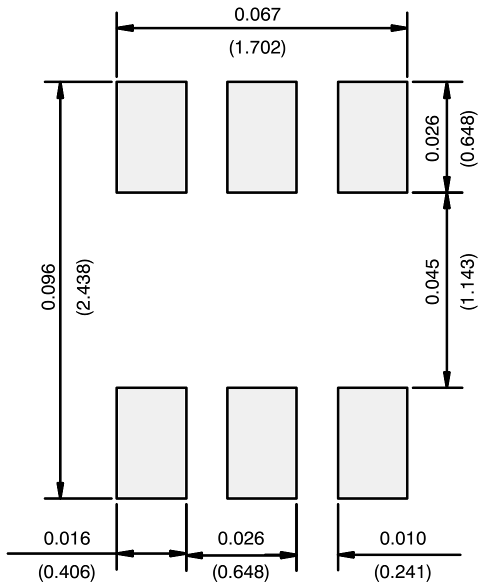
FIGURE 2. Comparison of Dual SC70-6 on EVB and 1” Square FR4 PCB.

The results show that if the board area can be increased and maximum copper traces are added, the thermal resistance reduction is limited to 20%. This fact confirms that the power dissipation is restricted with the package size and the Alloy 42 leadframe.

ASSOCIATED DOCUMENT

Single-Channel LITTLE FOOT SC-70 6-Pin MOSFET Copper Leadframe Version, REcommended Pad Pattern and Thermal Performance, AN815, (http://www.vishay.com/doc?71334).

RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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