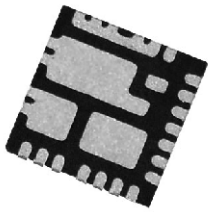
24 A Synchronous Buck Regulator



DESCRIPTION

The SiC431 is a synchronous buck regulator with integrated high side and low side power MOSFETs. Its power stage is capable of supplying 24 A continuous current at up to 1 MHz switching frequency. This regulator produces an adjustable output voltage down to 0.6 V from 3 V to 24 V input rail to accommodate a variety of applications, including computing, consumer electronics, telecom, and industrial.

SiC431's architecture delivers ultrafast transient response with minimum output capacitance and tight ripple regulation at very light load. The device is internally compensated and is stable with any capacitor. No external ESR network is required for loop stability purpose. The device also incorporates a power saving scheme that significantly increases light load efficiency.

The regulator integrates a full protection feature set, including output overvoltage protection (OVP), cycle by cycle overcurrent protection (OCP) short circuit protection (SCP) and thermal shutdown (OTP). It also has UVLO and a user programmable soft start.

The SiC431 is available in lead (Pb)-free power enhanced MLP-24L package in 4 mm x 4 mm dimension.

APPLICATIONS

- 5 V, 12 V, and 24 V input rail POLs
- Desktop, notebooks, server, and industrial computing
- Industrial and automation
- consumer electronics

FEATURES

- Versatile
  - Operation from 3 V to 24 V input voltage (4.5 V to 24 V using single supply)
  - Adjustable output voltage down to 0.6 V
  - Scalable solution 8 A (SiC438), 12 A (SiC437), and 24 A (SiC431)
  - Output voltage tracking and sequencing with pre-bias start up
  - ± 1 % output voltage accuracy at -40 °C to +125 °C
- Highly efficient
  - 97 % peak efficiency
  - 1 µA supply current at shutdown
  - 50 µA operating current not switching
- Highly configurable
  - Four programmable switching frequencies available: 300 kHz, 500 kHz, 750 kHz, and 1 MHz
  - Adjustable soft start (3 ms / 6 ms) and adjustable current limit
  - Three modes of operation
  - Forced continuous conduction, power save (SiC431B), or ultrasonic (SiC431A)
- Robust and reliable
  - Cycle-by-cycle current limit
  - Output overvoltage protection
  - Output undervoltage / short circuit protection with auto retry
  - Power good flag and over temperature protection
- Design tools
- Supported by Vishay PowerCAD Online Design Simulation (www.vishay.com/power-ics/powercad-list/)
- Evaluation board (www.vishay.com/doc?#####)

RoHS COMPLIANT
HALOGEN FREE

TYPICAL APPLICATION CIRCUIT AND PACKAGE OPTIONS

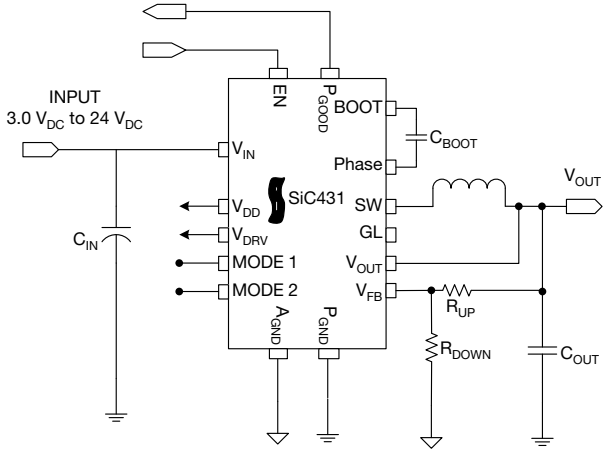


Fig. 1 - Typical Application Circuit for SiC431

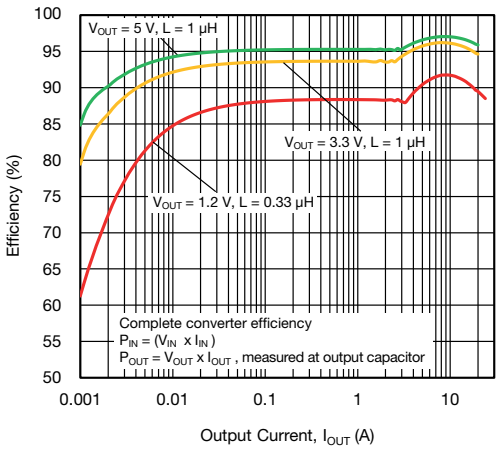


Fig. 2 - Efficiency vs. Output Current (V_{IN} = 12 V, f_{sw} = 500 kHz)

PIN CONFIGURATION

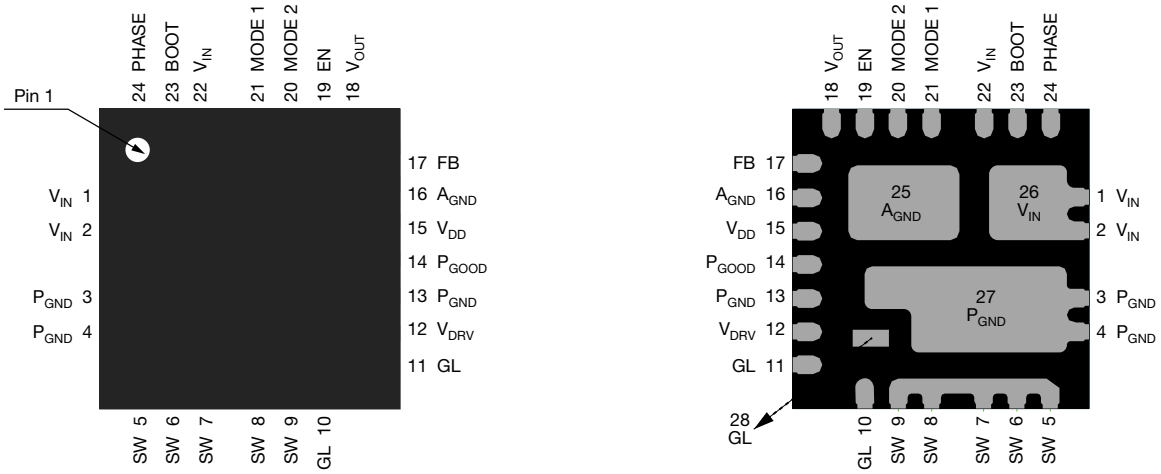


Fig. 3 - SiC431 Pin Configuration

PIN DESCRIPTION		
PIN NUMBER	**SYMBOL**	**DESCRIPTION**
1, 2, 22, 26	V_{IN}	Input voltage
3, 4, 13, 27	P_{GND}	Power signal return ground
5 to 9	SW	Switching node signal; output inductor connection point
10, 11	GL	Low side power MOSFET gate signal
12	V_{DRV}	Supply voltage for internal gate driver. Connect a 2.2 µF decoupling capacitor to P_{GND}
14	P_{GOOD}	Power good signal output; open drain
15	V_{DD}	Supply voltage for internal logic. Connect a 1 µF decoupling capacitor to A_{GND}
16, 25	A_{GND}	Analog signal return ground
17	FB	Output voltage feedback pin; connect to V_{OUT} through a resistor divider network.
18	V_{OUT}	Output voltage sense pin
19	EN	Enable pin
20	MODE 2	Connect a resistor to V_{DD} to set the soft start timing at 6 ms and current limit level; connect a resistor to A_{GND} to set the soft start timing at 3 ms and current limit level
21	MODE 1	Connect a resistor to V_{DD} for CCM and switching frequency setting; connect a resistor to A_{GND} for DCM and switching frequency setting
23	BOOT	Bootstrap pin; connect a capacitor to PHASE pin for HS power MOSFET gate voltage supply
24	PHASE	Switching node signal for bootstrap return path

ORDERING INFORMATION						
PART NUMBER	**PART MARKING**	**MAXIMUM CURRENT**	**V_{DD}, V_{DRV}**	**LIGHT LOAD MODE**	**JUNCTION TEMPERATURE RANGE**	**PACKAGE**
SiC431AED-T1-GE3	SiC431A	24 A	Internal	Ultrasonic	-40 °C to +125 °C	PowerPAK® MLP44-24L
SiC431BED-T1-GE3	SiC431B			Power saving		
SiC431CED-T1-GE3	SiC431C		External	Ultrasonic		
SiC431DED-T1-GE3	SiC431D			Power saving		

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)			
ELECTRICAL PARAMETER	**CONDITIONS**	**LIMITS**	**UNIT**
V_{IN}	Reference to P_{GND}	-0.3 to +25	V
V_{OUT}	Reference to P_{GND}	-0.3 to +22	
V_{DD} / V_{DRV}	Reference to P_{GND}	-0.3 to +6	
SW / PHASE	Reference to P_{GND}	-0.3 to +25	
SW / PHASE (AC)	100 ns; reference to P_{GND}	-4 to +30; negative side = -8 V with 100 ns duration	
BOOT		-0.3 to +31	
BOOT to SW		-0.3 to +6	
A_{GND} to P_{GND}		-0.3 to +0.3	
EN		-0.3 to +25	
All other pins	Reference to A_{GND}	-0.3 to +6	
Temperature			
Junction temperature	T_J	-40 to +150	°C
Storage temperature	T_{STG}	-65 to +150	
Power Dissipation			
Junction to ambient thermal impedance ($R_{\theta JA}$)		16	°C/W
Junction to case thermal impedance ($R_{\theta JC}$)		2	
Maximum power dissipation	Ambient temperature = 25 °C	6.25	
ESD Protection			
Electrostatic discharge protection	Human body model	4000	V
	Charged device model	1000	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (all voltages referenced to GND = 0 V)				
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Input voltage (V_{IN})	4.5	-	24	V
Enable (EN)	0	-	24	
Input voltage (V_{IN}), external 5.3 V on V_{DD} / V_{DRV}	3	-	24	
Output voltage (V_{OUT})	0.6	-	0.9 x V_{IN} and < 20 V	
Temperature				
Recommended ambient temperature	-40 to +105			°C
Operating junction temperature	-40 to +125			

ELECTRICAL SPECIFICATIONS (V_{IN} = 12 V, T_J = -40 °C to +125 °C, unless otherwise stated)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Power Supplies						
V_{DD} supply	V_{DD}	V_{IN} = 6 V to 24 V, V_{EN} = 5 V, not switching	4.75	5	5.25	V
V_{DD} UVLO threshold, rising	V_{DD_UVLO}		3	3.3	3.6	
V_{DD} UVLO hysteresis	$V_{DD\_UVLO\_HYST}$		-	300	-	mV
Maximum V_{DD} current	I_{DD}	V_{IN} = 6 V to 24 V	3	-	-	mA
V_{DRV} supply	V_{DRV}	V_{IN} = 6 V to 24 V, V_{EN} = 5 V, not switching	4.75	5	5.25	V
Maximum V_{DRV} current	I_{DRV}	V_{IN} = 6 V to 24 V	50	-	-	mA
Input current	IV_{IN}	Non-switching, V_{FB} > 0.6 V	-	50	120	µA
Shutdown current	IV_{IN_SHDN}	V_{EN} = 0 V	-	0.5	3	
Controller and Timing						
Feedback voltage	V_{FB}	T_J = 25 °C	597	600	603	m/V
		T_J = -40 °C to +125 °C (1)	594	600	606	
V_{FB} input bias current	I_{FB}		-	2	-	nA
Minimum on-time	$t_{ON\_MIN.}$		-	50	65	ns
t_{ON} accuracy	$t_{ON\_ACCURACY}$		-10	-	10	%
On-time range	t_{ON_RANGE}		65	-	2250	ns
Minimum frequency, skip mode	f_{kHz}	Ultrasonic version (SiC431A)	20	-	-	kHz
		Power save version (SiC431B)	0	-	-	
Minimum off-time	$t_{OFF\_MIN.}$		205	250	305	ns
Power MOSFETs						
High side on resistance	R_{ON_HS}	V_{DRV} = 5 V, T_A = 25 °C	-	6	-	mΩ
Low side on resistance	R_{ON_LS}		-	2	-	
Fault Protections						
Valley current limit	I_{OCL}	T_J = -10 °C to +125 °C	-20	-	20	%
Output OVP threshold	OVP	V_{FB} with respect to 0.6 V reference	-	20	-	
Output UVP threshold	UVP		-	-80	-	
Over temperature protection	OTP_R	Rising temperature	-	150	-	°C
	OTP_{HYST}	Hysteresis	-	25	-	
Power Good						
Power good output threshold	$V_{FB\_RISING\_VTH\_OV}$	V_{FB} rising above 0.6 V reference	-	20	-	%
	$V_{FB\_FALLING\_VTH\_UV}$	V_{FB} falling below 0.6 V reference	-	-10	-	
Power good hysteresis	P_{GOOD_HYST}		-	40	-	mV
Power good on resistance	R_{ON_PGOOD}		-	7.5	15	Ω
Power good delay time	t_{DLY_PGOOD}		15	25	35	µs
EN / MODE / Ultrasonic Threshold						
EN logic high level	V_{EN_H}		1.6	-	-	V
EN logic low level	V_{EN_L}		-	-	0.4	
EN pull down resistance	R_{EN}		-	5	-	MΩ
Switching Frequency						
Switching frequency	f_{sw}	R_{MODE1} = 51 kΩ	-	300	-	kHz
		R_{MODE1} = 100 kΩ	-	500	-	
		R_{MODE1} = 200 kΩ	-	750	-	
		R_{MODE1} = 500 kΩ	-	1000	-	
Soft Start						
Soft start time	t_{ss}	Connect R_{MODE2} between MODE2 and GND	2.7	4.5	6.3	ms
		Connect R_{MODE2} between MODE2 and V_{DD}	5.4	9	12.6	
Over Current Protection						
Over current limit (inductor valley current)	I_{OCL}	R_{MODE2} = 500 kΩ	-	32	-	A
		R_{MODE2} = 200 kΩ	-	24.8	-	
		R_{MODE2} = 100 kΩ	-	17.3	-	
		R_{MODE2} = 51 kΩ	-	9.6	-	

Note
(1) Guaranteed by design

FUNCTIONAL BLOCK DIAGRAM

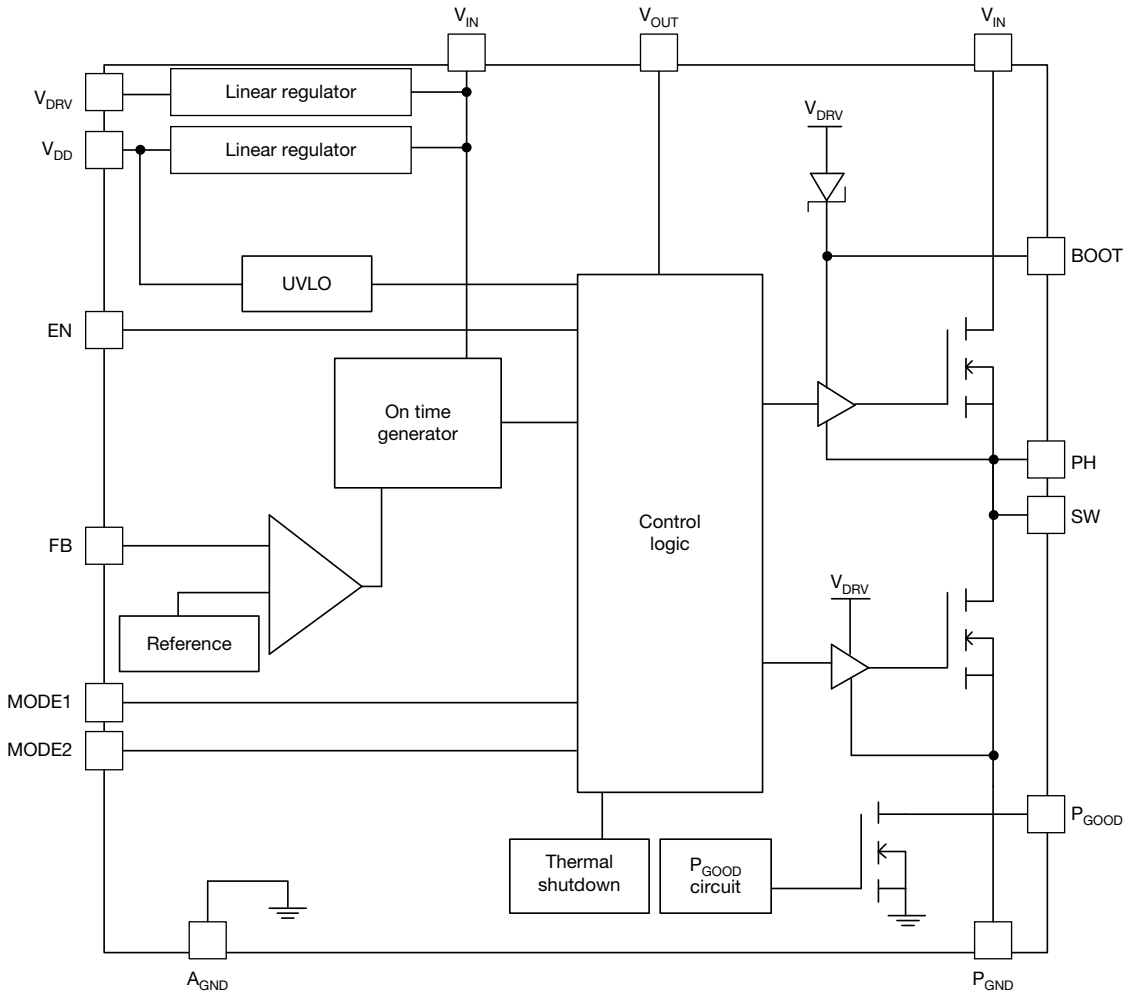


Fig. 4 - SiC431 Functional Block Diagram

OPERATIONAL DESCRIPTION

Device Overview

SiC431 is a high efficiency synchronous buck regulator capable of delivering up to 24 A continuous current. The device has programmable switching frequency of 300 kHz, 500 kHz, 750 kHz, and 1 MHz. The control scheme delivers fast transient response and minimizes external components. Thanks to the internal current ramp information, no high ESR output bulk or virtual ESR network is required for the loop stability. This device also incorporates a power saving feature by enabling diode emulation mode and frequency fold back as the load decreases.

SiC431 has a full set of protection and monitoring features:

- Over current protection in pulse-by-pulse mode
- Output over voltage protection
- Output under voltage protection with device latch
- Over temperature protection with hysteresis
- Dedicated enable pin for easy power sequencing
- Power good open drain output

This device is available in MLP44-24L package to deliver high power density and minimize PCB area.

Power Stage

SiC431 integrates a high performance power stage with a ~ 2 mΩ n-channel low side MOSFET and a 6 mΩ n-channel high side MOSFET. The MOSFETs are optimized to achieve up to 97 % efficiency.

The input voltage (V_{IN}) can go up to 24 V and down as low as 4.5 V for power conversion. For input voltages (V_{IN}) below 4.5 V an external 5.3 V supply on V_{DD} and V_{DRV} is required.

Control Mechanism

SiC431 employs a voltage - mode COT control mechanism. During steady-state operation, feedback voltage is compared with internal reference (0.6 V typ.) and the amplified error signal (V_{COMP}) is generated in the internal comp node. An internally generated ramp signal and V_{COMP} are fed into a comparator. Once V_{RAMP} crosses V_{COMP}, a single shot on-time pulse is generated for a fixed time, programmed by the external R_{fsw}. During the on-time pulse, the high side MOSFET will be turned on. Once the on-time pulse expires, the low side MOSFET will be turned on after a break-before-make period. The low side MOSFET will be on for duration of minimum off-time pulse until V_{RAMP} crosses V_{COMP}. The cycle is then repeated.

Fig. 5 illustrates the basic block diagram for VM-COT architecture. In this architecture the following is achieved:

- The reference of a basic ripple control regulator is replaced with a high again error amplifier loop
- This establishes two parallel voltage regulating feedback paths, a fast and slow path (hence V2)
- Fast path is the ripple injection which ensures rapid correction of the transient perturbation
- Slow path is the error amplifier loop which ensures the DC component of the output voltage follows the internal accurate reference voltage

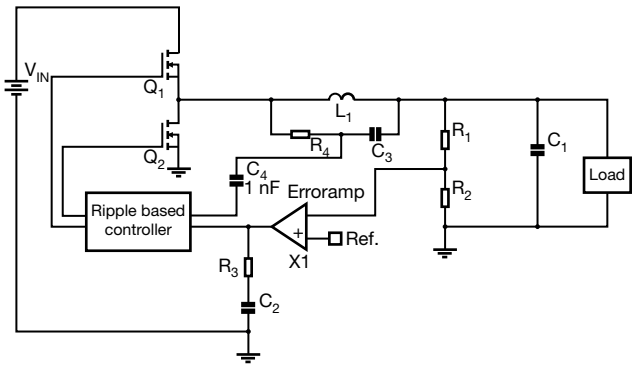


Fig. 5 - VM-COT Block Diagram

The SiC431 integrates the error amplifier compensation components (R_3 and C_2) and the ripple injection components (R_4, C_4, and C_3) shown in Fig. 5. Based on the operating modes, the regulator automatically picks the correct compensation and ripple injection components from an array that is available on the IC die. This reduces external components and makes the use of the SiC431 far simpler than industry standard regulators that require external components to be calculated for each voltage rail in the system.

Fig. 6 demonstrates the basic operational waveforms:

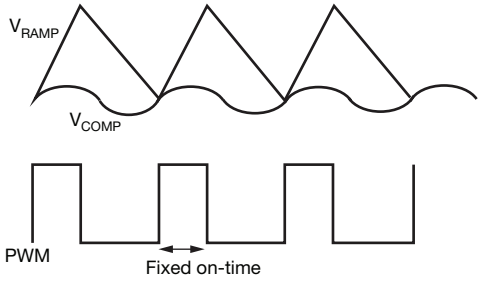


Fig. 6 - VM-COT Operational Principle

Mode Setting, Soft Start, and Frequency Selection

To improve efficiency at light-load condition, SiC431 provides a set of innovative implementations to eliminate LS re-circulating current and switching losses. The internal zero crossing detector (ZCD) monitors V_{SW} node voltage to determine when inductor current starts to flow negatively. In power saving mode, as soon as inductor valley current crosses zero, the device first deploys diode emulation mode by turning off LS FET. If load further decreases, switching frequency is further reduced proportional to load condition to save switching losses while keeping output ripple within tolerance. The switching frequency is set by the controller to maintain regulation. In the standard power save mode, there is no minimum switching frequency for SiC431B.

For SiC431A, the minimum switching frequency that the regulator will drop to is 25 kHz as the part avoids switching frequencies in the audible range to prevent audible noise. In this version of the part, the light load mode, is called the ultrasonic mode.

The SiC431 has a low pin count and minimum external components. To offer the user maximum flexibility to choose soft start times, current limit settings, switching frequencies and to enable or disable the light load mode, just two MODE pins are used and a particular resistor value connected to V_{DD} or GND allows the user to choose various operating modes.This is best explained by the below tables:

TABLE 1 - MODE 1 CONFIGURATION SETTINGS

OPERATION	CONNECTION	f_{SWITCH} (kHZ)	R_{MODE1} (kΩ)
Skip	To A_{GND}	300	51
		500	100
		750	200
		1000	500
Forced CCM	To V_{DD}	300	51
		500	100
		750	200
		1000	500

TABLE 2 - MODE 2 CONFIGURATION SETTINGS

SOFT-START TIME	CONNECTION	I_{LIMIT} (%)	R_{MODE2} (kΩ)
3 ms	To A_{GND}	30	51
		54	100
		78	200
		100 (32 A)	500
6 ms	To V_{DD}	30	51
		54	100
		78	200
		100 (32 A)	500

OUTPUT MONITORING AND PROTECTION FEATURES

Output Overcurrent Protection (OCP)

SiC431 has pulse-by-pulse overcurrent limit control. The inductor valley current is monitored during LS FET turn-on period through $R_{DS(on)}$ sensing. After a pre-defined blanking time, the valley current is compared with internal threshold to determine the threshold for OCP. If monitored current is higher than threshold, HS turn-on pulse is skipped and LS FET is kept on until the valley current returns below OCP limit.

In the severe over-current condition, pulse-by-pulse current limit eventually triggers output undervoltage protection (UVP) and the device will go into hiccup mode as described in the next section.

OCP is enabled immediately after V_{DD} passes UVLO level.

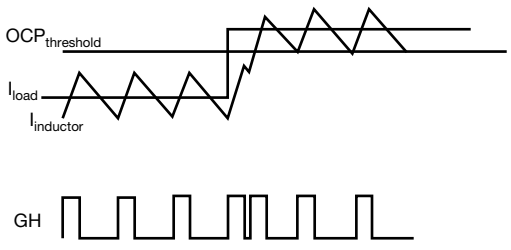


Fig. 7 - Over-Current Protection Illustration

Output Undervoltage Protection (UVP)

UVP is implemented by monitoring output through V_{FB} pin. If the voltage level at V_{FB} goes below 0.54 V for more than 25 µs, then a UVP event is recognized and both HS and LS MOSFETs are turned off. After a period of 20 soft start cycles, the IC attempts to re-start and goes through a soft start cycle. If the fault condition still exists, the above cycle will be repeated.

UVP is only active after the completion of soft-start sequence.

Output Overvoltage Protection (OVP)

For OVP implementation, output is monitored through FB pin. After soft start, if the voltage level at FB is above 20 % (typ.), OVP is triggered with both the HS and LS MOSFETs turned off. Normal operation is resumed once FB voltage drops back to 0.672 V.

OVP is active immediately after V_{DD} passes UVLO level.

Over-Temperature Protection (OTP)

SiC431 has internal thermal monitor block that turns off both HS and LS FETs when junction temperature is above 150 °C (typ). A hysteresis of 35 °C is implemented, so when junction temperature drops below 115 °C, the device restarts by initiating soft-start sequence again.

Sequencing of Input / Output Supplies

SiC431 has no sequencing requirements on any of its input / output (V_{IN}, V_{DRV}, V_{DD}, EN) supplies or enables. In cases with input voltages below 4.5 V the V_{DD} and V_{DRV} pins must be biased first (> 5.3 V).

Enable

The SiC431 has an enable pin to turn the part on and off. Driving this pin high enables the device, while grounding it turns it off.

The SiC431 enable has a weak pull down to prevent unwanted turn on due to a floating GPIO.

There are no sequencing requirements w.r.t other input / output supplies.

Pre-Bias Start-Up

In case of pre-bias startup, output is monitored through FB pin. If the sensed voltage on FB is higher than the internal reference ramp value, control logic prevents HS and LS FET from switching to avoid negative output voltage spike and excessive current sinking through LS FET.

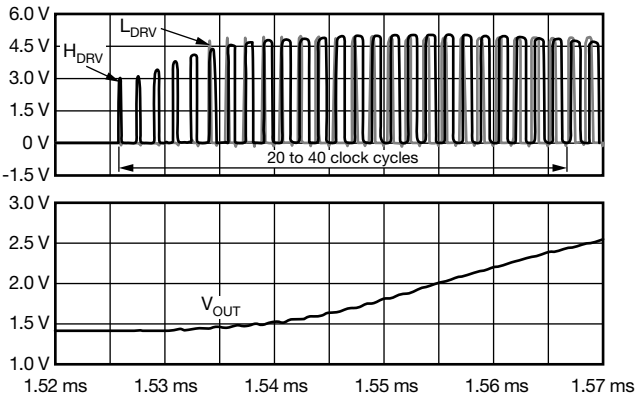


Fig. 8 - Pre-Bias Start-Up

Power Good

SiC431's power good is an open-drain output. Pull P_{GOOD} pin high up to 5 V through a 10K resistor to use this signal. Power good window is shown in the below diagram. If voltage level on FB pin is out of this window, PG signal is de-asserted by pulling down to GND. To prevent false triggering during transient events, P_{GOOD} has a 25 µs blanking time.

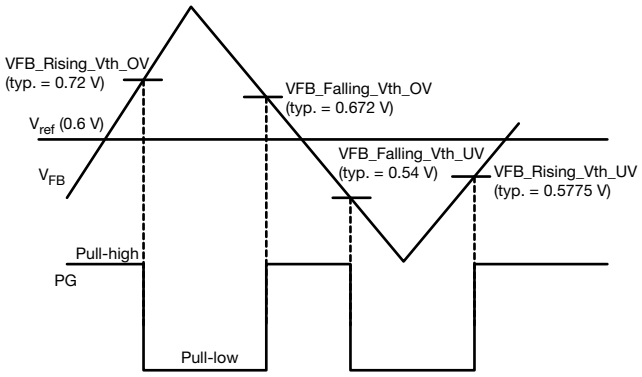


Fig. 9 - P_{GOOD} Window and Timing Diagram

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{sw} = 500 kHz, C_{OUT} = 47 µF x 13, C_{IN} = 10 µF x 6, unless otherwise noted)

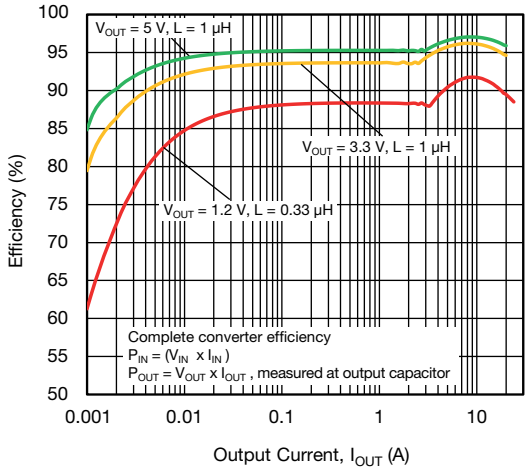


Fig. 10 - Efficiency vs. Output Current (V_{IN} = 12 V, f_{sw} = 500 kHz)

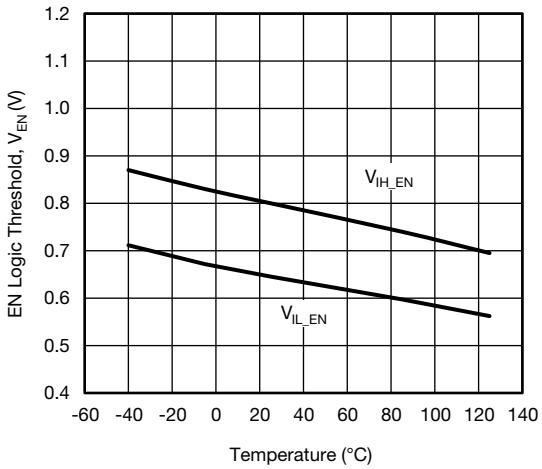


Fig. 13 - EN Logic Threshold vs. Junction Temperature

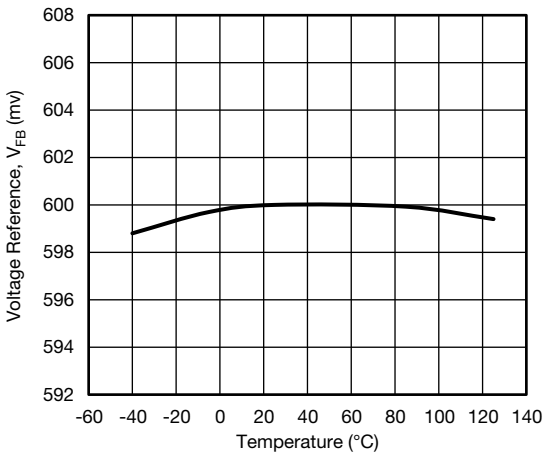


Fig. 11 - Voltage Reference vs. Junction Temperature

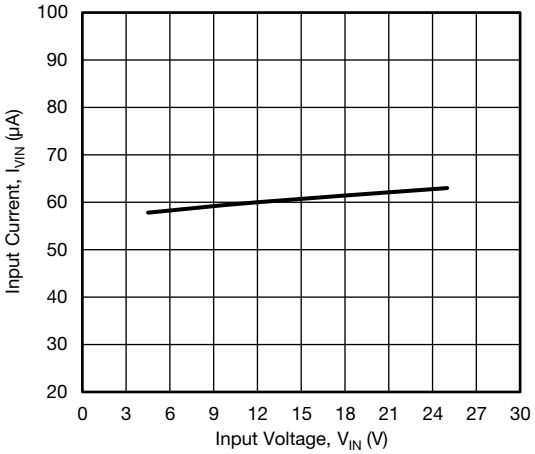


Fig. 14 - Input Current vs. Input Voltage

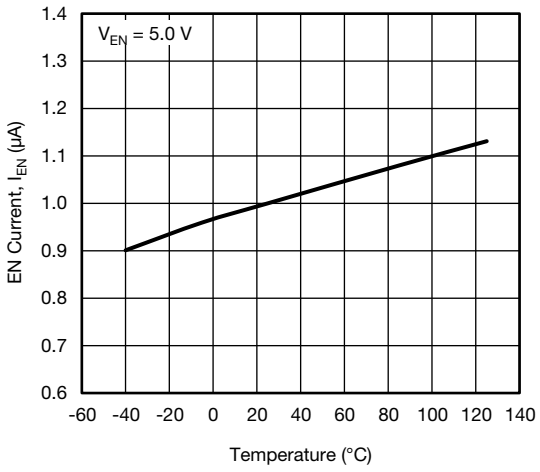


Fig. 12 - EN Current vs. Junction Temperature

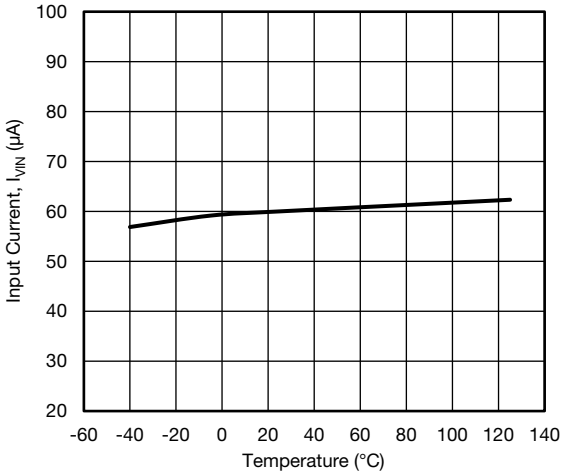


Fig. 15 - Input Current vs. Junction Temperature

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{sw} = 500 kHz, C_{OUT} = 47 µF x 13, C_{IN} = 10 µF x 6, unless otherwise noted)

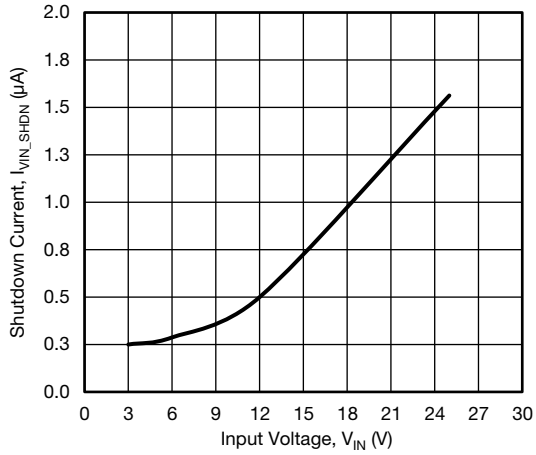


Fig. 16 - Shutdown Current vs. Input Voltage

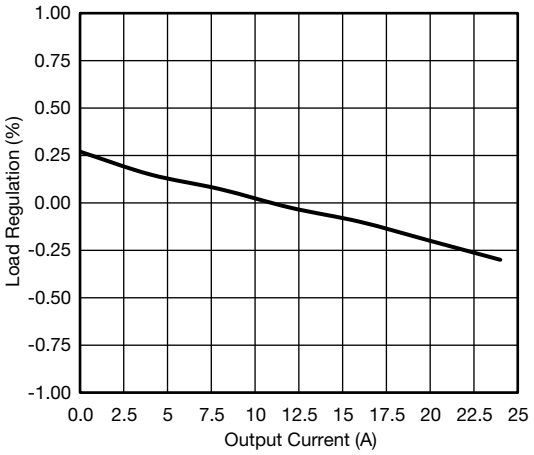


Fig. 19 - Load Regulation vs. Output Current

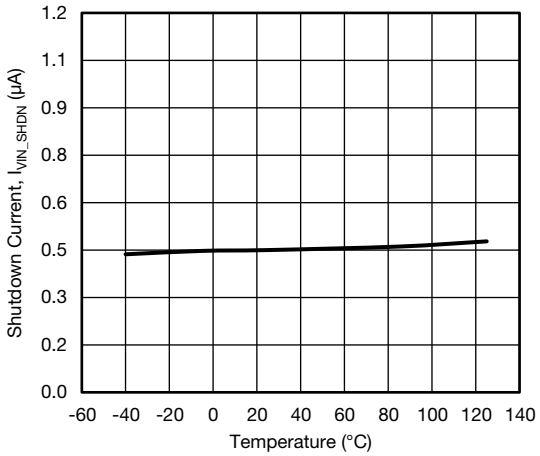


Fig. 17 - Shutdown Current vs. Junction Temperature

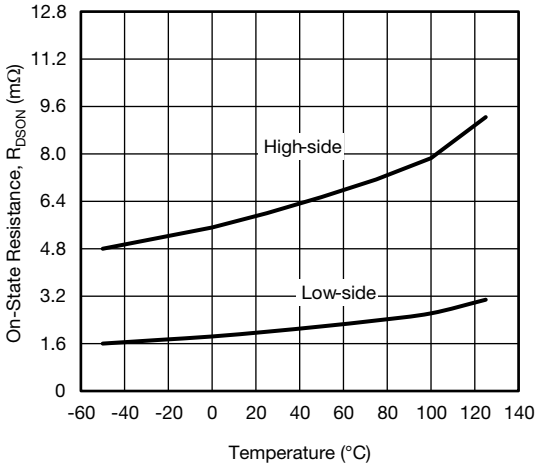


Fig. 20 - On Resistance vs. Junction Temperature

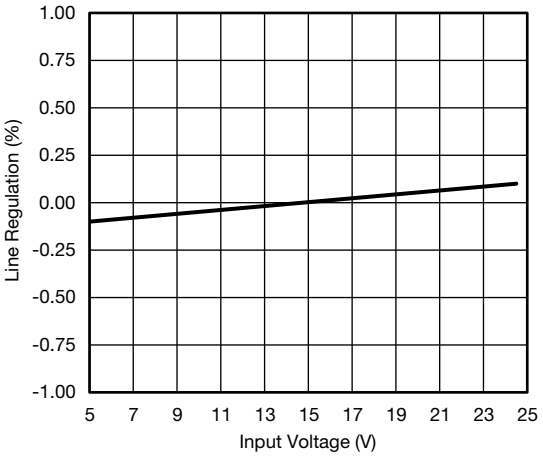


Fig. 18 - Line Regulation vs. Input Voltage

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{sw} = 500 kHz, C_{OUT} = 47 µF x 13, C_{IN} = 10 µF x 6, unless otherwise noted)

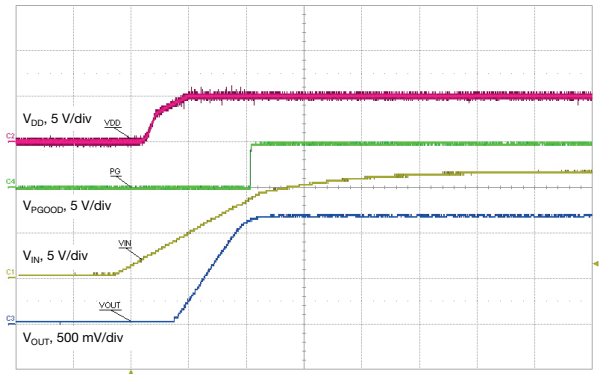


Fig. 21 - Startup with V_{IN}, t = 2 ms/div

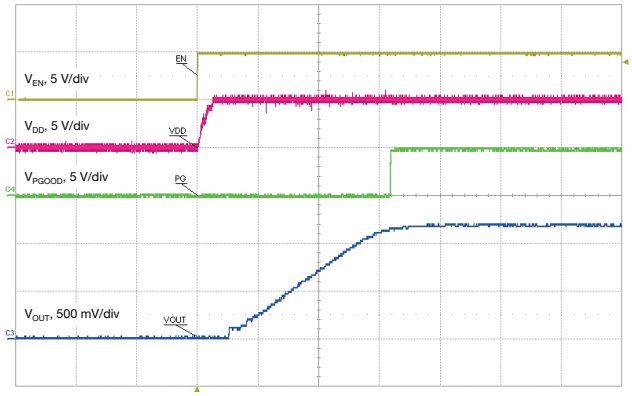


Fig. 24 - Startup with EN, t = 1 ms/div

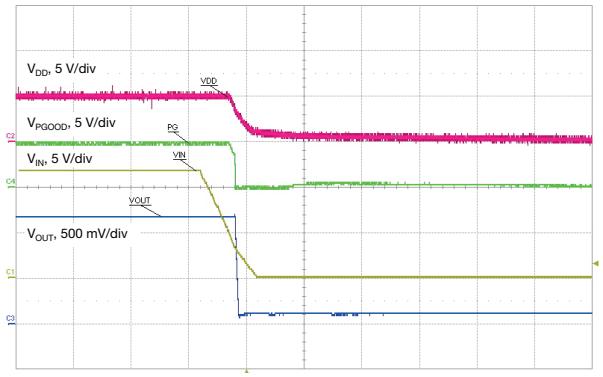


Fig. 22 - Shut down with V_{IN}, t = 100 ms/div

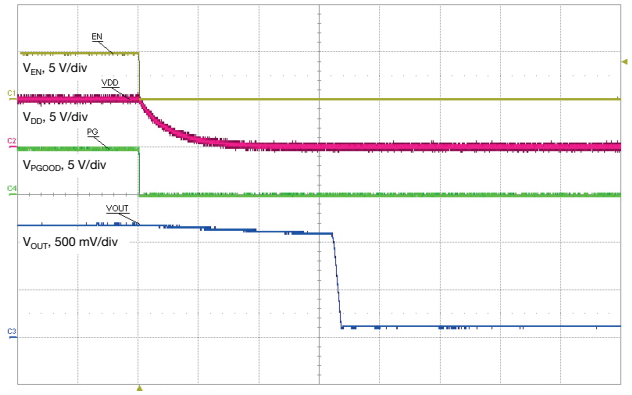


Fig. 25 - Shut down with EN, t = 200 ms/div

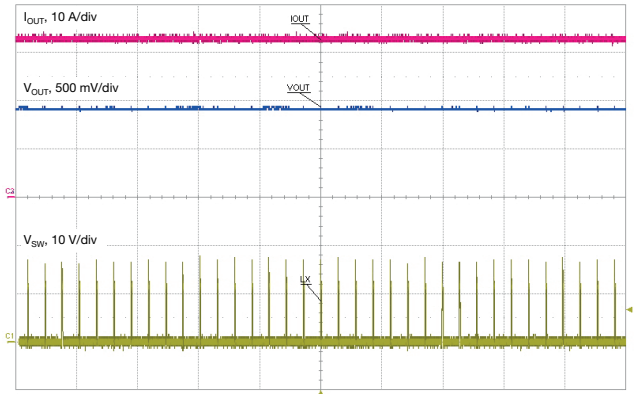


Fig. 23 - Overcurrent Protection Behavior, t = 5 µs/div

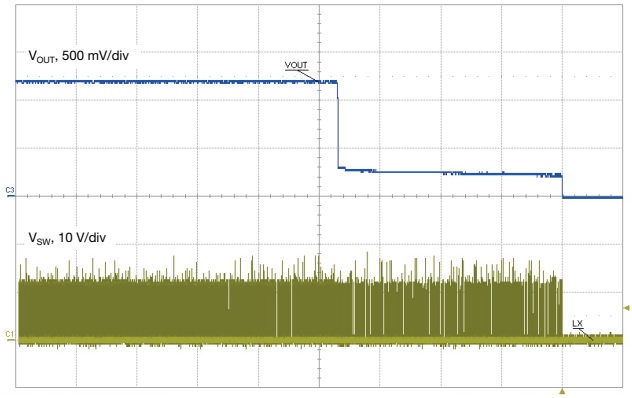


Fig. 26 - Output Undervoltage Protection Behavior, t = 50 ms/div

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{sw} = 500 kHz, C_{OUT} = 47 µF x 13, C_{IN} = 10 µF x 6, unless otherwise noted)

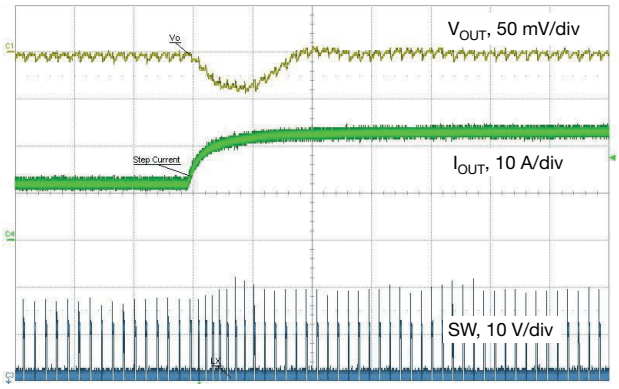


Fig. 27 - Load Step, 12 A to 24 A, 1 A/µs, t = 10 µs/div

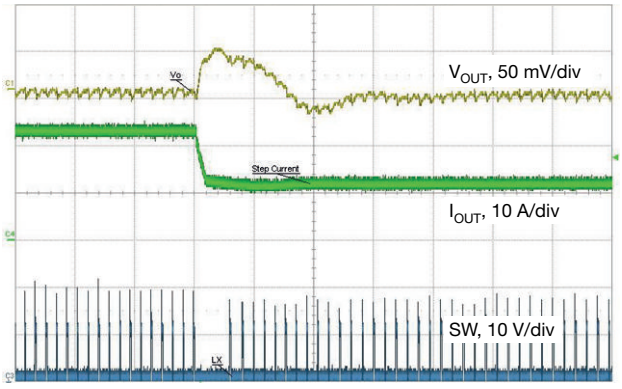


Fig. 30 - Load Release, 24 A to 12 A, 1 A/µs, t = 10 µs/div

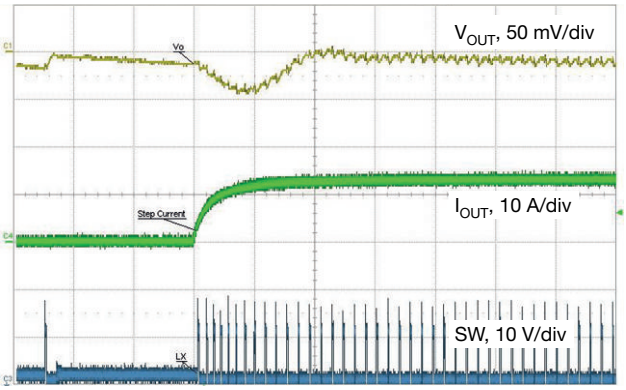


Fig. 28 - Load Step, 0.1 A to 12 A, 1 A/µs, t = 10 µs/div
Skip Mode Enabled

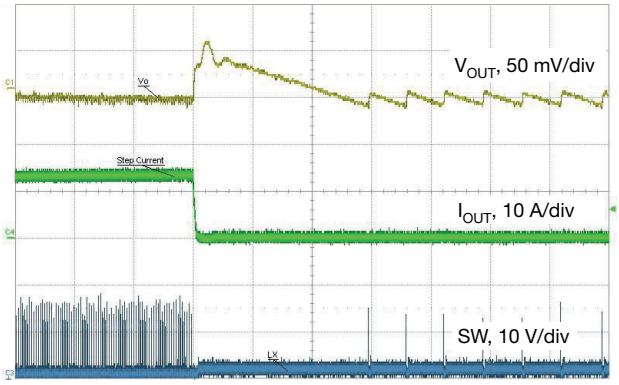


Fig. 31 - Load Release, 12 A to 0.1 A, 1 A/µs, t = 50 µs/div
Skip Mode Enabled

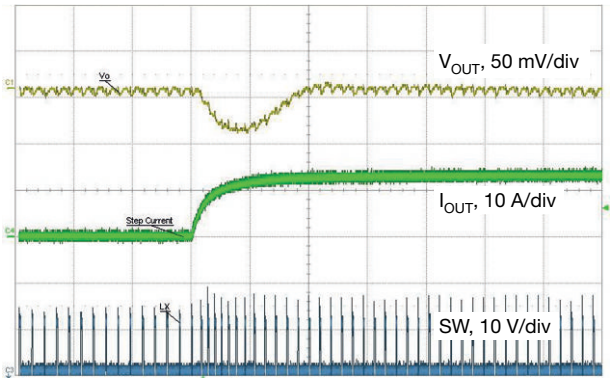


Fig. 29 - Load Step, 0.1 A to 12 A, 1 A/µs, t = 10 µs/div
Forced Continuous Conduction Mode

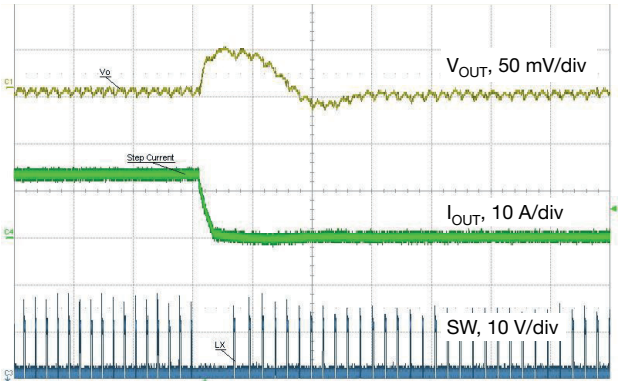


Fig. 32 - Load Release, 12 A to 0.1 A, 1 A/µs, t = 20 µs/div
Forced Continuous Conduction Mode

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{sw} = 500 kHz, C_{OUT} = 47 µF x 13, C_{IN} = 10 µF x 6, unless otherwise noted)

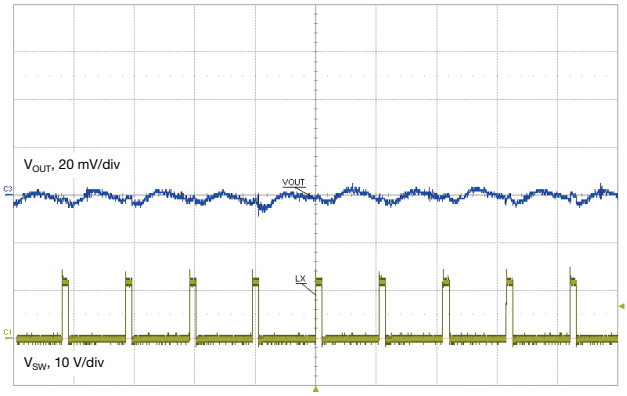


Fig. 33 - Output Ripple, 0.1 A, t = 2 µs/div
Forced Continuous Conduction Mode

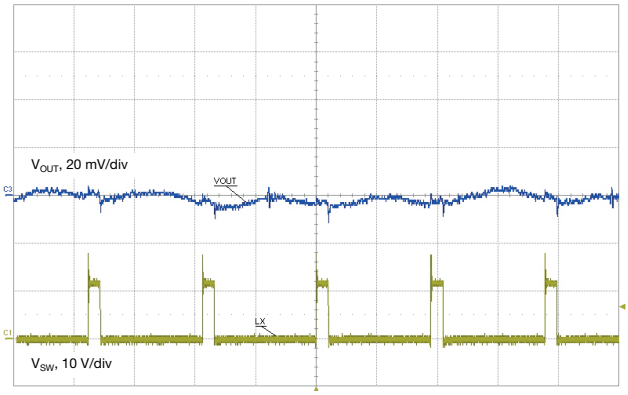


Fig. 35 - Output Ripple, 12 A, t = 1 µs/div
Forced Continuous Conduction Mode

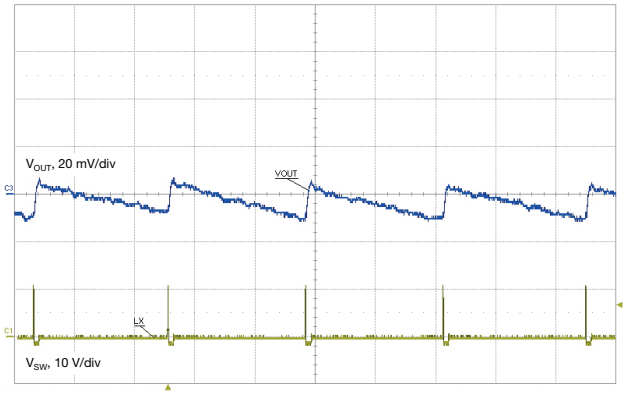


Fig. 34 - Output Ripple, 0.1 A, t = 20 µs/div
Skip Mode Enabled

EXAMPLE SCHEMATIC FOR SiC431

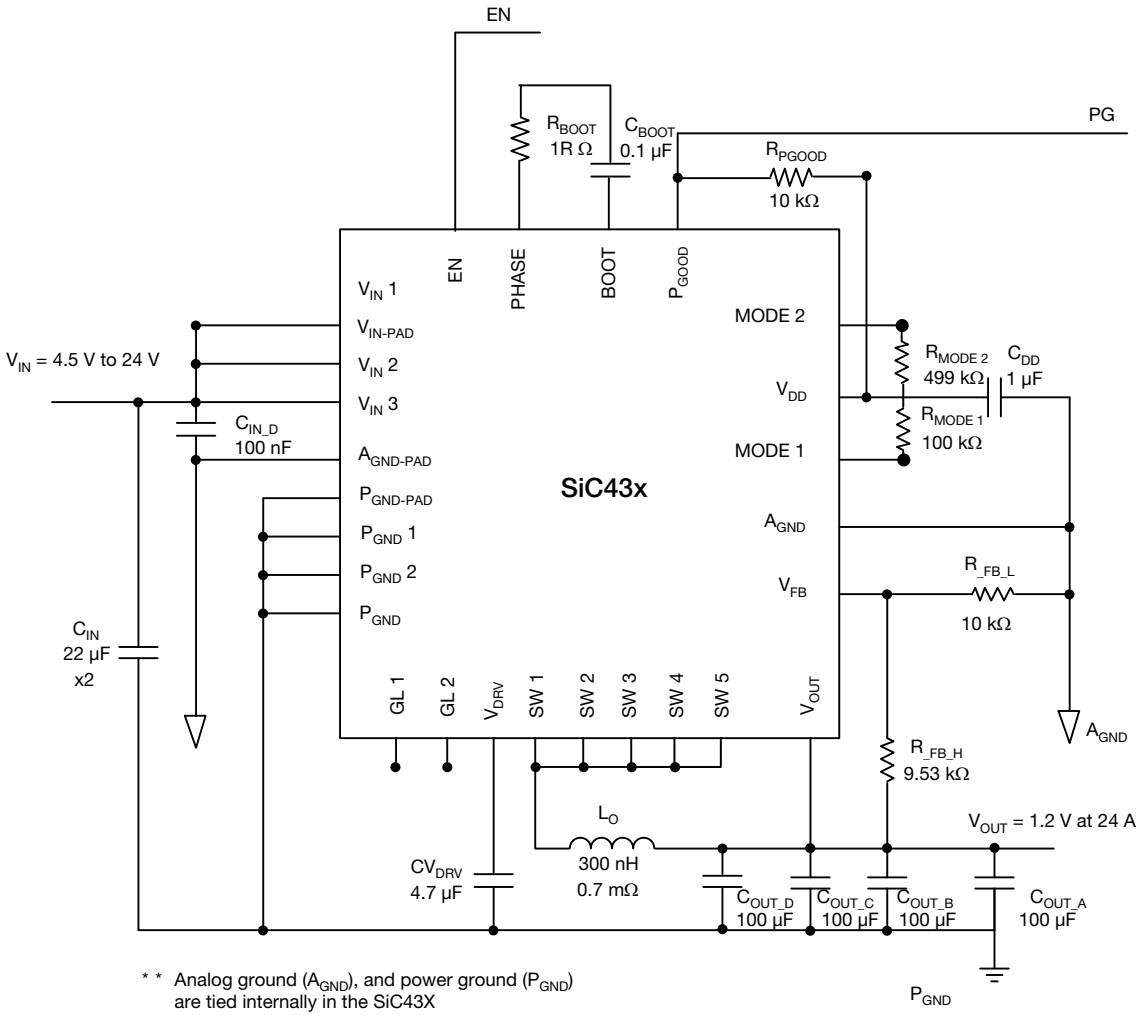


Fig. 36 - Schematic

EXTERNAL COMPONENT SELECTION FOR THE SiC43X

This section explains external component selection for the SiC43x family of regulators. Component reference designators in any equation refer to the schematic shown in Fig. 36.
The user can use the PowerCAD online design center to simplify external component calculations.

Output Voltage Adjustment

If a different output voltage is needed, simply change the value of V_{OUT} and solve for $R_{\_FB\_H}$ based on the following formula:

$$R_{\_FB\_H} = \frac{R_{\_FB\_L}(V_{OUT} - V_{FB})}{V_{FB}}$$

Where V_{FB} is 0.6 V for the SiC43X. $R_{\_FB\_L}$ should be a maximum of 10 kΩ to prevent V_{OUT} from drifting at no load.

Inductor Selection

The choice of inductor is specific to each application and quickly determined with the following equations:

$$t_{ON} = \frac{V_{OUT}}{V_{IN\_max.} \times f_{sw}}$$

and

$$L = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{I_{OUT\_MAX.} \times K}$$

Where K is a percentage of maximum output current ripple required. The designer can quickly make a choice of inductor if the ripple percentage is decided, usually no more than 30 % however higher or lower percentages of I_{OUT} can be acceptable depending on application. This device allows choices larger than 30 %.

Other than the inductance the DCR and saturation current parameters are key values. The DCR causes an I^2R loss which will decrease the system efficiency and generate heat. The saturation current has to be higher than the maximum output current plus ½ of the ripple current. In an over current condition the inductor current may be very high. All this needs to be considered when selecting the inductor.

Output Capacitor Selection

The SiC43x is stable with any type of output capacitors by choosing the appropriate ripple injection components. This allows the user to choose the output capacitance based on the best trade off of board space, cost and application requirements.

The output capacitance will be determined by the ripple voltage requirement. Voltage mode COT topology can work with very small values of capacitor ESR.

The following equations are used to calculate the size needed to meet a transient load response:

$$I_{LPK} = I_{max.} + 0.5 \times I_{RIPPLE\_max.}$$

and

$$C_{OUT\_min.} = I_{LPK} \times \frac{L \times \frac{I_{LPK}^2}{V_{OUT}} - \frac{I_{max}^2 \times dt}{dI_{LOAD}}}{2 \times (V_{PK} - V_{OUT})}$$

Where I_{LPK} is the peak inductor current, $I_{MAX.}$ is the maximum output current, dI_{LOAD} is the current step in µs and V_{PK} is the peak voltage, the output voltage summed with the specified over and under shoot.

In case high ESR electrolytic capacitors are used, it is good practice to also include low ESR ceramic capacitors in parallel with the high ESR bulk capacitance to improve output ripple and transient response. A good starting point is to use a 10 µF output capacitor.

Care must be taken to account for voltage derating of the capacitance when choosing an all ceramic output capacitance.

Enable Pin Voltage

The EN pin has an internal pull down resistor and only requires an enable voltage. This needs to be greater than 1.4 V. An input voltage or a resistor connected across V_{IN} and EN can be used. The internal pull down resistance is 5 MΩ.

Input Capacitance

In order to determine the minimum capacitance the input voltage ripple needs to be specified; $V_{CINPP} \leq 500$ mV is a suitable starting point. This magnitude is determined by the final application specification. The input current needs to be determined for the lowest operating input voltage,

$$I_{CIN(RMS)} = I_O \times \sqrt{D \times (1-D) + \frac{1}{12} \times \left(\frac{V_{OUT}}{L \times f_{sw} \times I_{OUT}}\right)^2 \times (1-D)^2 \times D}$$

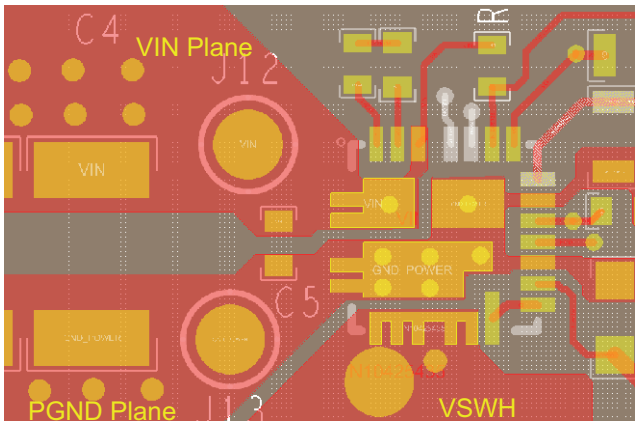
The minimum input capacitance can then be found,

$$C_{IN\_min.} = I_{OUT} \times \frac{D - (1 - D)}{V_{CINPKPK} \times f_{sw}}$$

If high ESR capacitors are used, it is good practice to also add low ESR ceramic capacitance. A 4.7 µF ceramic input capacitance is a suitable starting point.
Care must be taken to account for voltage derating of the capacitance when choosing an all ceramic input capacitance.

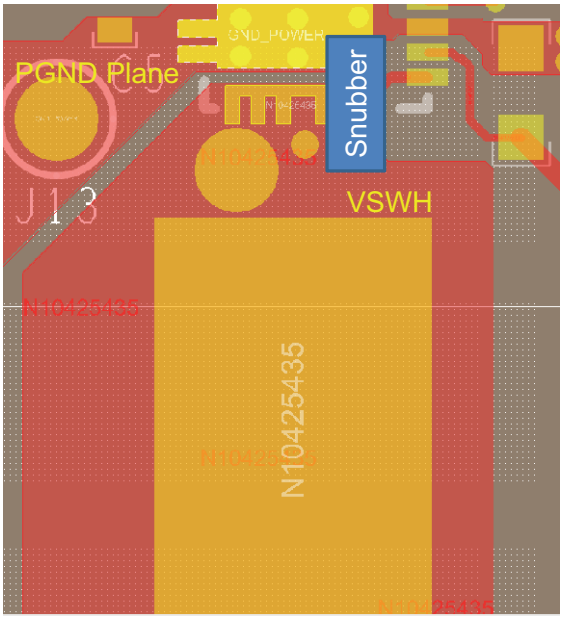
PCB LAYOUT RECOMMENDATIONS

Step 1: V_{IN}/GND Planes and Decoupling



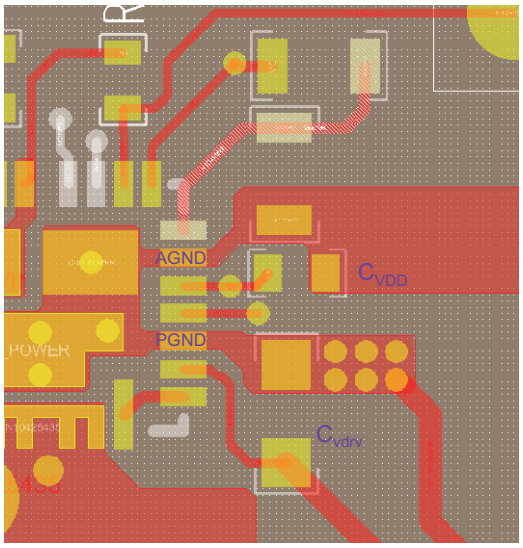
1. Layout V_{IN} and P_{GND} planes as shown above
2. Ceramic capacitors should be placed right between V_{IN} and P_{GND}, and very close to the device for best decoupling effect
3. Different values / packages of ceramic capacitors should be used to cover entire decoupling spectrum e.g. 1210 and 0603
4. Smaller capacitance value, closer to device V_{IN} pin(s), provide better high frequency response

Step 2: V_{SWH} Plane



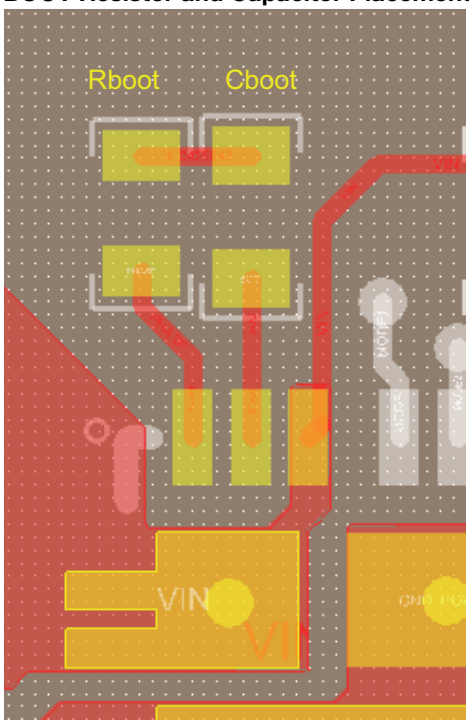
1. Connect output inductor to SiC431 with large plane to lower the resistance
2. If any snubber network is required, place the components on the bottom side as shown above

Step 3: V_{DD}/V_{DRV} Input Filter



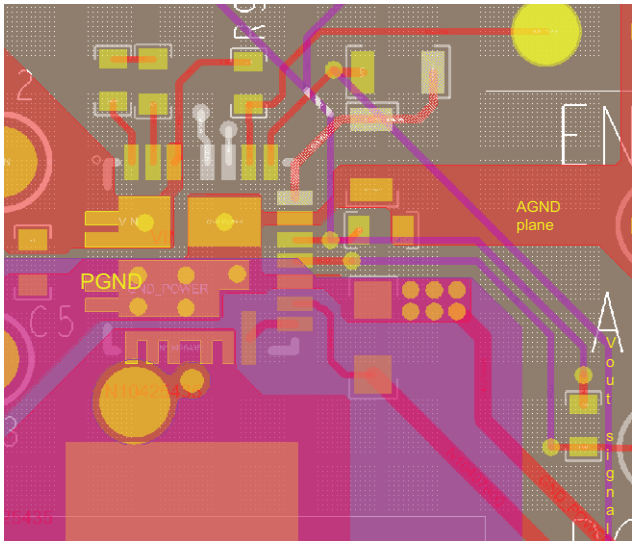
1. C_{VDD} cap should be placed between pin 15 and pin 16 (the A_{GND} of driver IC) to achieve best noise filtering
2. C_{VDRV} cap should be placed close to V_{DRV} (pin12) and P_{GND} (pin13) to reduce effects of trace impedance and provide maximum instantaneous driver current for low side MOSFET during switching cycle

Step 4: BOOT Resistor and Capacitor Placement



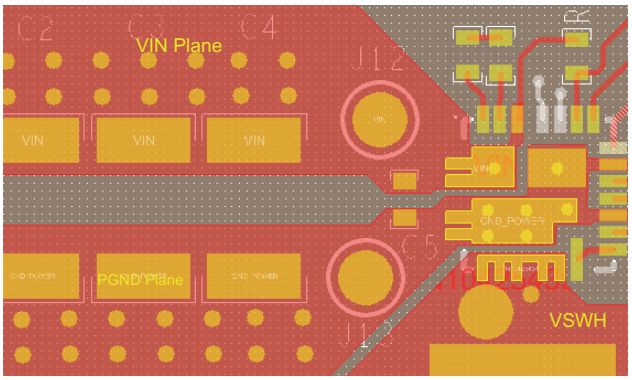
1. These components need to be placed very close to SiC431, right between PHASE (pin 24) and BOOT (pin 23)
2. In order to reduce parasitic inductance, it is recommended to use 0402 chip size for the resistor and the capacitor.

Step 5: Signal Routing



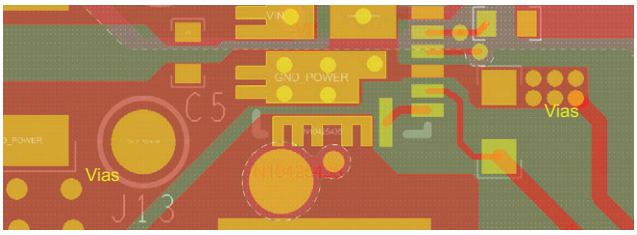
1. Separate the small analog signal from high current path. As shown above, the high paths with high dv/dt, di/dt are placed on the left side of the IC, while the small control signals are placed on the right side of the IC. All the components for small analog signal should be placed closer to IC with minimum trace length
2. Pin16 is considered as IC analog ground, which should have single connection to power ground. The A_{GND} ground plane connected with pin16 helps to keep A_{GND} quite and improve noise immunity
3. The output signal can be routed through inner layer. Make sure this signal is far away from V_{SWH} node and shielded by an inner ground layer

Step 6: Thermal Management



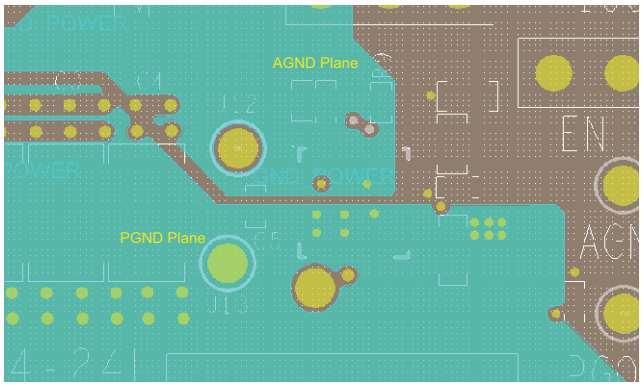
1. Thermal relief vias can be added on the V_{IN} and P_{GND} pads to utilize inner layers for high current and thermal dissipation
2. To achieve better thermal performance, additional vias can be put on V_{IN} and P_{GND} plane. It's also necessary to duplicate the V_{IN} and ground plane at bottom layer to maximize the power dissipation capability from PCB
3. V_{SWH} pad is a noise source and not recommended to put vias on this pad
4. 8 mil drill for pads and 10 mils drill for plane can be the optional via size. The vias on pad may drain solder during assembly and cause assembly issue. Please consult with the assembly house for guideline

Step 7: Ground Connection



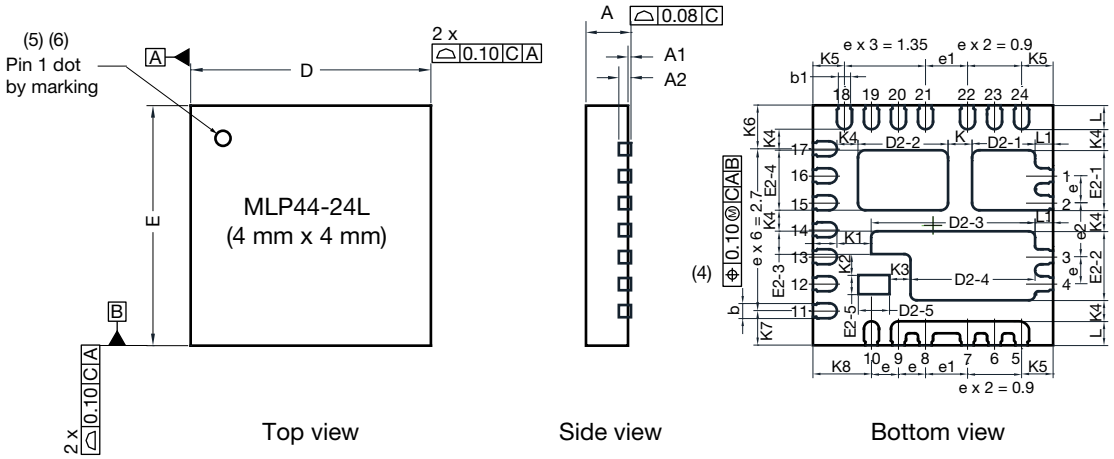
1. In order to minimize the ground voltage drop due to high current, it is recommended to put vias on the both side of the IC of the P_{GND} pin. Make use of the inner ground layers to lower the impedance

Step 7: Ground Layer



1. It is recommended to make the whole inner 1 layer (next to top layer) ground plane
2. This ground plane provides shielding between noise source on top layer and signal trace within inner layer
3. The Ground plane can be broken into two section as P_{GND} and A_{GND}

PACKAGE OUTLINE DRAWING PowerPAK® MLP44-24L



Top view Side view Bottom view

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A [8]	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 ref.			0.008 ref.	
b [4]	0.20	0.25	0.30	0.008	0.010	0.012
b1	0.15	0.20	0.25	0.006	0.008	0.010
D	3.90	4.00	4.10	0.155	0.157	0.159
e		0.45 BSC			0.018 BSC	
e1		0.70 BSC			0.028 BSC	
e2		0.90 BSC			0.035 BSC	
E	3.90	4.00	4.10	0.155	0.157	0.159
L	0.35	0.40	0.45	0.014	0.016	0.018
N [3]		24			24	
D2-1	1.00	1.05	1.10	0.039	0.041	0.043
D2-2	1.45	1.50	1.55	0.057	0.059	0.061
D2-3	2.68	2.73	2.78	0.106	0.108	0.110
D2-4	2.02	2.07	2.12	0.079	0.081	0.083
D2-5	0.47	0.52	0.57	0.018	0.020	0.022
E2-1	0.95	1.00	1.05	0.037	0.039	0.041
E2-2	1.10	1.15	1.20	0.043	0.045	0.047
E2-3	0.33	0.38	0.43	0.013	0.015	0.017
E2-4	0.95	1.00	1.05	0.037	0.039	0.041
E2-5	0.27	0.32	0.37	0.011	0.013	0.015
K		0.40 ref.			0.016 ref.	
K1		0.57 ref.			0.022 ref.	
K2		0.35 ref.			0.014 ref.	
K3		0.35 ref.			0.014 ref.	
K4		0.35 ref.			0.014 ref.	
K5		0.525 ref.			0.021 ref.	
K6		0.725 ref.			0.029 ref.	
K7		0.575 ref.			0.023 ref.	
K8		0.975 ref.			0.038 ref.	

Notes

(1) Use millimeters as the primary measurement
(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994
(3) N is the number of terminals
(4) Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
(5) The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
(6) Exact shape and size of this feature is optional
(7) Package warpage max. 0.08 mm
(8) Applied only for terminals

PRODUCT SUMMARY				
Part number	SiC431A	SiC431B	SiC431C	SiC431D
Description	24 A, 4.5 V to 24 V input, 300 kHz, 500 kHz, 750 kHz, 1 MHz, synchronous buck regulator with ultrasonic mode and internal 5 V bias	24 A, 4.5 V to 24 V input, 300 kHz, 500 kHz, 750 kHz, 1 MHz, synchronous buck regulator with power save mode and internal 5 V bias	24 A, 3 V to 24 V input, 300 kHz, 500 kHz, 750 kHz, 1 MHz, synchronous buck regulator with power save mode and internal 5 V bias	24 A, 3 V to 24 V input, 300 kHz, 500 kHz, 750 kHz, 1 MHz, synchronous buck regulator with power save mode and internal 5 V bias
Input voltage min. (V)	4.5	4.5	3.0	3.0
Input voltage max. (V)	24	24	24	24
Output voltage min. (V)	0.6	0.6	0.6	0.6
Output voltage max. (V)	0.90 x V_{IN}	0.90 x V_{IN}	0.90 x V_{IN}	0.90 x V_{IN}
Continuous current (A)	24	24	24	24
Switch frequency min. (kHz)	300	300	300	300
Switch frequency max. (kHz)	1000	1000	1000	1000
Pre-bias operation (yes / no)	Y	Y	Y	Y
Internal bias reg. (yes / no)	Y	Y	N	N
Compensation	Internal	Internal	Internal	Internal
Enable (yes / no)	Y	Y	Y	Y
P_{GOOD} (yes / no)	Y	Y	Y	Y
Over current protection	Y	Y	Y	Y
Protection	OVP, OCP, UVP/SCP, OTP, UVLO	OVP, OCP, UVP/SCP, OTP, UVLO	OVP, OCP, UVP/SCP, OTP, UVLO	OVP, OCP, UVP/SCP, OTP, UVLO
Light load mode	Selectable ultrasonic	Selectable powersave	Selectable ultrasonic	Selectable powersave
Peak efficiency (%)	97	97	97	97
Package type	PowerPAK MLP 44-24L	PowerPAK MLP 44-24L	PowerPAK MLP 44-24L	PowerPAK MLP 44-24L
Package size (W, L, H) (mm)	4 x 4 x 0.75	4 x 4 x 0.75	4 x 4 x 0.75	4 x 4 x 0.75
Status code	1	1	1	1
Product type	microBUCK (step down regulator)	microBUCK (step down regulator)	microBUCK (step down regulator)	microBUCK (step down regulator)
Applications	Computers, consumer, industrial, healthcare, networking	Computers, consumer, industrial, healthcare, networking	Computers, consumer, industrial, healthcare, networking	Computers, consumer, industrial, healthcare, networking

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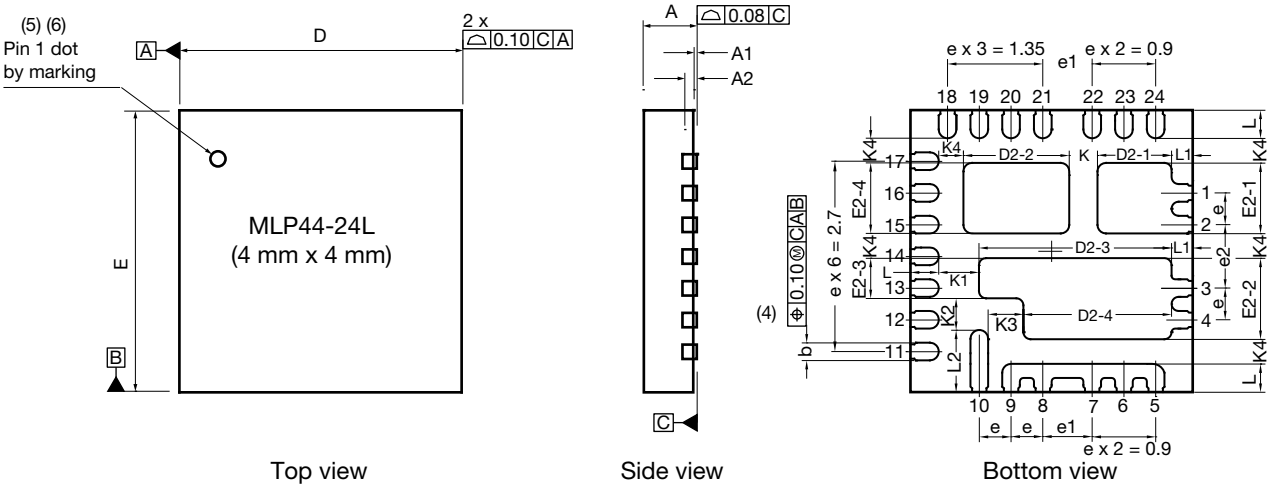
PowerPAK® MLP44-24L Case Outline



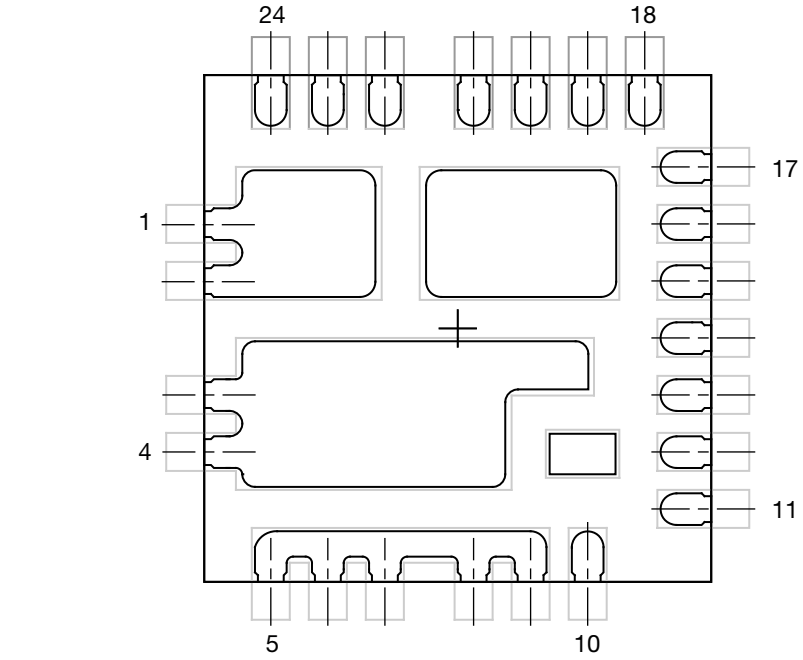
Top view Side view Bottom view

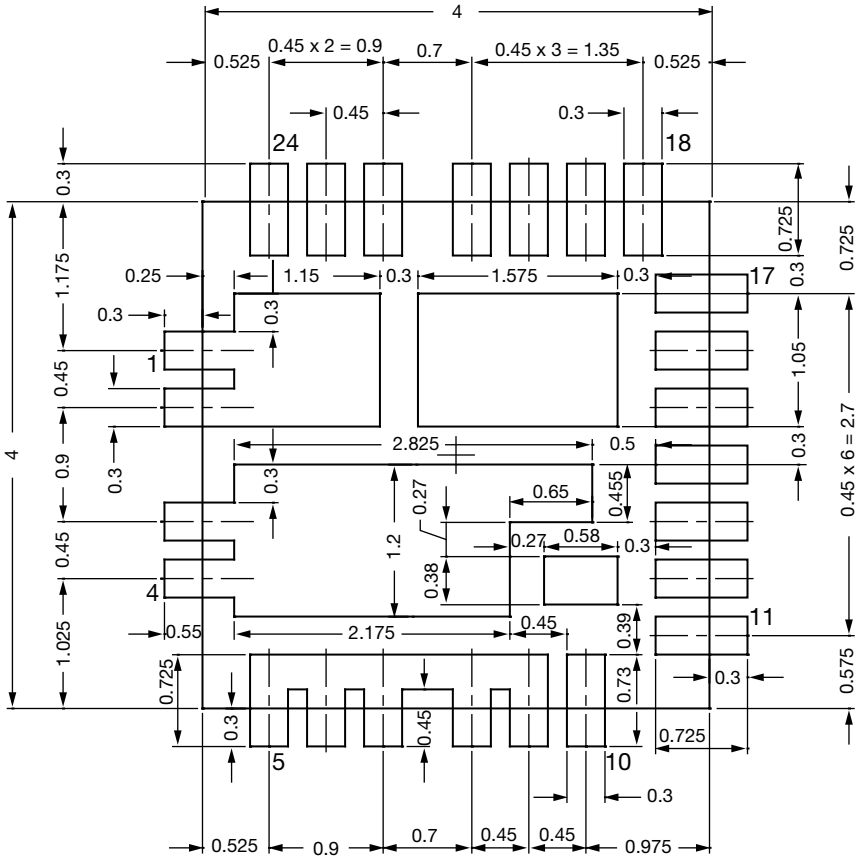
DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A [8]	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 ref.			0.008 ref.	
b [4]	0.20	0.25	0.30	0.078	0.098	0.110
D	3.90	4.00	4.10	0.155	0.157	0.159
e		0.45 BSC			0.018 BSC	
e1		0.70 BSC			0.028 BSC	
e2		0.90 BSC			0.035 BSC	
E	3.90	4.00	4.10	0.155	0.157	0.159
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.25	0.30	0.35	0.010	0.012	0.014
L2	0.83	0.88	0.93	0.033	0.035	0.037
N [3]		24			24	
D2-1	1.00	1.05	1.10	0.039	0.041	0.043
D2-2	1.45	1.50	1.55	0.057	0.059	0.061
D2-3	2.68	2.73	2.78	0.106	0.108	0.110
D2-4	2.05	2.10	2.15	0.081	0.083	0.085
E2-1	0.95	1.00	1.05	0.037	0.039	0.041
E2-2	1.10	1.15	1.20	0.043	0.045	0.047
E2-3	0.52	0.57	0.62	0.020	0.022	0.024
E2-4	0.95	1.00	1.05	0.037	0.039	0.041
K		0.40 ref.			0.016 ref.	
K1		0.57 ref.			0.022 ref.	
K2		0.45 ref.			0.018 ref.	
K3		0.50 ref.			0.020 ref.	
K4		0.35 ref.			0.014 ref.	
ECN: T16-0945-Rev. A, 19-Dec-16 DWG: 6055						

Notes

(1) Use millimeters as the primary measurement
(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994
(3) N is the number of terminals
(4) Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
(5) The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
(6) Exact shape and size of this feature is optional
(7) Package warpage max. 0.08 mm
(8) Applied only for terminals

Recommended Land Pattern PowerPAK® MLP44-24L





All dimensions are in millimeters

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