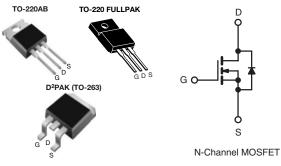


Vishay Siliconix

Power MOSFET

PRODUCT SUMMARY				
V _{DS} (V) at T _J max.	560 V			
R _{DS(on)} (Ω)	$V_{GS} = 10 V$	0.555		
Q _g (Max.) (nC)	48			
Q _{gs} (nC)	12			
Q _{gd} (nC)	15			
Configuration	Single			



FEATURES

- Low Figure-of-Merit Ron x Qg
- 100 % Avalanche Tested
- Gate Charge Improved
- T_{rr}/Q_{rr} Improved
- Compliant to RoHS Directive 2002/95/EC



ORDERING INFORMATION				
Package	TO-220AB	D ² PAK (TO-263)	TO-220 FULLPAK	
Lead (Pb)-free	SiHP12N50C-E3	SiHB12N50C-E3	SiHF12N50C-E3	

ABSOLUTE MAXIMUM RATINGS ($T_C = 25 \text{ °C}$, unless otherwise				LIMIT		
PARAMETER			SYMBOL	TO220-AB D ² PAK (TO-263)	TO-220 FULLPAK	UNIT
Drain-Source Voltage			V _{DS}	500		v
Gate-Source Voltage			V _{GS}	± 30		v
Continuous Drain Current (T, = 150 °C) ^a	V _{GS} at 10 V	T _C = 25 °C	1	12		
Continuous Drain Current (1) = 150°C)*	VGS at TU V	T _C = 100 °C	I _D	7.5	5	А
Pulsed Drain Current ^c			I _{DM}	28		
Linear Derating Factor				1.67	0.28	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	180		mJ
Maximum Power Dissipation			PD	208	36	W
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150		*0
Soldering Recommendations (Peak Temperature) ^d for 10 s				300		°C

Notes

a. Limited by maximum junction temperature.

b. $V_{DD} = 50$ V, starting $T_J = 25$ °C, L = 2.5 mH, $R_g = 25 \Omega$, $I_{AS} = 12$ A.

c. Repetitive rating; pulse width limited by maximum junction temperature.

d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

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THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TO220-AB D ² PAK (TO-263)	TO-220 FULLPAK	UNIT	
Maximum Junction-to-Ambient	R _{thJA}	62	65		
Maximum Junction-to-Case (Drain)	R _{thJC}	0.6	3.5	°C/W	
Junction-to-Ambient (PCB mount) ^a	R _{thJA}	40	-		

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static		1			<u> </u>	I	
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0	V, I _D = 250 μA	500	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference t	o 25 °C, I _D = 1 mA	-	0.6	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	$V_{DS} = V$	_{GS} , I _D = 250 μΑ	3.0	-	5.0	V
Gate-Source Leakage	I _{GSS}	VG	_S = ± 30 V	-	-	± 100	nA
Zaro Cata Valtago Drain Current	1	V _{DS} = 50	00 V, V _{GS} = 0 V	-	-	50	
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 400 V, V	∕ _{GS} = 0 V, T _J = 125 °C	-	-	250	μA
Drain-Source On-State Resistance	R _{DS(on)}	$V_{GS} = 10 V$	I _D = 4 A	-	0.46	0.555	Ω
Forward Transconductance	9 _{fs}	V _{DS} =	50 V, I _D = 3 A	-	3	-	S
Dynamic							
Input Capacitance	C _{iss}	$V_{GS} = 0 V$,		-	1375	-	
Output Capacitance	C _{oss}	V	_{DS} = 25 V,	-	165	-	pF
Reverse Transfer Capacitance	C _{rss}	f = 1.0 MHz		-	17	-	1
Total Gate Charge	Qg			-	32	48	
Gate-Source Charge	Q_gs	$V_{GS} = 10 V$	$V_{GS} = 10 \text{ V}$ $I_D = 10 \text{ A}, V_{DS} = 400 \text{ V}$		12	-	nC
Gate-Drain Charge	Q_{gd}			-	15	-	
Turn-On Delay Time	t _{d(on)}	$V_{DD} = 250 \text{ V}, \text{ I}_{D} = 10 \text{ A} \\ \text{R}_{g} = 4.3 \ \Omega, \text{ V}_{\text{GS}} = 10 \text{ V}$		-	18	-	- ns
Rise Time	t _r			-	35	-	
Turn-Off Delay Time	t _{d(off)}			-	23	-	
Fall Time	t _f			-	6	-	
Gate Input Resistance	R _g	f = 1 MHz, open drain		-	1.1	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	12	А
Pulsed Diode Forward Current	I _{SM}			-	-	28	
Body Diode Voltage	V_{SD}	$T_{J} = 25 \text{ °C}, I_{S} = 10 \text{ A}, V_{GS} = 0 \text{ V}$		-	-	1.8	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = I _S , dl/dt = 100 A/µs, V _R = 20 V		-	580	-	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	4.3	-	μC
Body Diode Reverse Recovery Current	I _{RRM}			-	13	-	Α

Note

• The information shown here is a preliminary product proposal, not a commercial product data sheet. Vishay Siliconix is not committed to produce this or any similar product. This information should not be used for design purposes, nor construed as an offer to furnish or sell such products.



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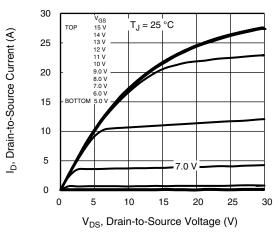


Fig. 1 - Typical Output Characteristics (TO-220)

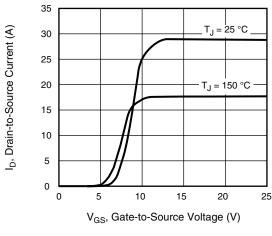


Fig. 3 - Typical Transfer Characteristics

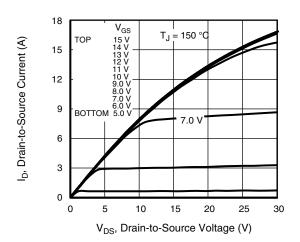


Fig. 2 - Typical Output Characteristics (TO-220)

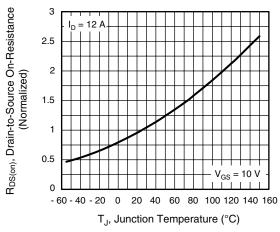


Fig. 4 - Normalized On-Resistance vs. Temperature

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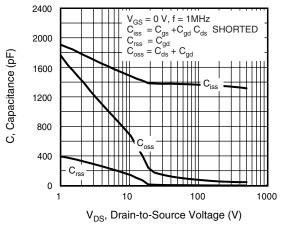


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

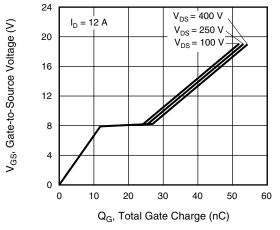


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

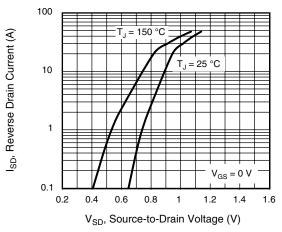
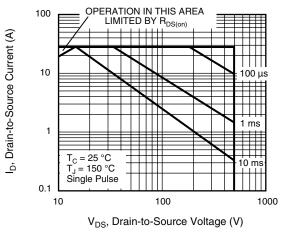
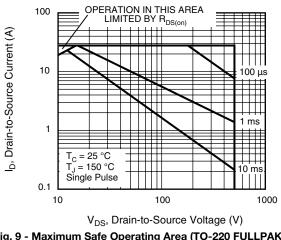


Fig. 7 - Typical Source-Drain Diode Forward Voltage











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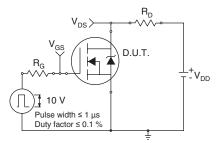
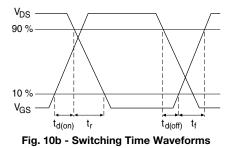
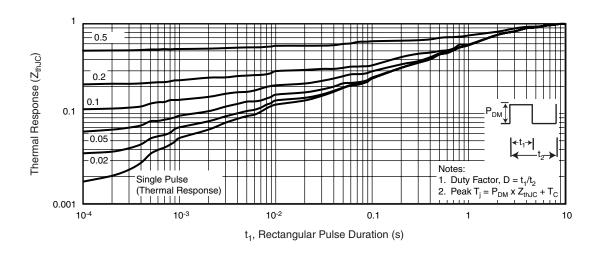


Fig. 10a - Switching Time Test Circuit



1 0.5 Thermal Response (Z_{thJC}) 0.1 0.05 0.1 P_{DM} Single Pulse (Thermal Response) 0.02 \square Notes: 1. Duty Factor, $D = t_1/t_2$ 2. Peak $T_j = P_{DM} \times Z_{thJC} +$ Т 0.001 10-4 10⁻³ 10⁻² 0.1 1 t₁, Rectangular Pulse Duration (s)

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-220AB, D²PAK)





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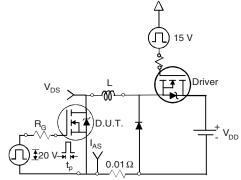
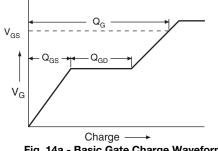


Fig. 13a - Unclamped Inductive Test Circuit





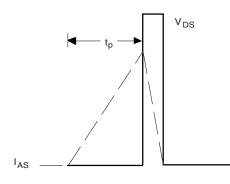


Fig. 13b - Unclamped Inductive Waveforms

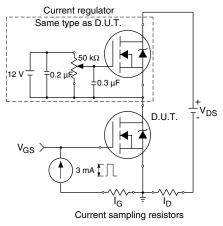
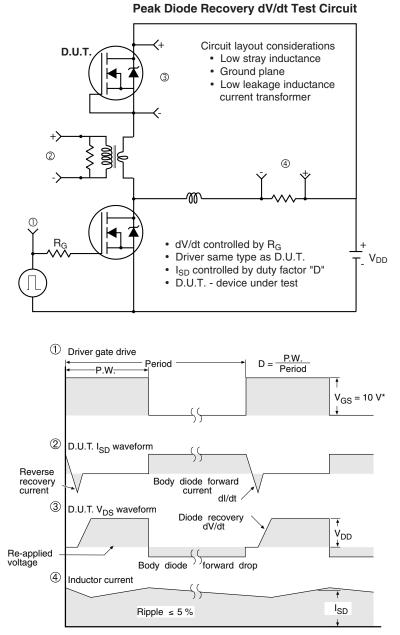


Fig. 14b - Gate Charge Test Circuit



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* $V_{GS} = 5$ V for logic level devices

Fig. 15 - For N-Channel

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www.vishay.com

TO-220-1



DIM.	MILLIN	IETERS	INCHES		
DIN.	MIN.	MAX.	MIN.	MAX.	
А	4.24	4.65	0.167	0.183	
b	0.69	1.02	0.027	0.040	
b(1)	1.14	1.78	0.045	0.070	
С	0.36	0.61	0.014	0.024	
D	14.33	15.85	0.564	0.624	
E	9.96	10.52	0.392	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.10	6.71	0.240	0.264	
J(1)	2.41	2.92	0.095	0.115	
L	13.36	14.40	0.526	0.567	
L(1)	3.33	4.04	0.131	0.159	
ØР	3.53	3.94	0.139	0.155	
Q	2.54	3.00	0.100	0.118	
ECN: X15-0364-Rev. C, 14-Dec-15 DWG: 6031					

Note

- M^{\star} = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

Package Picture					
AS	ASE		Xi'an		
		IRF 9510 744K AB			

Revison: 14-Dec-15

1 For technical questions, contact: <u>hvm@vishay.com</u> Document Number: 66542

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RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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