

Vishay Siliconix

# 6.5 m $\Omega$ , Bi-Directional Battery Switch in Compact WCSP

### DESCRIPTION

The SiP32101, SiP32102, and SiP32103 bidirectional switches feature reverse blocking capability to isolate the battery from the system. The internal switch has an ultra-low 6.5 m $\Omega$  (typ at 3.3 V) on-resistance and operates from a +2.3 V to +5.5 V input voltage range, making the devices ideal battery-disconnect switches for high-capacity battery applications.

The SiP32101, SiP32102, and SiP32103 have slew rate control, making them ideal in large load capacitor as well as high-current load switching applications. These devices are also highly efficient, consuming a mere 10 pA (typ.) current in shutdown and 15 pA while operating.

The SiP32101 and SiP32103 have an active low enable and the SiP32102 has an active high enable. They can interface directly with a low voltage control signal.

The SiP32101, SiP32102, and SiP32103 are available in an ultra compact 12-Bump, 1.3 mm x 1.7 mm, 0.4 mm pitch WCSP package with top side lamination. The device operates over the temperature of -40  $^{\circ}$ C to +85  $^{\circ}$ C.

### FEATURES

- Bi-directional ON and OFF
- 7 A continuous current capability
- Ultra low  $R_{on}$ , 6.5 m $\Omega$  (typ.) at 3.3 V
- Wide input voltage, 2.3 V to 5.5 V
- Slew rate controlled turn on
- Ultra-low quiescent current: 15 pA (SiP32101, SiP32102)
- EN pin with integrated pull up or pull down resistor
- Available in both logic high and logic low enable options
- Compact 12-Bump, 1.3 mm x 1.7 mm x 0.55 mm WCSP package
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

### APPLICATIONS

- Smartphones and tablets
- Digital still / video cameras
- Portable meters and test instruments
- · Communication devices with embedded batteries
- Portable medical and healthcare systems
- Data storage
- Battery bank



#### Fig. 1 - Typical Application Circuit

ORDERING INFORMATION							
PART NUMBER	MARKING	ENABLE	ENABLE PULL RESISTOR	PACKAGE	TEMPERATURE		
SiP32101DB-T1-GE1	32101	Low enable	Pull Low				
SiP32102DB-T1-GE1	32102	High enable	Pull Low	12-Bump, 1.3 mm x 1.7 mm,	40 °C to 185 °C		
SiP32102DB-T5-GE1	32102	High enable	Pull Low	WCSP package	-40 0 10 +85 0		
SiP32103DB-T1-GE1	32103	Low enable	Pull High				
SiP32101EVB	-	-	-		-		
SiP32102EVB	-	-	-	Evaluation Board	-		
SiP32103EVB	-	-	-		-		

#### Note

GE1 denotes halogen-free and RoHS-compliant

### MARKING



S15-0598-Rev. G, 30-Mar-15

1 For technical questions, contact: <u>powerictechsupport@vishay.com</u> Document Number: 62617

Pb-free RoHS

**TYPICAL APPLICATION CIRCUIT** 





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ABSOLUTE MAXIMUM RATINGS					
PARAMETER	CONDITIONS	LIMIT	UNIT		
N N	Reference to GND	-0.3 to +6			
VPA, VPB	Pulse at 1 ms reference to GND <sup>a</sup>	-1.6	V		
V <sub>EN</sub>	Reference to GND	-0.3 to +6			
Maximum Continuous Switch Current		7	^		
Maximum Pulse Current	100 µs pulse	15	A		
ESD (HBM)		8000	V		
Operating Temperature		-40 to +85			
Operating Junction Temperature		125	°C		
Storage Temperature		-65 to +150			
Thermal Resistance $(\theta_{JA})^{b}$		73	°C/W		
Power Dissipation (P <sub>D</sub> ) <sup>b, c</sup>	T <sub>A</sub> = 70 °C	1096	mW		

#### Notes

a. Negative current injection up to 300 mA.

b. All bumps soldered to 1 inch x 1 inch, 2 oz. copper, 4 layers PC board.

c. Derate 13.7 mW/°C above  $T_A = 70$  °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

SPECIFICATIONS								
		TEST CONDITIONS UNLESS SPECIFIED	LIMITS					
PARAMETER	SYMBOL	$ \begin{array}{l} V_{IN} = V_{PA}/V_{PB} = 2.3 \ V \ to \ 5.5 \ V, \ T_A = -40 \ ^\circ C \ to \ 85 \ ^\circ C \\ (Typical \ values \ are \ at \ V_{PA}, \ V_{PB} = 4.2 \ V, \\ C_{PA}, \ C_{PB} = 0.1 \ \mu F, \ T_A = 25 \ ^\circ C) \end{array} $	MIN.ª	TYP. <sup>b</sup>	MAX.ª	UNIT		
Power Supply								
Operating Voltage <sup>c</sup>	V <sub>PA/PB</sub>		2.3	-	5.5	V		
Quiescent Current	Ι <sub>Q</sub>		-	0.015	300	nA		
		$V_{\overline{EN}} = 0 V$ (for SiP32103), no load		8.2	15	μA		
Shutdown Current	I <sub>SHDN</sub>		-	0.010	300	nA		
Internal FET	Internal FET							
On Resistance	R <sub>DS(on)</sub>	$V_{PA}/V_{PB}$ = 2.3 V, I <sub>L</sub> = 500 mA, T <sub>A</sub> = 25 °C	-	8	13	mQ		
On-nesistance		$V_{PA}/V_{PB} = 3.3 \text{ V}, \text{ I}_{L} = 500 \text{ mA}, \text{ T}_{A} = 25 \text{ °C}$ - 6.5 10				11122		
Control								
EN / EN Input Logic-Low Voltage <sup>c</sup>	V <sub>IL</sub>		-	-	0.4	V		
EN / EN Input Logic-High Voltage c	VIH		1.4	-	-	v		
EN / EN Pull Resistor	R <sub>EN</sub>	$V_{PA}/V_{PB}$ = 5.5 V, $V_{\overline{EN}}$ (or $V_{EN})$ = 2.3 V	-	500	700	kΩ		
Timing								
Output Turn-On Delay Time	t <sub>d(on)</sub>		-	0.5	-			
Output Turn-On Rise Time	t <sub>r</sub>	$V_{\rm ev} = 4.2 \text{ V}$ B <sub>c</sub> = 100 O C <sub>c</sub> = 0.1 µE T <sub>c</sub> = 25 °C	-	1	-	ms		
Output Turn-Off Delay Time t <sub>d(off)</sub>		$v_{IN} = 4.2$ $v_{1}$ $H_{L} = 100$ $22$ , $O_{L} = 0.1$ $\mu$ $H_{A} = 20$ $O_{L}$	-	2.4	-			
Output Turn-Off Fall Time	t <sub>f</sub>		-	1	-			

#### Notes

a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.

b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

c. For V<sub>IN</sub> outside this range consult typical EN, EN threshold curve.

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### **BUMP CONFIGURATION**



Top view (solder bumps on bottom)

Fig. 2 - WCSP12, 1.3 mm x 1.7 mm

BUMP DESCRIPTION				
BUMP NUMBER	NAME	FUNCTION		
A1, B1, A3, B3, C3	PB	Power port B		
C1	GND	Ground		
A2, B2, C2, B4, C4	PA	Power port A		
A4	ĒN / EN	Switch enable input, active low for SiP32101 and SiP32103, active high for SiP32102		

### FUNCTIONAL BLOCK DIAGRAM





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# TYPICAL CHARACTERISTICS (internally regulated 25 °C, unless otherwise noted)



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### TYPICAL CHARACTERISTICS (internally regulated 25 °C, unless otherwise noted)



Fig. 9 - Shutdown Current vs.Temperature









Fig. 12 - Normalized On Resistance vs. Load Current



Fig. 13 - Reverse Blocking Current (I<sub>RB</sub>) vs. Output Voltage



Fig. 14 - Rise Time vs. Temperature

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# TYPICAL CHARACTERISTICS (internally regulated 25 °C, unless otherwise noted)



Fig. 15 - EN, EN Threshold Voltage vs. Input Voltage



Fig. 16 - Turn-on Delay Time vs. Temperature



Fig. 17 - Turn-off Delay Time vs. Temperature



Fig. 18 - Fall Time vs. Temperature



#### **DETAILED DESCRIPTION**

The SiP32101, SiP32102, and SiP32103 bidirectional switches feature reverse blocking capability to isolate the battery from the system. The internal switch has an ultra-low 6.5 m $\Omega$  (typ. at 3.3 V) on-resistance and operates from a +2.3 V to +5.5 V input voltage range, making the device ideal battery-disconnect switch for high-capacity battery applications. The parts can handle 7 A continuous current at both directions.

The SiP32101, SiP32102, and SiP32103 have slew rate control, making them ideal in large load capacitor as well as high-current load switching applications.

The SiP32101, SiP32102, and SiP32103 are available in an ultra compact 12-Bump, 1.3 mm x 1.7 mm, 0.4 mm pitch WCSP package with top side lamination. The device operates over the temperature of -40  $^{\circ}$ C to +85  $^{\circ}$ C.

#### **REVERSE CURRENT BLOCKING**

The SiP32101, SiP32102, and SiP32103 are bidirectional switches that prevent current flowing from either port to the other when the device is disabled.

### EN, EN INPUT

SiP32101 and SiP32103 have an active-low enable pin which can interface with low voltage GPIO directly. The switch is on when EN is low and off when EN is high. The SiP32102 has an active-high enable pin that turns the switch on when high and off when low. The SiP32101 and SiP32102 have an integrated pull down resistor at EN pin. The SiP32103 EN pin integrates a pull up resistor that will automatically connected to either port A or port whichever is of higher voltage.

### SWITCH ON AND OFF PERFORMANCE

The SiP32101, SiP32102, and SiP32103 have slew rate control. This minimizes the inrush current and provides a soft turn on.





Fig. 20 - Port B Turn-Off Time (VPA = 4.2 V, RL = 10  $\Omega,$  CL = 0.1  $\mu\text{F})$ 

#### **DEVICE PIN OUT**

Device pin out is designed for ease of layout.



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?62617">www.vishay.com/ppg?62617</a>.

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# WCSP12: 12 Bumps

(3 x 4, 0.4 mm pitch, 208 µm bump height, 1.71 mm x 1.31 mm die size)



(NSMD)

	MILLIMETERS <sup>(5)</sup>			INCHES		
DIMENSION	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.515	0.530	0.545	0.0203	0.0209	0.0215
A1	0.183	0.208	0.233	0.0072	0.0082	0.0092
b	0.234	0.260	0.312	0.0092	0.0102	0.0123
е		0.400			0.0157	
S	0.235	0.255	0.275	0.0093	0.0100	0.0108
D	1.270	1.310	1.350	0.0500	0.0516	0.0531
E	1.670	1.710	1.750	0.0657	0.0673	0.0689

Notes (unless otherwise specified)

<sup>(1)</sup> Laser mark on the silicon die back coated with an epoxy film.

(2) Bumps are SAC396.

<sup>(3)</sup> 0.050 max. co-planarity.

<sup>(4)</sup> Laminate tape thickness is 0.022 mm.

<sup>(5)</sup> Use millimeters as the primary measurement.

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