

# SN74AVCH20T245

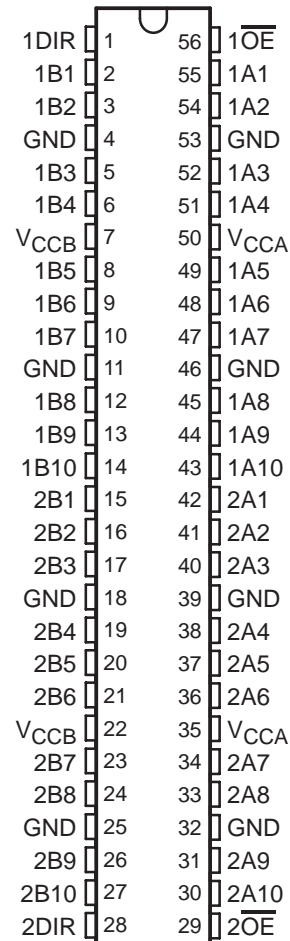
## 20-BIT DUAL-SUPPLY BUS TRANSCEIVER

### WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

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- Control Inputs  $V_{IH}/V_{IL}$  Levels are Referenced to  $V_{CCA}$  Voltage
- $V_{CC}$  Isolation Feature – If Either  $V_{CC}$  Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- I/Os Are 4.6-V Tolerant
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Max Data Rates
  - 380 Mbps (1.8-V to 3.3-V Translation)
  - 260 Mbps (< 1.8-V to 3.3-V Translation)
  - 260 Mbps (Translate to 2.5 V)
  - 210 Mbps (Translate to 1.8 V)
  - 120 Mbps (Translate to 1.5 V)
  - 100 Mbps (Translate to 1.2 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 8000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DGG OR DGV PACKAGE  
(TOP VIEW)



#### description/ordering information

This 20-bit noninverting bus transceiver uses two separate configurable power-supply rails. The SN74AVCH20T245 is optimized to operate with  $V_{CCA}/V_{CCB}$  set at 1.4 V to 3.6 V. It is operational with  $V_{CCA}/V_{CCB}$  as low as 1.2 V. The A port is designed to track  $V_{CCA}$ .  $V_{CCA}$  accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track  $V_{CCB}$ .  $V_{CCB}$  accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

#### ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74AVCH20T245GR	AVCH20T245
	TVSOP – DGV	Tape and reel	SN74AVCH20T245VR	WK245
	VFBGA – GQL	Tape and reel	SN74AVCH20T245KR	WK245
	VFBGA – ZQL (Pb-free)		74AVCH20T245ZQLR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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#### description/ordering information (continued)

The SN74AVCH20T245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the outputs so that the buses are effectively isolated.

The SN74AVCH20T245 is designed so that the control (1DIR, 2DIR,  $1\overline{OE}$ , and  $2\overline{OE}$ ) inputs are supplied by  $V_{CCA}$ .

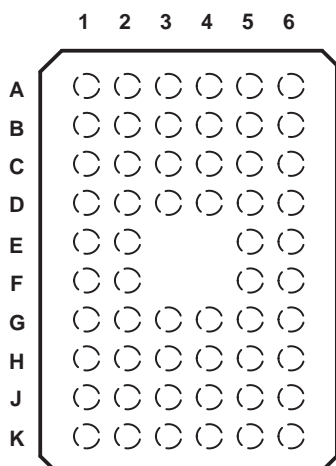
This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The  $V_{CC}$  isolation feature ensures that if either  $V_{CC}$  input is at GND, both outputs are in the high-impedance state. The bus-hold circuitry on the powered-up side always stays active.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

#### GQL OR ZQL PACKAGE (TOP VIEW)



#### terminal assignments

	1	2	3	4	5	6
A	1B1	1B2	1DIR	$1\overline{OE}$	1A2	1A1
B	1B3	1B4	GND	GND	1A4	1A3
C	1B5	1B6	$V_{CCB}$	$V_{CCA}$	1A6	1A5
D	1B7	1B8	GND	GND	1A8	1A7
E	1B9	1B10			1A10	1A9
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	$V_{CCB}$	$V_{CCA}$	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2B9	2B10	2DIR	$2\overline{OE}$	2A10	2A9

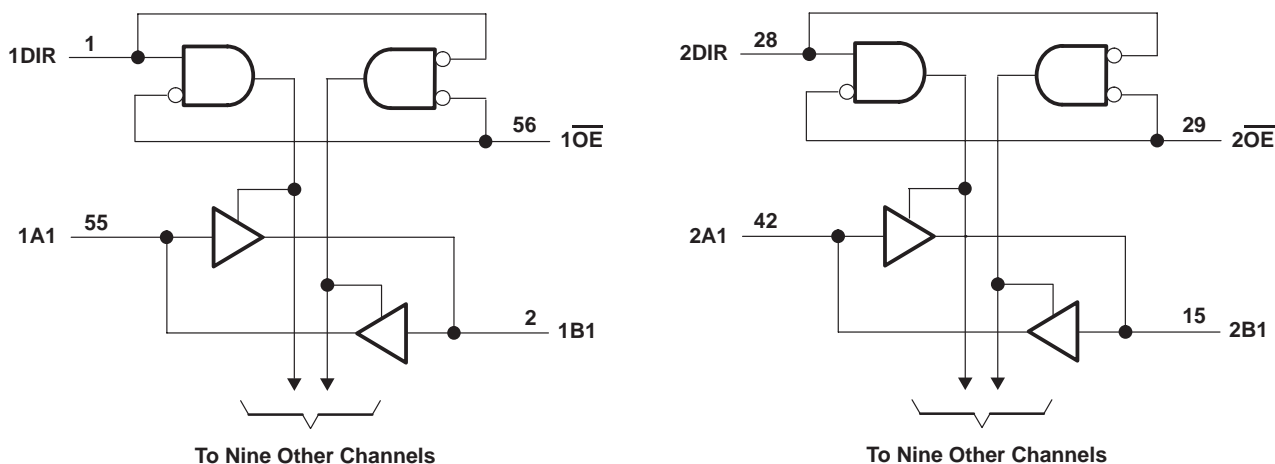
#### FUNCTION TABLE (each 10-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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**logic diagram (positive logic)**



Pin numbers shown are for the DGG and DGV packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CCA}$ and $V_{CCB}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1): I/O ports (A port) .....	-0.5 V to 4.6 V
I/O ports (B port) .....	-0.5 V to 4.6 V
Control inputs .....	-0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$	
(see Note 1): (A port) .....	-0.5 V to 4.6 V
(B port) .....	-0.5 V to 4.6 V
Voltage range applied to any output in the high or low state, $V_O$	
(see Notes 1 and 2): (A port) .....	-0.5 V to $V_{CCA} + 0.5$ V
(B port) .....	-0.5 V to $V_{CCB} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ .....	$\pm 50$ mA
Continuous current through each $V_{CCA}$ , $V_{CCB}$ , and GND .....	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package .....	64°C/W
DGV package .....	48°C/W
GQL/ZQL package .....	42°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.  
3. The package thermal impedance is calculated in accordance with JESD 51-7.

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#### recommended operating conditions (see Notes 4 through 8)

		V <sub>CCI</sub>	V <sub>CCO</sub>	MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage			1.2	3.6	V
V <sub>CCB</sub>	Supply voltage			1.2	3.6	V
V <sub>IH</sub>	High-level input voltage	Data inputs (see Note 7)	1.2 V to 1.95 V	V <sub>CCI</sub> × 0.65		V
			1.95 V to 2.7 V	1.6		
			2.7 V to 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	Data inputs (see Note 7)	1.2 V to 1.95 V	V <sub>CCI</sub> × 0.35		V
			1.95 V to 2.7 V	0.7		
			2.7 V to 3.6 V	0.8		
V <sub>IH</sub>	High-level input voltage	DIR (referenced to V <sub>CCA</sub> ) (see Note 8)	1.2 V to 1.95 V	V <sub>CCA</sub> × 0.65		V
			1.95 V to 2.7 V	1.6		
			2.7 V to 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	DIR (referenced to V <sub>CCA</sub> ) (see Note 8)	1.2 V to 1.95 V	V <sub>CCA</sub> × 0.35		V
			1.95 V to 2.7 V	0.7		
			2.7 V to 3.6 V	0.8		
V <sub>I</sub>	Input voltage			0	3.6	V
V <sub>O</sub>	Output voltage	Active state		0	V <sub>CCO</sub>	V
		3-state		0	3.6	V
I <sub>OH</sub>	High-level output current		1.2 V	-3		mA
			1.4 V to 1.6 V	-6		
			1.65 V to 1.95 V	-8		
			2.3 V to 2.7 V	-9		
			3 V to 3.6 V	-12		
I <sub>OL</sub>	Low-level output current		1.2 V	3		mA
			1.4 V to 1.6 V	6		
			1.65 V to 1.95 V	8		
			2.3 V to 2.7 V	9		
			3 V to 3.6 V	12		
Δt/Δv	Input transition rise or fall rate				5	ns/V
T <sub>A</sub>	Operating free-air temperature			-40	85	°C

- NOTES:
- V<sub>CCI</sub> is the V<sub>CC</sub> associated with the data input port.
  - V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.
  - All unused data inputs of the device must be held at V<sub>CCI</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
  - For V<sub>CCI</sub> values not specified in the data sheet, V<sub>IH(min)</sub> = V<sub>CCI</sub> × 0.7 V, V<sub>IL(max)</sub> = V<sub>CCI</sub> × 0.3 V.
  - For V<sub>CCB</sub> values not specified in the data sheet, V<sub>IH(min)</sub> = V<sub>CCB</sub> × 0.7 V, V<sub>IL(max)</sub> = V<sub>CCB</sub> × 0.3 V.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 9)

PARAMETER	TEST CONDITIONS		V <sub>CCA</sub>	V <sub>CCB</sub>	T <sub>A</sub> = 25°C			-40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	V <sub>I</sub> = V <sub>IH</sub>	1.2 V to 3.6 V	1.2 V to 3.6 V				V <sub>CCO</sub> - 0.2 V		V
	I <sub>OH</sub> = -3 mA		1.2 V	1.2 V	0.95					
	I <sub>OH</sub> = -6 mA		1.4 V	1.4 V				1.05		
	I <sub>OH</sub> = -8 mA		1.65 V	1.65 V				1.2		
	I <sub>OH</sub> = -9 mA		2.3 V	2.3 V				1.75		
	I <sub>OH</sub> = -12 mA		3 V	3 V				2.3		
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	V <sub>I</sub> = V <sub>IL</sub>	1.2 V to 3.6 V	1.2 V to 3.6 V				0.2		V
	I <sub>OL</sub> = 3 mA		1.2 V	1.2 V	0.15					
	I <sub>OL</sub> = 6 mA		1.4 V	1.4 V				0.35		
	I <sub>OL</sub> = 8 mA		1.65 V	1.65 V				0.45		
	I <sub>OL</sub> = 9 mA		2.3 V	2.3 V				0.55		
	I <sub>OL</sub> = 12 mA		3 V	3 V				0.7		
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CCA</sub> or GND	1.2 V to 3.6 V	1.2 V to 3.6 V	±0.025	±0.25	±1		μA	
I <sub>BHL</sub> <sup>†</sup>	V <sub>I</sub> = 0.42 V		1.2 V	1.2 V	25					μA
	V <sub>I</sub> = 0.49 V		1.4 V	1.4 V				15		
	V <sub>I</sub> = 0.58 V		1.65 V	1.65 V				25		
	V <sub>I</sub> = 0.7 V		2.3 V	2.3 V				45		
	V <sub>I</sub> = 0.8 V		3.3 V	3.3 V				100		
I <sub>BHH</sub> <sup>‡</sup>	V <sub>I</sub> = 0.78 V		1.2 V	1.2 V	-25					μA
	V <sub>I</sub> = 0.91 V		1.4 V	1.4 V				-15		
	V <sub>I</sub> = 1.07 V		1.65 V	1.65 V				-25		
	V <sub>I</sub> = 1.6 V		2.3 V	2.3 V				-45		
	V <sub>I</sub> = 2 V		3.3 V	3.3 V				-100		
I <sub>BHLO</sub> <sup>§</sup>	V <sub>I</sub> = 0 to V <sub>CC</sub>		1.2 V	1.2 V	50					μA
			1.6 V	1.6 V				125		
			1.95 V	1.95 V				200		
			2.7 V	2.7 V				300		
			3.6 V	3.6 V				500		
I <sub>BHHO</sub> <sup>¶</sup>	V <sub>I</sub> = 0 to V <sub>CC</sub>		1.2 V	1.2 V	-50					μA
			1.6 V	1.6 V				-125		
			1.95 V	1.95 V				-200		
			2.7 V	2.7 V				-300		
			3.6 V	3.6 V				-500		

<sup>†</sup> The bus-hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub> max. I<sub>BHL</sub> should be measured after lowering V<sub>IN</sub> to GND and then raising it to V<sub>IL</sub> max.

<sup>‡</sup> The bus-hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub> min. I<sub>BHH</sub> should be measured after raising V<sub>IN</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub> min.

<sup>§</sup> An external driver must source at least I<sub>BHLO</sub> to switch this node from low to high.

<sup>¶</sup> An external driver must sink at least I<sub>BHHO</sub> to switch this node from high to low.

NOTE 9: V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Notes 10 and 11) (continued)

PARAMETER		TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	T <sub>A</sub> = 25°C			-40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
I <sub>off</sub>	A port	V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6 V	0 V	0 to 3.6 V	±0.1	±1		±5	μA	
	B port		0 to 3.6 V	0 V	±0.1	±1		±5		
I <sub>OZ</sub> †	A or B ports	V <sub>O</sub> = V <sub>CCO</sub> or GND, V <sub>I</sub> = V <sub>CCI</sub> or GND	$\overline{OE} = V_{IH}$	3.6 V	3.6 V	±0.5	±2.5		±5	μA
	B port		$\overline{OE} =$ don't care	0 V	3.6 V				±5	
	A port			3.6 V	0 V				±5	
I <sub>CCA</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.2 V to 3.6 V	1.2 V to 3.6 V				35	μA	
			0 V	3.6 V				-5		
			3.6 V	0 V				35		
I <sub>CCB</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.2 V to 3.6 V	1.2 V to 3.6 V				35	μA	
			0 V	3.6 V				35		
			3.6 V	0 V				-5		
I <sub>CCA</sub> + I <sub>CCB</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.2 V to 3.6 V	1.2 V to 3.6 V				65	μA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3.3 V or GND	3.3 V	3.3 V		3.5			pF	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = 3.3 V or GND	3.3 V	3.3 V		7			pF	

† For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

NOTES: 10. V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

11. V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.

switching characteristics over recommended operating free-air temperature range,  
V<sub>CCA</sub> = 1.2 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.2 V	V <sub>CCB</sub> = 1.5 V	V <sub>CCB</sub> = 1.8 V	V <sub>CCB</sub> = 2.5 V	V <sub>CCB</sub> = 3.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
t <sub>PLH</sub>	A	B	3.8	3.1	2.8	2.7	3.3	ns
t <sub>PHL</sub>			3.8	3.1	2.8	2.7	3.3	
t <sub>PLH</sub>	B	A	4.1	3.8	3.6	3.5	3.4	ns
t <sub>PHL</sub>			4.1	3.8	3.6	3.5	3.4	
t <sub>PZH</sub>	$\overline{OE}$	A	6.5	6.5	6.5	6.5	6.5	ns
t <sub>PZL</sub>			6.5	6.5	6.5	6.5	6.5	
t <sub>PZH</sub>	$\overline{OE}$	B	5.6	4.4	3.8	3.3	3.2	ns
t <sub>PZL</sub>			5.6	4.4	3.8	3.3	3.2	
t <sub>PHZ</sub>	$\overline{OE}$	A	6.4	6.4	6.4	6.4	6.4	ns
t <sub>PLZ</sub>			6.4	6.4	6.4	6.4	6.4	
t <sub>PHZ</sub>	$\overline{OE}$	B	5.7	4.6	4.7	4.1	5.4	ns
t <sub>PLZ</sub>			5.7	4.6	4.7	4.1	5.4	



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switching characteristics over recommended operating free-air temperature range,  
 $V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$  (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	B	3.8	0.5	6.4	0.5	5.4	0.5	4.3	0.5	3.9	ns
t <sub>PHL</sub>			3.8	0.5	6.4	0.5	5.4	0.5	4.3	0.5	3.9	
t <sub>PLH</sub>	B	A	3.1	0.5	6.4	0.5	6.1	0.5	5.8	0.5	5.7	ns
t <sub>PHL</sub>			3.1	0.5	6.4	0.5	6.1	0.5	5.8	0.5	5.7	
t <sub>PZH</sub>	$\overline{\text{OE}}$	A	4.3	1.5	10.3	1.5	10.3	1.5	10.2	1.5	10.2	ns
t <sub>PZL</sub>			4.3	1.5	10.3	1.5	10.3	1.5	10.2	1.5	10.2	
t <sub>PZH</sub>	$\overline{\text{OE}}$	B	5.2	1	10.3	1	8.4	0.5	6.1	0.5	5.3	ns
t <sub>PZL</sub>			5.2	1	10.3	1	8.4	0.5	6.1	0.5	5.3	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	A	4.5	2	9	2	9	2	9	2	9	ns
t <sub>PLZ</sub>			4.5	2	9	2	9	2	9	2	9	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	B	5.1	1.5	9	1.5	7.8	1	6.4	1	5.9	ns
t <sub>PLZ</sub>			5.1	1.5	9	1.5	7.8	1	6.4	1	5.9	

switching characteristics over recommended operating free-air temperature range,  
 $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$  (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	B	3.6	0.5	6.1	0.5	5	0.5	3.9	0.5	3.5	ns
t <sub>PHL</sub>			3.6	0.5	6.1	0.5	5	0.5	3.9	0.5	3.5	
t <sub>PLH</sub>	B	A	2.8	0.5	5.4	0.5	5	0.5	4.7	0.5	4.6	ns
t <sub>PHL</sub>			2.8	0.5	5.4	0.5	5	0.5	4.7	0.5	4.6	
t <sub>PZH</sub>	$\overline{\text{OE}}$	A	3.4	1	8.1	1	7.9	1	7.9	1	7.9	ns
t <sub>PZL</sub>			3.4	1	8.1	1	7.9	1	7.9	1	7.9	
t <sub>PZH</sub>	$\overline{\text{OE}}$	B	5	0.5	10	0.5	7.9	0.5	5.7	0.5	4.8	ns
t <sub>PZL</sub>			5	0.5	10	0.5	7.9	0.5	5.7	0.5	4.8	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	A	4.1	2	7.4	2	7.4	2	7.4	2	7.4	ns
t <sub>PLZ</sub>			4.1	2	7.4	2	7.4	2	7.4	2	7.4	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	B	4.9	1.5	8.7	1.5	7.4	1	5.8	1	5.1	ns
t <sub>PLZ</sub>			4.9	1.5	8.7	1.5	7.4	1	5.8	1	5.1	



# SN74AVCH20T245

## 20-BIT DUAL-SUPPLY BUS TRANSCEIVER

### WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$  (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.2 V	V <sub>CCB</sub> = 1.5 V ± 0.1 V		V <sub>CCB</sub> = 1.8 V ± 0.15 V		V <sub>CCB</sub> = 2.5 V ± 0.2 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	B	3.5	0.5	5.8	0.5	4.7	0.5	3.5	0.5	3	ns
t <sub>PHL</sub>			3.5	0.5	5.8	0.5	4.7	0.5	3.5	0.5	3	
t <sub>PLH</sub>	B	A	2.7	0.5	4.3	0.5	3.9	0.5	3.5	0.5	3.4	ns
t <sub>PHL</sub>			2.7	0.5	4.3	0.5	3.9	0.5	3.5	0.5	3.4	
t <sub>PZH</sub>	$\overline{OE}$	A	2.5	0.5	5.4	0.5	5.3	0.5	5.2	0.5	5.2	ns
t <sub>PZL</sub>			2.5	0.5	5.4	0.5	5.3	0.5	5.2	0.5	5.2	
t <sub>PZH</sub>	$\overline{OE}$	B	4.8	0.5	9.6	0.5	7.6	0.5	5.3	0.5	4.3	ns
t <sub>PZL</sub>			4.8	0.5	9.6	0.5	7.6	0.5	5.3	0.5	4.3	
t <sub>PHZ</sub>	$\overline{OE}$	A	3	1.1	5.2	1.1	5.2	1.1	5.2	1.1	5.2	ns
t <sub>PLZ</sub>			3	1.1	5.2	1.1	5.2	1.1	5.2	1.1	5.2	
t <sub>PHZ</sub>	$\overline{OE}$	B	4.7	1.2	8.2	1.2	6.9	1	5.3	1	5	ns
t <sub>PLZ</sub>			4.7	1.2	8.2	1.2	6.9	1	5.3	1	5	

switching characteristics over recommended operating free-air temperature range,  
 $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$  (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.2 V	V <sub>CCB</sub> = 1.5 V ± 0.1 V		V <sub>CCB</sub> = 1.8 V ± 0.15 V		V <sub>CCB</sub> = 2.5 V ± 0.2 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	B	3.4	0.5	5.7	0.5	4.6	0.5	3.4	0.5	2.9	ns
t <sub>PHL</sub>			3.4	0.5	5.7	0.5	4.6	0.5	3.4	0.5	2.9	
t <sub>PLH</sub>	B	A	3.3	0.5	3.9	0.5	3.5	0.5	3	0.5	2.9	ns
t <sub>PHL</sub>			3.3	0.5	3.9	0.5	3.5	0.5	3	0.5	2.9	
t <sub>PZH</sub>	$\overline{OE}$	A	2.2	0.5	4.4	0.5	4.3	0.5	4.2	0.5	4.1	ns
t <sub>PZL</sub>			2.2	0.5	4.4	0.5	4.3	0.5	4.2	0.5	4.1	
t <sub>PZH</sub>	$\overline{OE}$	B	4.7	1	9.6	0.5	7.5	0.5	5.1	0.5	4.1	ns
t <sub>PZL</sub>			4.7	1	9.6	0.5	7.5	0.5	5.1	0.5	4.1	
t <sub>PHZ</sub>	$\overline{OE}$	A	3.4	0.8	5	0.8	5	0.8	5	0.8	5	ns
t <sub>PLZ</sub>			3.4	0.8	5	0.8	5	0.8	5	0.8	5	
t <sub>PHZ</sub>	$\overline{OE}$	B	4.6	1.2	8.1	1.2	6.7	1	5.1	0.8	5	ns
t <sub>PLZ</sub>			4.6	1.2	8.1	1.2	6.7	1	5.1	0.8	5	





**SN74AVCH20T245**  
**20-BIT DUAL-SUPPLY BUS TRANSCEIVER**  
**WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS**

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operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CCA} =$ $V_{CCB} = 1.2\text{ V}$	$V_{CCA} =$ $V_{CCB} = 1.5\text{ V}$	$V_{CCA} =$ $V_{CCB} = 1.8\text{ V}$	$V_{CCA} =$ $V_{CCB} = 2.5\text{ V}$	$V_{CCA} =$ $V_{CCB} = 3.3\text{ V}$	UNIT
				TYP	TYP	TYP	TYP	TYP	
$C_{pdA}^\dagger$	A to B	Outputs Enabled	$C_L = 0,$ $f = 10\text{ MHz},$ $t_r = t_f = 1\text{ ns}$	1	1	1	1	2	pF
		Outputs Disabled		1	1	1	1	1	
	B to A	Outputs Enabled		12	13	14	15	16	
		Outputs Disabled		1	1	1	1	1	
$C_{pdB}^\dagger$	A to B	Outputs Enabled		13	13	14	15	16	pF
		Outputs Disabled		1	1	1	1	1	
	B to A	Outputs Enabled		1	1	1	2	2	
		Outputs Disabled		1	1	1	1	1	

$^\dagger$  Power-dissipation capacitance per transceiver

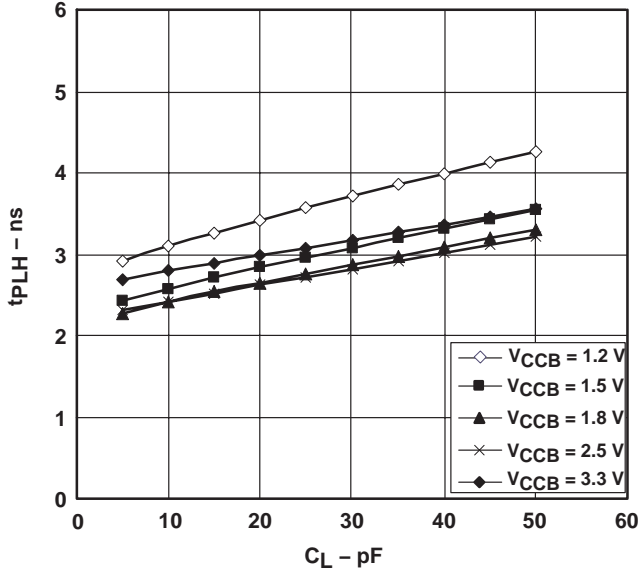
typical total static power consumption ( $I_{CCA} + I_{CCB}$ )

TABLE 1

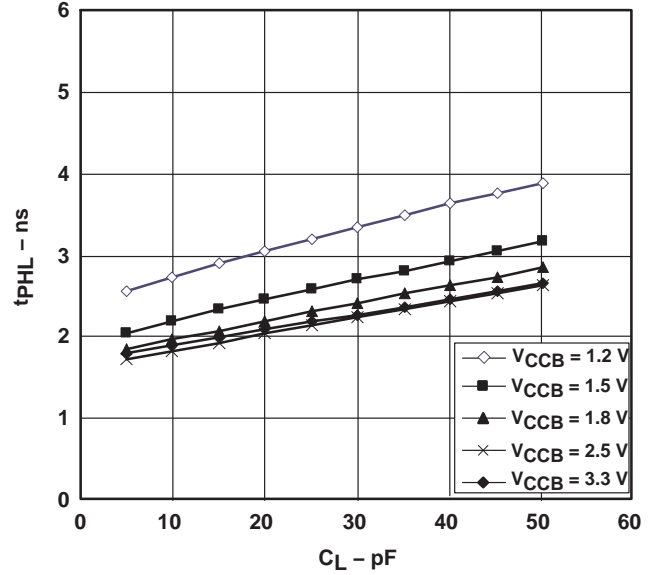
$V_{CCB}$	$V_{CCA}$						UNIT
	0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5	$\mu\text{A}$
1.2 V	< 0.5	< 1	< 1	< 1	< 1	1	
1.5 V	< 0.5	< 1	< 1	< 1	< 1	1	
1.8 V	< 0.5	< 1	< 1	< 1	< 1	< 1	
2.5 V	< 0.5	1	< 1	< 1	< 1	< 1	
3.3 V	< 0.5	1	< 1	< 1	< 1	< 1	

**TYPICAL CHARACTERISTICS**

**TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE**  
 $T_A = 25^\circ\text{C}, V_{CCA} = 1.2\text{ V}$

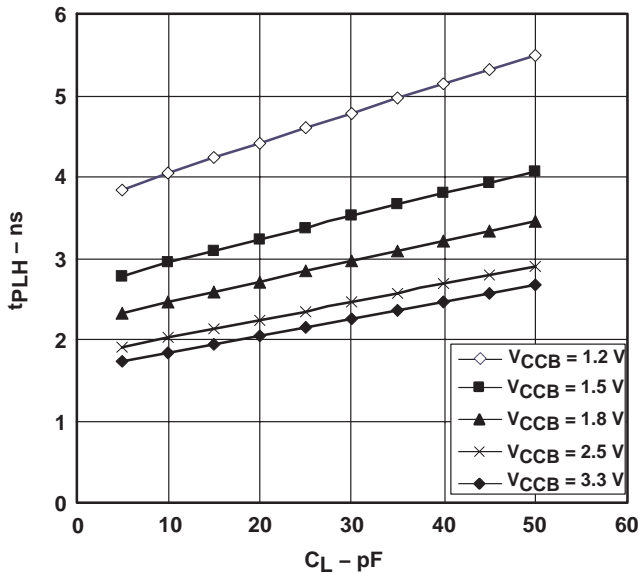


**Figure 1**

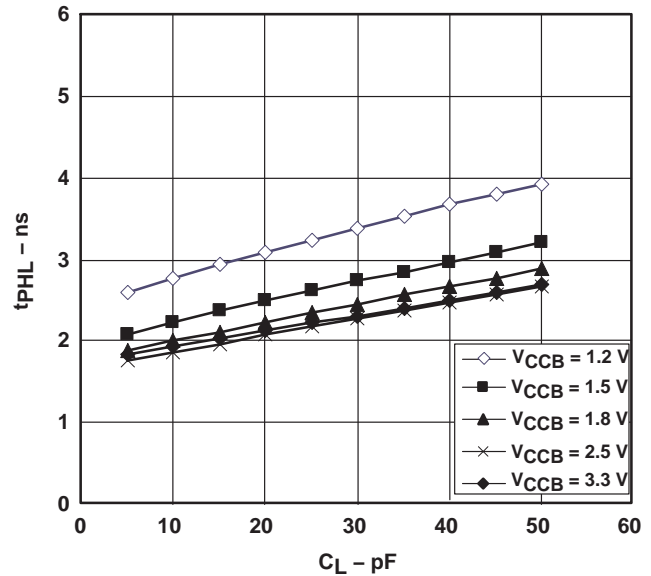


**Figure 2**

**TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE**  
 $T_A = 25^\circ\text{C}, V_{CCA} = 1.5\text{ V}$



**Figure 3**



**Figure 4**

**SN74AVCH20T245**  
**20-BIT DUAL-SUPPLY BUS TRANSCEIVER**  
**WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS**

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**TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE**  
 $T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 1.8\text{ V}$

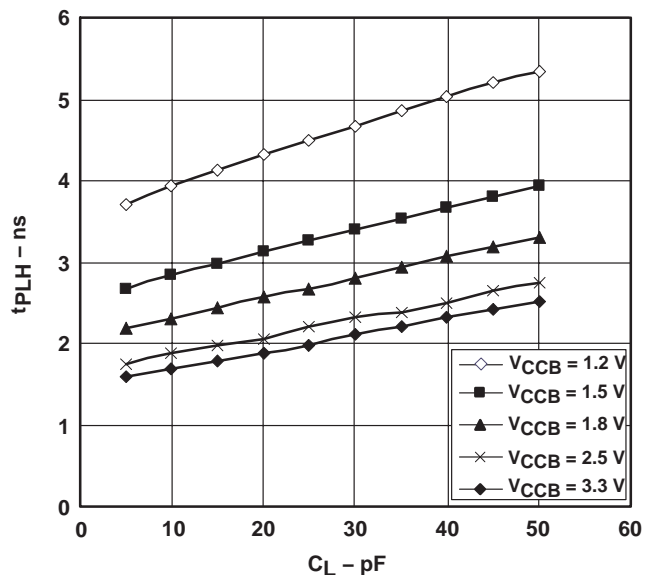


Figure 5

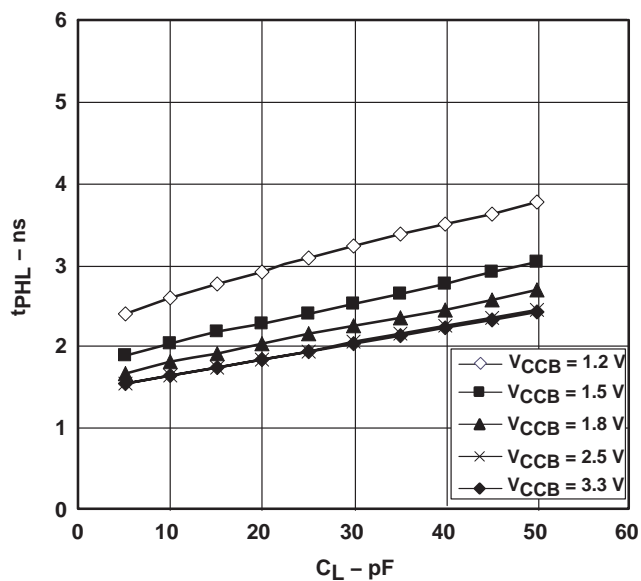


Figure 6

**TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE**  
 $T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 2.5\text{ V}$

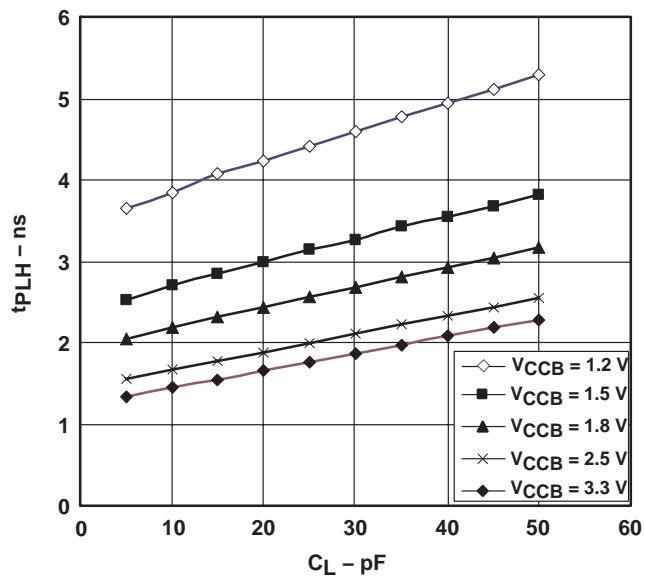


Figure 7

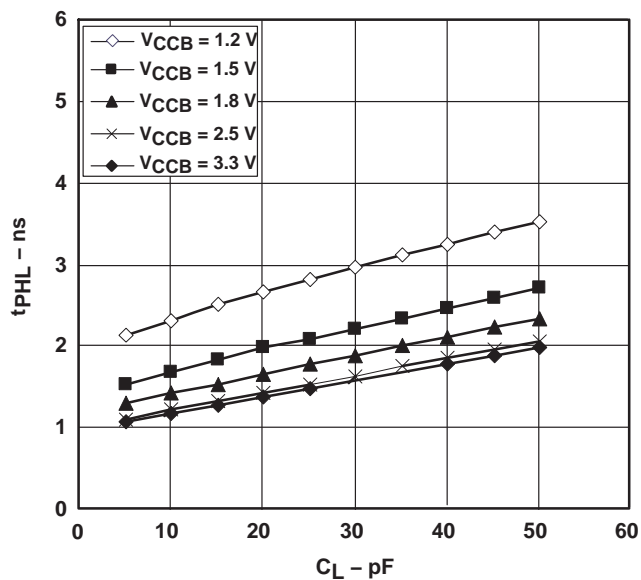


Figure 8

**SN74AVCH20T245**  
**20-BIT DUAL-SUPPLY BUS TRANSCEIVER**  
**WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS**

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**TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE**  
 $T_A = 25^\circ\text{C}, V_{CCA} = 3.3\text{ V}$

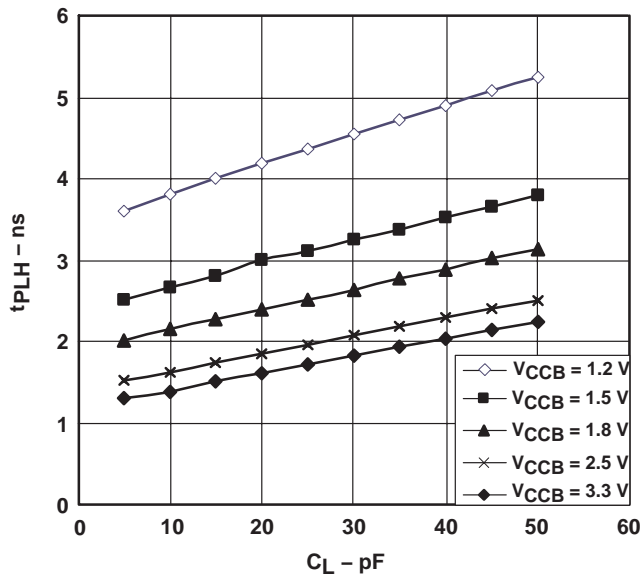


Figure 9

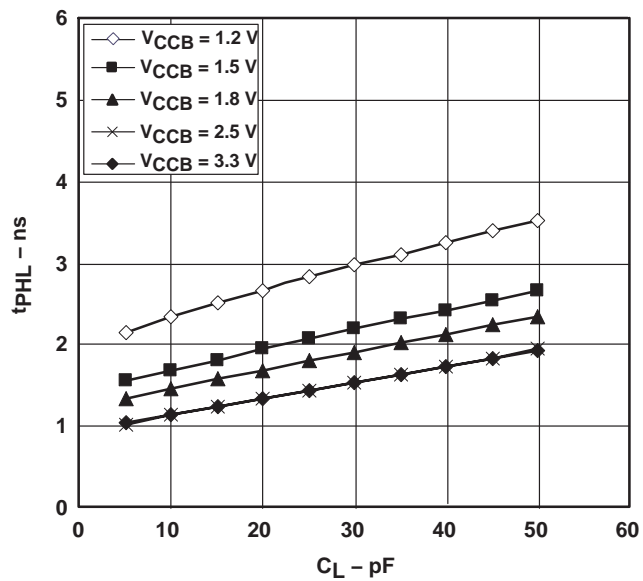
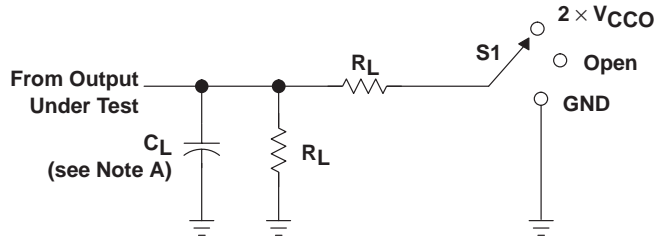


Figure 10

**SN74AVCH20T245**  
**20-BIT DUAL-SUPPLY BUS TRANSCEIVER**  
**WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS**

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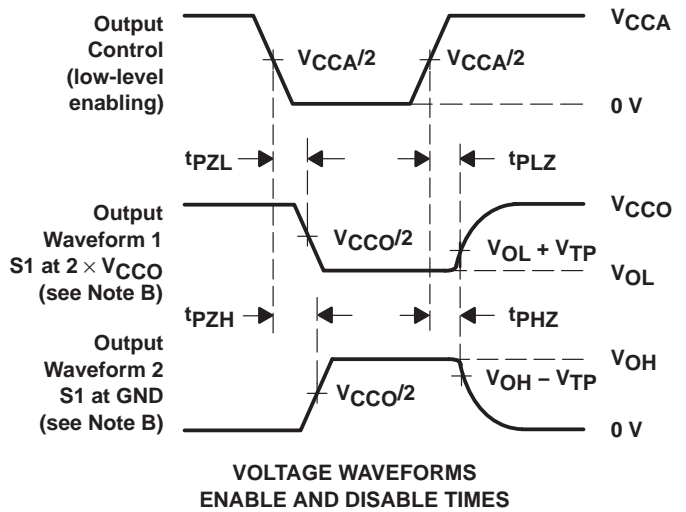
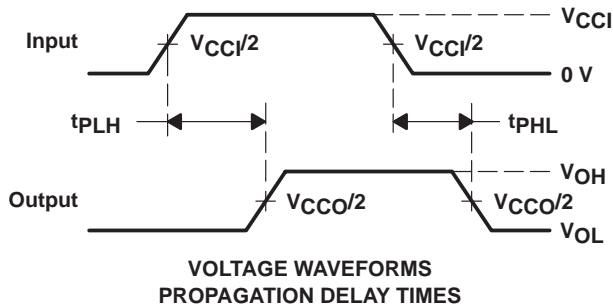
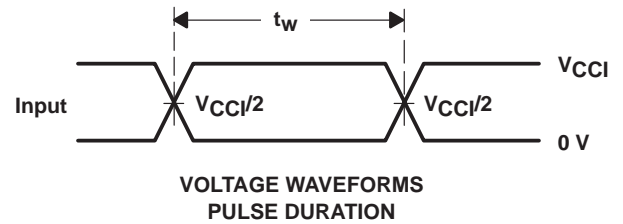
**PARAMETER MEASUREMENT INFORMATION**



**LOAD CIRCUIT**

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CCO}$
$t_{PHZ}/t_{PZH}$	GND




$V_{CCO}$	$C_L$	$R_L$	$V_{TP}$
1.2 V	15 pF	2 k $\Omega$	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.8 V $\pm$ 0.15 V	15 pF	2 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	15 pF	2 k $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	15 pF	2 k $\Omega$	0.3 V



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $dv/dt \geq 1$  V/ns.
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
  - $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

**Figure 11. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AVCH20T245ZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	WK245	
SN74AVCH20T245GR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCH20T245	
SN74AVCH20T245VR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WK245	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AVCH20T245ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
SN74AVCH20T245GR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74AVCH20T245VR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AVCH20T245ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	333.2	345.9	28.6
SN74AVCH20T245GR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74AVCH20T245VR	TVSOP	DGV	56	2000	367.0	367.0	45.0

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

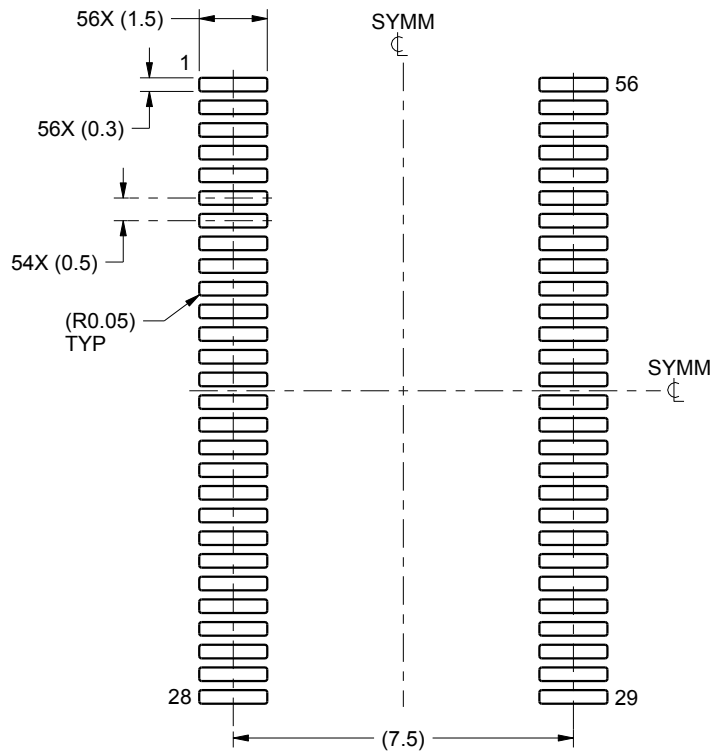


# EXAMPLE BOARD LAYOUT

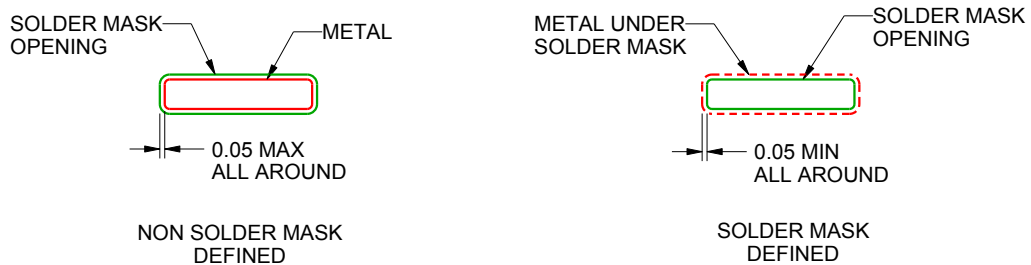
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

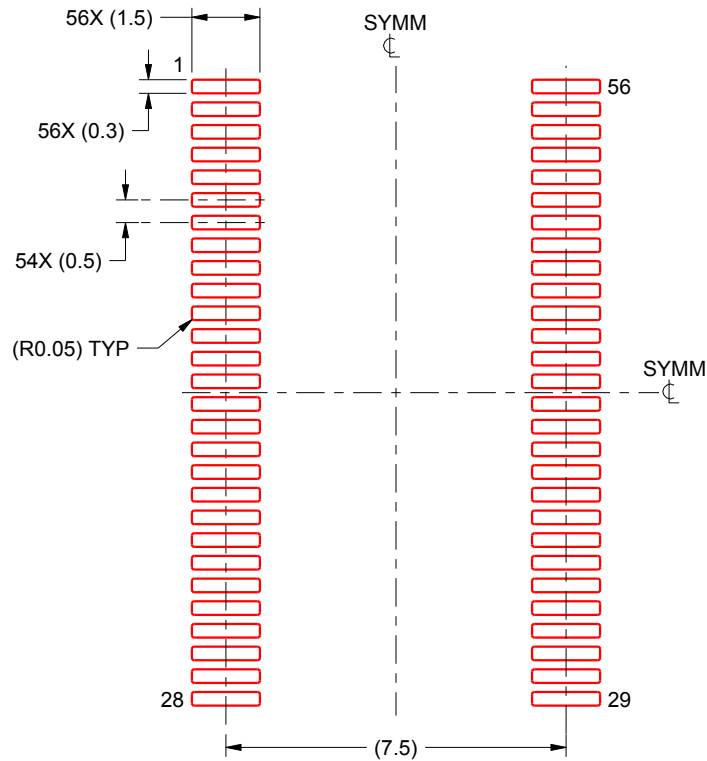
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

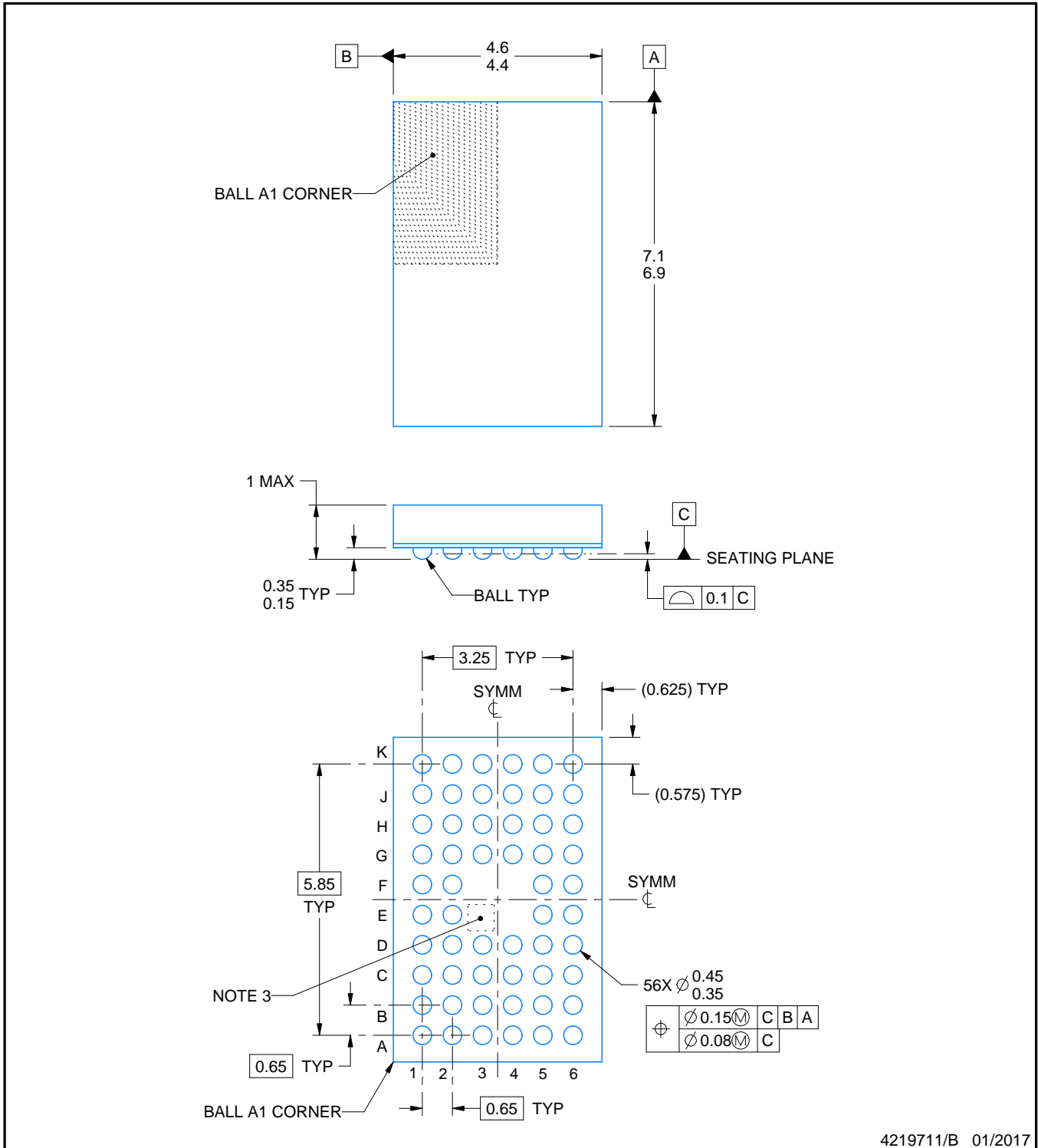
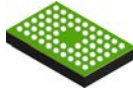


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4219711/B 01/2017

NOTES:

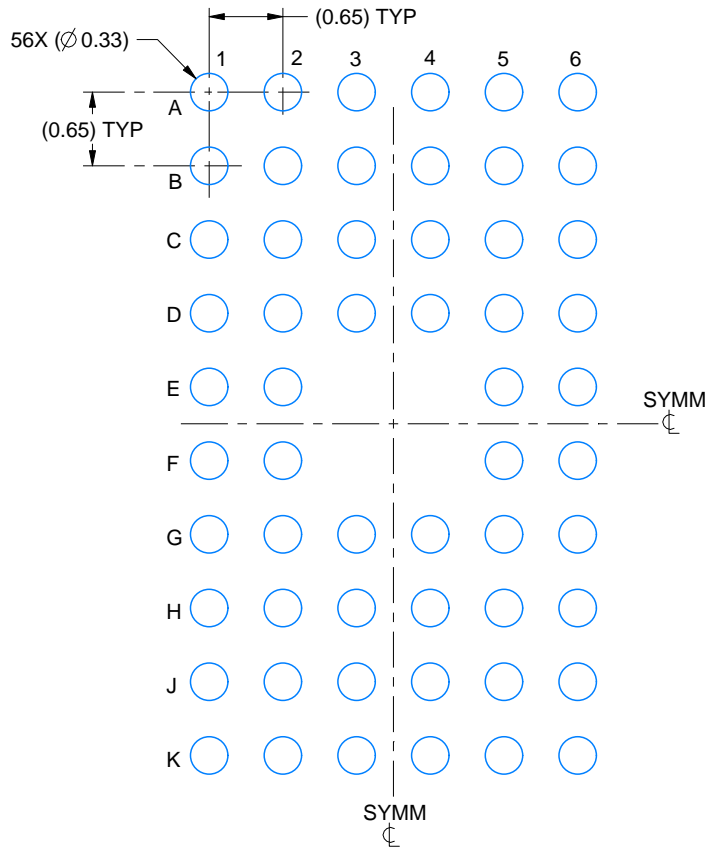
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. No metal in this area, indicates orientation.

# EXAMPLE BOARD LAYOUT

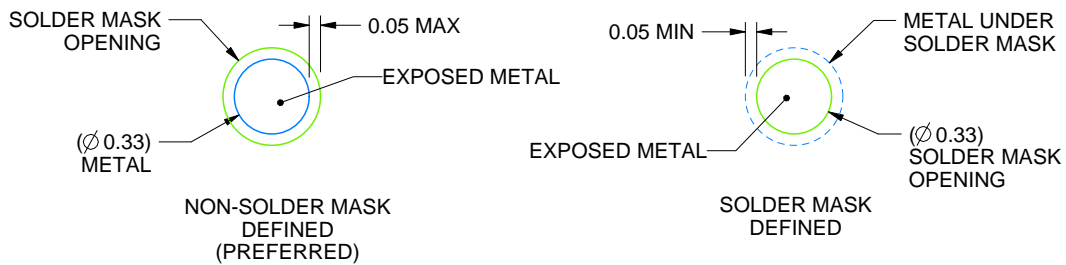
ZQL0056A

JRBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS  
NOT TO SCALE

4219711/B 01/2017

NOTES: (continued)

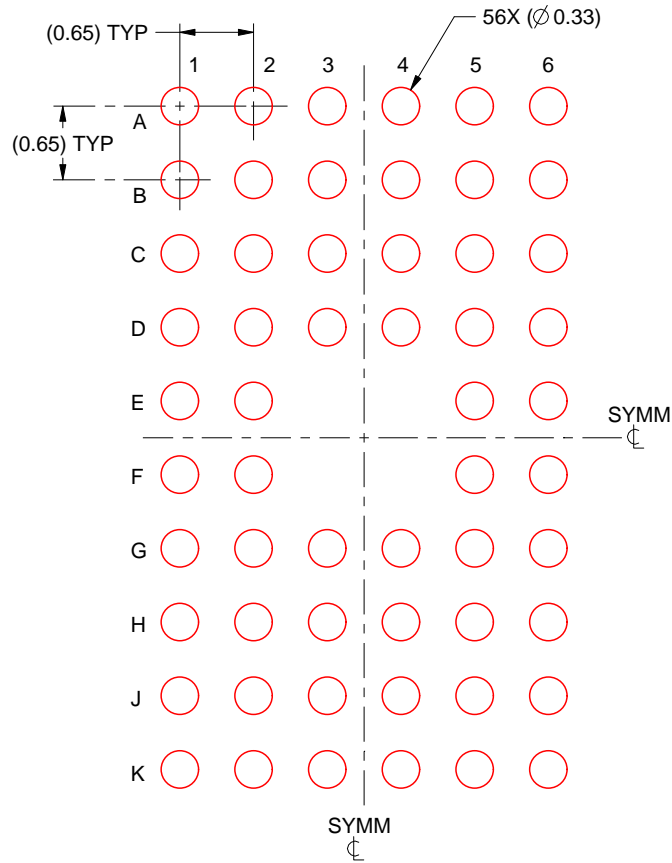
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 ([www.ti.com/lit/spraa99](http://www.ti.com/lit/spraa99)).

# EXAMPLE STENCIL DESIGN

ZQL0056A

JRBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4219711/B 01/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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