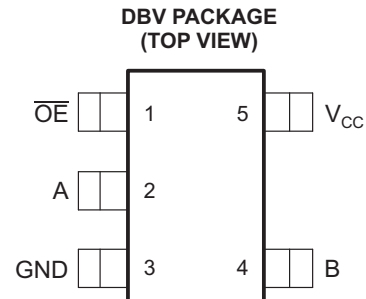


LOW-VOLTAGE SINGLE FET BUS SWITCH

Check for Samples: [SN74CBTLV1G125-Q1](#)

FEATURES

- Qualified for Automotive Applications
- 5-Ω Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- I_{off} Supports Partial-Power-Down Mode Operation



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The SN74CBTLV1G125 features a single high-speed line switch. The switch is disabled when the output-enable (\overline{OE}) input is high.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION⁽¹⁾

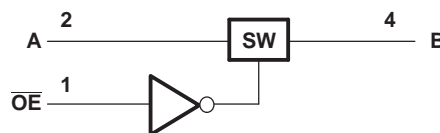
| T_A | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|--------------|-----------------------|------------------|
| -40°C to 125°C | SOT-23 – DBV | Reel of 3000 | 74CBTLV1G125DBVRQ1 | VCTO |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Table 1. FUNCTION TABLE

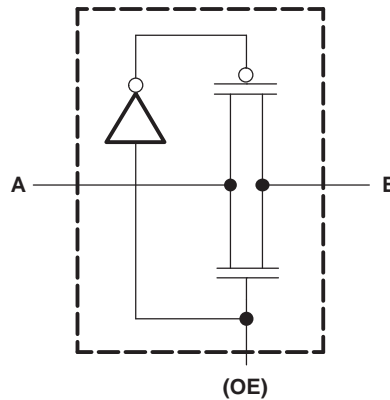
| INPUT \overline{OE} | FUNCTION |
|--------------------------|-----------------|
| L | A port = B port |
| H | Disconnect |

LOGIC DIAGRAM (POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SIMPLIFIED SCHEMATIC, EACH FET SWITCH

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|--|------|-----|------|
| V_{CC} Supply voltage range | -0.5 | 4.6 | V |
| V_I Input voltage range ⁽²⁾ | -0.5 | 4.6 | V |
| Continuous channel current | | 128 | mA |
| I_{IK} Input clamp current | | -50 | mA |
| θ_{JA} Package thermal impedance ⁽³⁾ | | 206 | °C/W |
| T_{stg} Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

| | MIN | MAX | UNIT |
|---|---|-----|------|
| V_{CC} Supply voltage | 2.3 | 3.6 | V |
| V_{IH} High-level control input voltage | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 1.7 | V |
| | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | 2 | |
| V_{IL} Low-level control input voltage | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 0.7 | V |
| | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | 0.8 | |
| T_A Operating free-air temperature | -40 | 125 | °C |

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP (1) | MAX | UNIT | |
|---------------------|---|---|----------------------|-----|------------|---------|---------------|----------|
| V_{IK} | | $V_{CC} = 3\text{ V}$, $I_I = -18\text{ mA}$ | | | | -1.2 | V | |
| I_I | | $V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND | | | | ± 1 | μA | |
| I_{off} | | $V_{CC} = 0$, V_I or $V_O = 0$ to 3.6 V , $\overline{OE} = 3.6\text{ V}$ | | | | 15 | μA | |
| | | $V_{CC} = 0$, V_I or $V_O = 0$ to 3.6 V , $\overline{OE} = 0\text{ V}$ | | | | 100 | | |
| I_{CC} | | $V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND | | | | 10 | μA | |
| ΔI_{CC} (2) | Control inputs | $V_{CC} = 3.6\text{ V}$, One input at 3 V , Other inputs at V_{CC} or GND | | | | 300 | μA | |
| C_i | Control inputs | $V_I = 3\text{ V}$ or 0 | | | | 2.5 | pF | |
| $C_{io(OFF)}$ | | $V_O = 3\text{ V}$ or 0 , $\overline{OE} = V_{CC}$ | | | | 7 | pF | |
| r_{on} (3) | $V_{CC} = 2.3\text{ V}$, TYP at $V_{CC} = 2.5\text{ V}$ | $V_I = 0$ | $I_I = 32\text{ mA}$ | | | 7 | 10 | Ω |
| | | | $I_I = 24\text{ mA}$ | | | 7 | 10 | |
| | | $V_I = 1.7\text{ V}$, | $I_I = 15\text{ mA}$ | | | 15 | 25 | |
| | $V_{CC} = 3\text{ V}$ | $V_I = 0$ | $I_I = 32\text{ mA}$ | | | 5 | 7 | |
| | | | $I_I = 24\text{ mA}$ | | | 5 | 7 | |
| | | $V_I = 2.4\text{ V}$, | $I_I = 15\text{ mA}$ | | | 10 | 15 | |

(1) All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

(2) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

(3) Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

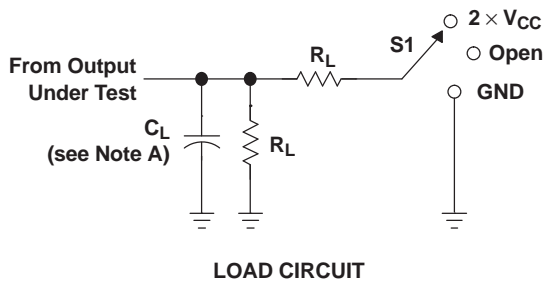
SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$ | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | UNIT |
|--------------|-----------------|----------------|---|------|---|------|------|
| | | | MIN | MAX | MIN | MAX | |
| t_{pd} (1) | A or B | B or A | | 0.15 | | 0.25 | ns |
| t_{en} | \overline{OE} | A or B | 0.5 | 8 | 0.5 | 7.5 | ns |
| t_{dis} | \overline{OE} | A or B | 0.5 | 8 | 0.5 | 7.5 | ns |

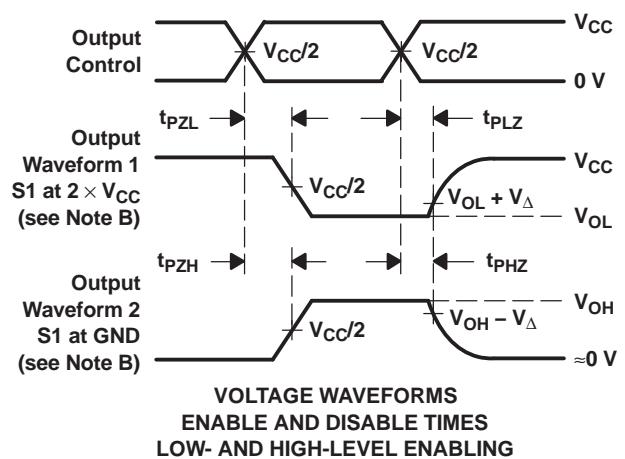
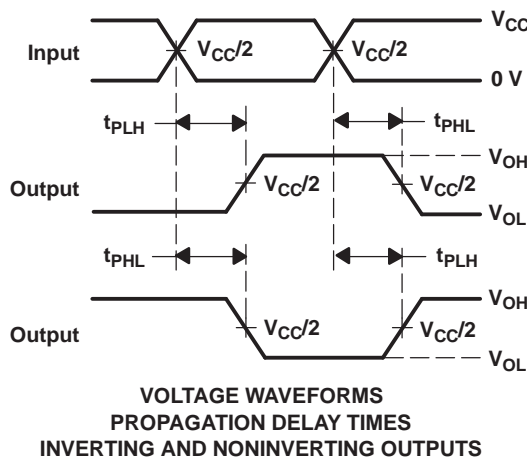
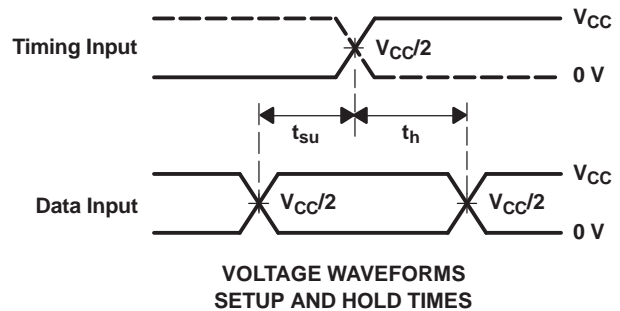
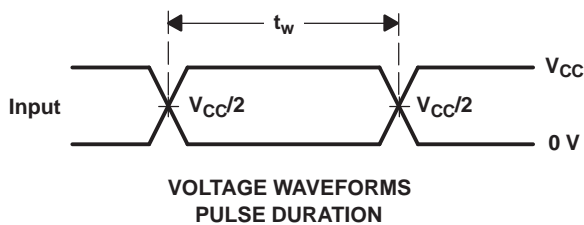
(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance of 50 pF , when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION



| TEST | S1 |
|-------------------|-------------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | C_L | R_L | V_{Δ} |
|-------------------|-------|--------------|--------------|
| $2.5 V \pm 0.2 V$ | 30 pF | 500 Ω | 0.15 V |
| $3.3 V \pm 0.3 V$ | 50 pF | 500 Ω | 0.3 V |



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|--------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|---------|
| 74CBTLV1G125DBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VCTO | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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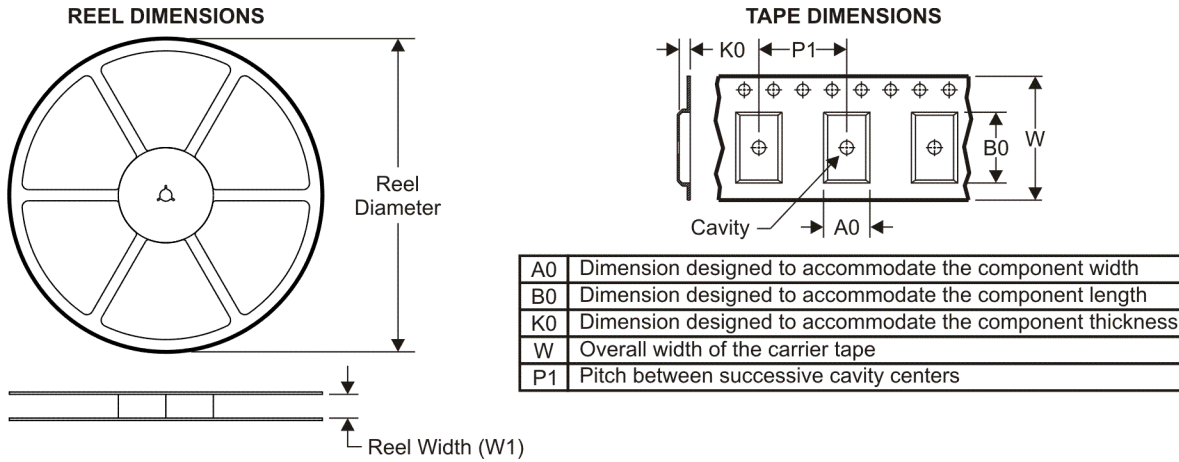
OTHER QUALIFIED VERSIONS OF SN74CBTLV1G125-Q1 :

- Catalog: [SN74CBTLV1G125](#)

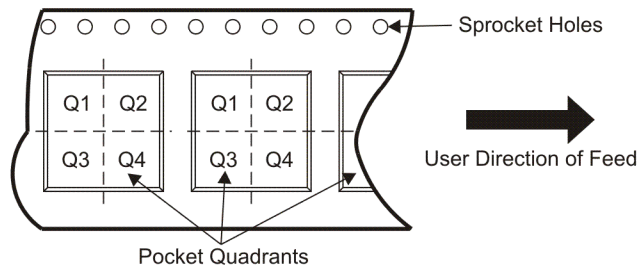
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74CBTLV1G125DBVRQ1 | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS

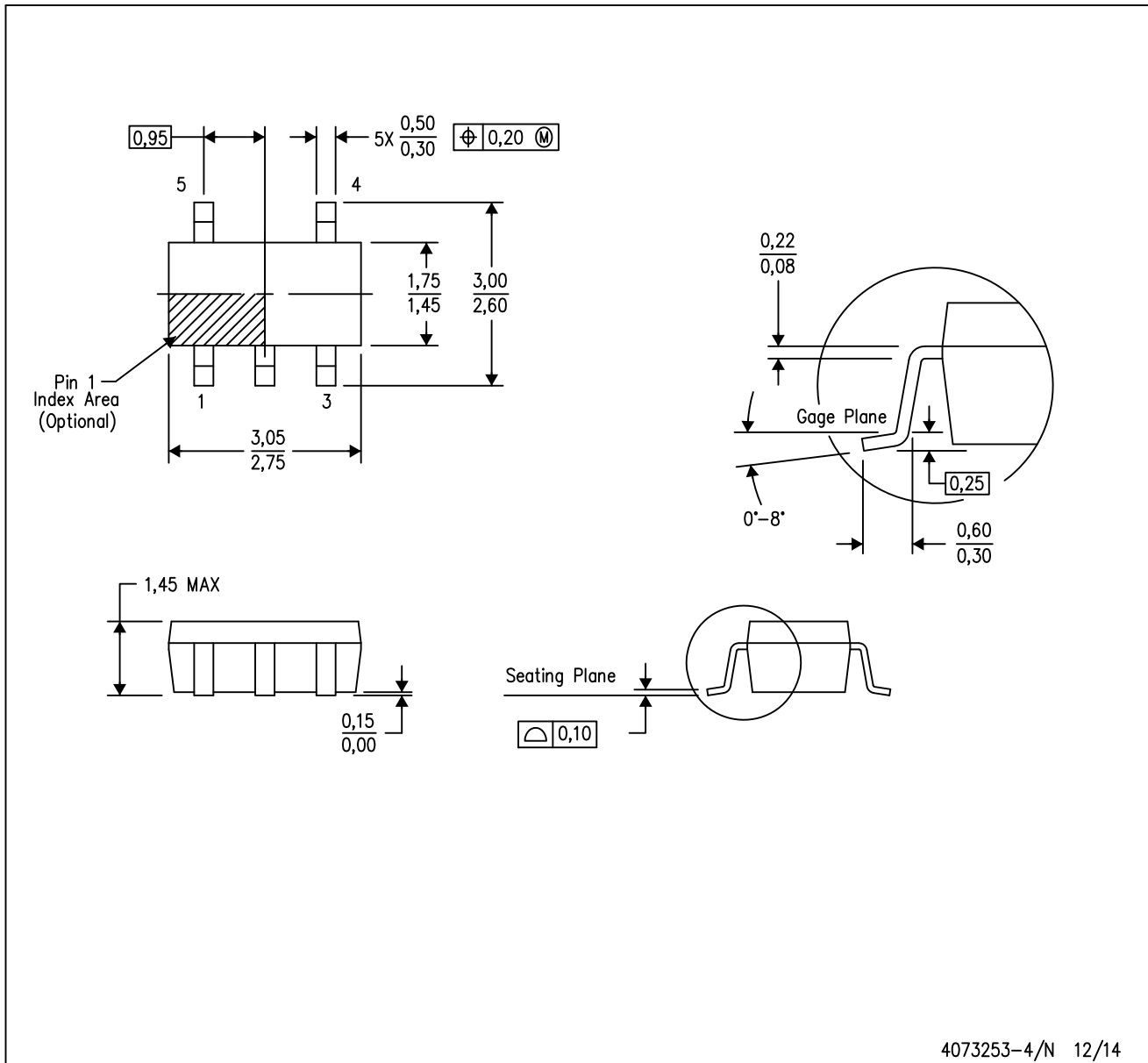


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74CBTLV1G125DBVRQ1 | SOT-23 | DBV | 5 | 3000 | 203.0 | 203.0 | 35.0 |

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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