

# **SN74LVC1T45 Single-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation and 3-State Outputs**

## **1 Features**

- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Available in the Texas Instruments NanoFree™ Package
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range
- $V_{CC}$  Isolation Feature – If Either  $V_{CC}$  Input Is at GND, Both Ports Are in the High-Impedance State
- DIR Input Circuit Referenced to  $V_{CCA}$
- Low Power Consumption, 4- $\mu$ A Max  $I_{CC}$
- $\pm 24$ -mA Output Drive at 3.3 V
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Max Data Rates
  - 420 Mbps (3.3-V to 5-V Translation)
  - 210 Mbps (Translate to 3.3 V)
  - 140 Mbps (Translate to 2.5 V)
  - 75 Mbps (Translate to 1.8 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

## **2 Applications**

- Personal Electronic
- Industrial
- Enterprise
- Telecom

## **3 Description**

This single-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track  $V_{CCA}$ .  $V_{CCA}$  accepts any supply voltage from 1.65 V to 5.5 V. The B port is designed to track  $V_{CCB}$ .  $V_{CCB}$  accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

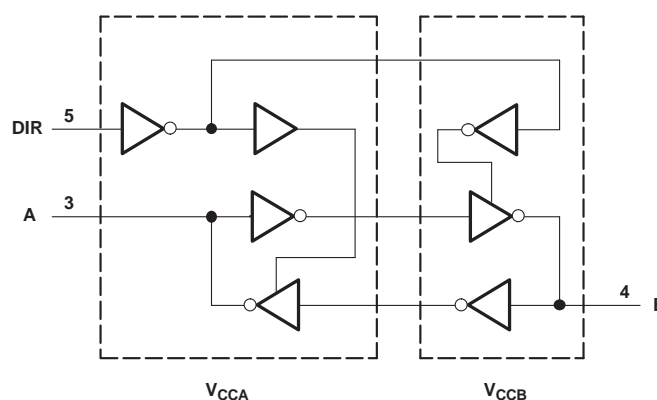
The SN74LVC1T45 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry is always active on both A and B ports and must have a logic HIGH or LOW level applied to prevent excess  $I_{CC}$  and  $I_{CCZ}$ .

### **Device Information<sup>(1)</sup>**

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1T45DRLR	SOT (6)	1.60 mm x 1.20 mm
SN74LVC1T45DBVR	SOT-23 (6)	2.90 mm x 1.60 mm
SN74LVC1T45DCKR	SC70 (6)	2.00 mm x 1.25 mm
SN74LVC1T45DPKR	USON (6)	1.60 mm x 1.60 mm
SN74LVC1T45YZPR	DSBGA (6)	1.39 mm x 0.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### **Functional Block Diagram**



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	9.1 Overview .....	12
<b>2 Applications</b> .....	<b>1</b>	9.2 Functional Block Diagram .....	12
<b>3 Description</b> .....	<b>1</b>	9.3 Feature Description .....	12
<b>4 Revision History</b> .....	<b>2</b>	9.4 Device Functional Modes .....	12
<b>5 Description (Continued)</b> .....	<b>3</b>	<b>10 Applications and Implementation</b> .....	<b>13</b>
<b>6 Pin Configuration and Functions</b> .....	<b>3</b>	10.1 Application Information .....	13
<b>7 Specifications</b> .....	<b>4</b>	10.2 Typical Application .....	13
7.1 Absolute Maximum Ratings .....	4	<b>11 Power Supply Recommendations</b> .....	<b>16</b>
7.2 ESD Ratings .....	4	<b>12 Layout</b> .....	<b>16</b>
7.3 Recommended Operating Conditions .....	4	12.1 Layout Guidelines .....	16
7.4 Thermal Information .....	5	12.2 Layout Example .....	16
7.5 Electrical Characteristics .....	6	<b>13 Device and Documentation Support</b> .....	<b>17</b>
7.6 Switching Characteristics ( $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$ ) ...	7	13.1 Documentation Support .....	17
7.7 Switching Characteristics ( $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ ) ....	7	13.2 Receiving Notification of Documentation Updates .....	17
7.8 Switching Characteristics ( $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$ ) ....	8	13.3 Community Resources .....	17
7.9 Switching Characteristics ( $V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$ ) .....	8	13.4 Trademarks .....	17
7.10 Operating Characteristics .....	8	13.5 Electrostatic Discharge Caution .....	17
7.11 Typical Characteristics .....	9	13.6 Glossary .....	17
<b>8 Parameter Measurement Information</b> .....	<b>11</b>	<b>14 Mechanical, Packaging, and Orderable Information</b> .....	<b>17</b>
<b>9 Detailed Description</b> .....	<b>12</b>		

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (December 2014) to Revision L	Page
• Added DPK (USON) package information .....	1
• Added Junction temperature, $T_J$ in <i>Absolute Maximum Ratings</i> .....	4
• Added <i>Documentation Support</i> section, <i>Receiving Notification of Documentation Updates</i> section, and <i>Community Resources</i> section .....	17

Changes from Revision J (December 2013) to Revision K	Page
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1

Changes from Revision I (December 2011) to Revision J	Page
• Updated document to new TI data sheet format - no specification changes. ....	1
• Removed ordering information. ....	1
• Added ESD warning. ....	1

## 5 Description (Continued)

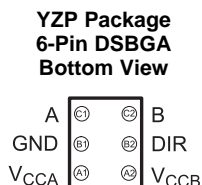
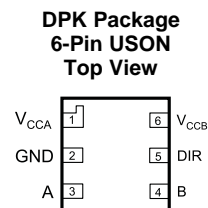
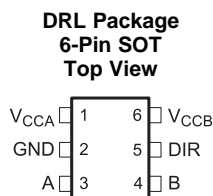
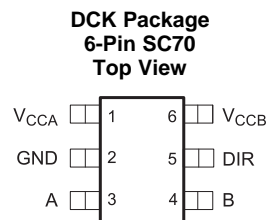
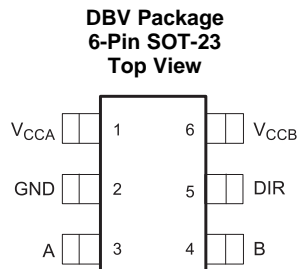
The SN74LVC1T45 is designed so that the DIR input is powered by  $V_{CCA}$ .

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The  $V_{CC}$  isolation feature is designed so that if either  $V_{CC}$  input is at GND, then both ports are in the high-impedance state.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

## 6 Pin Configuration and Functions



### Pin Functions

PIN			TYPE <sup>(1)</sup>	DESCRIPTION
NAME	DBV, DCK, DRL, DPK	YZP		
$V_{CCA}$	1	A1	P	SYSTEM-1 supply voltage (1.65 V to 5.5 V)
GND	2	B1	G	Device GND
A	3	C1	I/O	Output level depends on $V_{CC1}$ voltage.
B	4	C2	I/O	Input threshold value depends on $V_{CC2}$ voltage.
DIR	5	B2	I	GND (low level) determines B-port to A-port direction.
$V_{CCB}$	6	A2	P	SYSTEM-2 supply voltage (1.65 V to 5.5 V)

(1) P = power, G = ground, I/O = input and output, I = input

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CCA}$ $V_{CCB}$	Supply voltage	−0.5	6.5	V
$V_I$	Input voltage <sup>(2)</sup>	−0.5	6.5	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	−0.5	6.5	V
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	A port	$V_{CCA} + 0.5$	V
		B port	$V_{CCB} + 0.5$	
$I_{IK}$	Input clamp current	$V_I < 0$	−50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	−50	mA
$I_O$	Continuous output current		±50	mA
	Continuous current through $V_{CC}$ or GND		±100	mA
$T_J$	Junction temperature		150	°C
$T_{stg}$	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.

### 7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000
		Machine Model	±200

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

See <sup>(1)(2)(3)</sup>

			$V_{CCI}$	$V_{CCO}$	MIN	MAX	UNIT
$V_{CCA}$ $V_{CCB}$	Supply voltage				1.65	5.5	V
					1.65	5.5	
$V_{IH}$	High-level input voltage	Data inputs <sup>(4)</sup>	1.65 to 1.95 V		$V_{CCI} \times 0.65$		V
			2.3 to 2.7 V		1.7		
			3 to 3.6 V		2		
			4.5 to 5.5 V		$V_{CCI} \times 0.7$		
$V_{IL}$	Low-level input voltage	Data inputs <sup>(4)</sup>	1.65 to 1.95 V		$V_{CCI} \times 0.35$		V
			2.3 to 2.7 V		0.7		
			3 to 3.6 V		0.8		
			4.5 to 5.5 V		$V_{CCI} \times 0.3$		

- (1)  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
- (2)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.
- (3) All unused data inputs of the device must be held at  $V_{CCI}$  or GND to ensure proper device operation. See the TI application report, [Implications of Slow or Floating CMOS Inputs](#), SCBA004.
- (4) For  $V_{CCI}$  values not specified in the data sheet,  $V_{IH} \text{ min} = V_{CCI} \times 0.7 \text{ V}$ ,  $V_{IL} \text{ max} = V_{CCI} \times 0.3 \text{ V}$ .

## Recommended Operating Conditions (continued)

See (1)(2)(3)

		$V_{CCI}$	$V_{CCO}$	MIN	MAX	UNIT
$V_{IH}$	High-level input voltage	DIR (referenced to $V_{CCA}$ ) <sup>(5)</sup>	1.65 to 1.95 V	$V_{CCA} \times 0.65$		V
			2.3 to 2.7 V	1.7		
			3 to 3.6 V	2		
			4.5 to 5.5 V	$V_{CCA} \times 0.7$		
$V_{IL}$	Low-level input voltage	DIR (referenced to $V_{CCA}$ ) <sup>(5)</sup>	1.65 to 1.95 V	$V_{CCA} \times 0.35$		V
			2.3 to 2.7 V	0.7		
			3 to 3.6 V	0.8		
			4.5 to 5.5 V	$V_{CCA} \times 0.3$		
$V_I$	Input voltage			0	5.5	V
$V_O$	Output voltage			0	$V_{CCO}$	V
$I_{OH}$	High-level output current		1.65 to 1.95 V		–4	mA
			2.3 to 2.7 V		–8	
			3 to 3.6 V		–24	
			4.5 to 5.5 V		–32	
$I_{OL}$	Low-level output current		1.65 to 1.95 V		4	mA
			2.3 to 2.7 V		8	
			3 to 3.6 V		24	
			4.5 to 5.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	Data inputs	1.65 to 1.95 V		20	ns/V
			2.3 to 2.7 V		20	
			3 to 3.6 V		10	
			4.5 to 5.5 V		5	
	Control inputs		1.65 to 5.5 V		5	
$T_A$	Operating free-air temperature			–40	85	°C

(5) For  $V_{CCI}$  values not specified in the data sheet,  $V_{IH} \text{ min} = V_{CCA} \times 0.7 \text{ V}$ ,  $V_{IL} \text{ max} = V_{CCA} \times 0.3 \text{ V}$ .

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74LVC1T45					UNIT
		DBV (SOT-23)	DCK (SC70)	DPK (USON)	DRL (SOT)	YZP (DSBGA)	
		6 PINS					
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	200.1	286.8	278.3	223.7	131.0	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	144.5	93.9	133.4	88.7	1.3	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	45.7	95.5	174.1	58.4	22.6	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	36.2	1.9	23.4	5.9	5.2	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	25.3	94.7	173.5	58.1	22.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

**SN74LVC1T45**

SCES515L – DECEMBER 2003 – REVISED FEBRUARY 2017

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**7.5 Electrical Characteristics**

 over recommended operating free-air temperature range,  $T_A = -40$  to  $+85^\circ\text{C}$  (unless otherwise noted)<sup>(1)(2)</sup>

PARAMETER		TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>		MIN	TYP	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = −100 μA	V <sub>I</sub> = V <sub>IH</sub>	1.65 to 4.5 V	1.65 to 4.5 V	V <sub>CCO</sub> − 0.1		V	
		I <sub>OH</sub> = −4 mA		1.65 V	1.65 V	1.2			
		I <sub>OH</sub> = −8 mA		2.3 V	2.3 V	1.9			
		I <sub>OH</sub> = −24 mA		3 V	3 V	2.4			
		I <sub>OH</sub> = −32 mA		4.5 V	4.5 V	3.8			
V <sub>OL</sub>		I <sub>OL</sub> = 100 μA	V <sub>I</sub> = V <sub>IL</sub>	1.65 to 4.5 V	1.65 to 4.5 V	0.1		V	
		I <sub>OL</sub> = 4 mA		1.65 V	1.65 V	0.45			
		I <sub>OL</sub> = 8 mA		2.3 V	2.3 V	0.3			
		I <sub>OL</sub> = 24 mA		3 V	3 V	0.55			
		I <sub>OL</sub> = 32 mA		4.5 V	4.5 V	0.55			
I <sub>I</sub> DIR		V <sub>I</sub> = V <sub>CCA</sub> or GND	1.65 to 5.5 V	1.65 to 5.5 V	T <sub>A</sub> = 25 °C	±1		μA	
					T <sub>A</sub> = −40 to +85°C	±2			
I <sub>off</sub>	A port	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0 V	0 to 5.5 V	T <sub>A</sub> = 25 °C	±1		μA	
					T <sub>A</sub> = −40 to +85°C	±2			
	B port		0 to 5.5 V	0 V	T <sub>A</sub> = 25 °C	±1			
					T <sub>A</sub> = −40 to +85°C	±2			
I <sub>OZ</sub>	A or B port	V <sub>O</sub> = V <sub>CCO</sub> or GND	1.65 to 5.5 V	1.65 to 5.5 V	T <sub>A</sub> = 25 °C	±1		μA	
					T <sub>A</sub> = −40 to +85°C	±2			
I <sub>CCA</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.65 to 5.5 V	1.65 to 5.5 V		3		μA	
			5.5 V	0 V		2			
			0 V	5.5 V		−2			
I <sub>CCB</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.65 to 5.5 V	1.65 to 5.5 V		3		μA	
			5.5 V	0 V		−2			
			0 V	5.5 V		2			
I <sub>CCA</sub> + I <sub>CCB</sub> (see Table 1)		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.65 to 5.5 V	1.65 to 5.5 V		4		μA	
ΔI <sub>CCA</sub>	A port	A port at V <sub>CCA</sub> − 0.6 V, DIR at V <sub>CCA</sub> , B port = open	3 to 5.5 V	3 to 5.5 V		50		μA	
	DIR	DIR at V <sub>CCA</sub> − 0.6 V, B port = open, A port at V <sub>CCA</sub> or GND				50			
ΔI <sub>CCB</sub>	B port	B port at V <sub>CCB</sub> − 0.6 V, DIR at GND, A port = open	3 to 5.5 V	3 to 5.5 V		50		μA	
C <sub>i</sub>	DIR	V <sub>I</sub> = V <sub>CCA</sub> or GND	3.3 V	3.3 V	T <sub>A</sub> = 25 °C	2.5		pF	
C <sub>io</sub>	A or B port	V <sub>O</sub> = V <sub>CCA/B</sub> or GND	3.3 V	3.3 V	T <sub>A</sub> = 25 °C	6		pF	

 (1)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

 (2)  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.

## 7.6 Switching Characteristics ( $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$ )

over recommended operating free-air temperature range,  $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$  (see [Figure 9](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.8 V ±0.15 V		V <sub>CCB</sub> = 2.5 V ±0.2 V		V <sub>CCB</sub> = 3.3 V ±0.3 V		V <sub>CCB</sub> = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	B	3	17.7	2.2	10.3	1.7	8.3	1.4	7.2	ns
t <sub>PHL</sub>			2.8	14.3	2.2	8.5	1.8	7.1	1.7	7	
t <sub>PLH</sub>	B	A	3	17.7	2.3	16	2.1	15.5	1.9	15.1	ns
t <sub>PHL</sub>			2.8	14.3	2.1	12.9	2	12.6	1.8	12.2	
t <sub>PHZ</sub>	DIR	A	5.2	19.4	4.8	18.5	4.7	18.4	5.1	17.1	ns
t <sub>PLZ</sub>			2.3	10.5	2.1	10.5	2.4	10.7	3.1	10.9	
t <sub>PHZ</sub>	DIR	B	7.4	21.9	4.9	11.5	4.6	10.3	2.8	8.2	ns
t <sub>PLZ</sub>			4.2	16	3.7	9.2	3.3	8.4	2.4	6.4	
t <sub>PZH</sub> <sup>(1)</sup>	DIR	A	33.7		25.2		23.9		21.5		ns
t <sub>PZL</sub> <sup>(1)</sup>			36.2		24.4		22.9		20.4		
t <sub>PZH</sub> <sup>(1)</sup>	DIR	B	28.2		20.8		19		18.1		ns
t <sub>PZL</sub> <sup>(1)</sup>			33.7		27		25.5		24.1		

(1) The enable time is a calculated value, derived using the formula shown in the [Enable Times](#) section.

## 7.7 Switching Characteristics ( $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ )

over recommended operating free-air temperature range,  $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (see [Figure 9](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	2.3	16	1.5	8.5	1.3	6.4	1.1	5.1	ns
$t_{PHL}$			2.1	12.9	1.4	7.5	1.3	5.4	0.9	4.6	
$t_{PLH}$	B	A	2.2	10.3	1.5	8.5	1.4	8	1	7.5	ns
$t_{PHL}$			2.2	8.5	1.4	7.5	1.3	7	0.9	6.2	
$t_{PHZ}$	DIR	A	3	8.1	3.1	8.1	2.8	8.1	3.2	8.1	ns
$t_{PLZ}$			1.3	5.9	1.3	5.9	1.3	5.9	1	5.8	
$t_{PHZ}$	DIR	B	6.5	23.7	4.1	11.4	3.9	10.2	2.4	7.1	ns
$t_{PLZ}$			3.9	18.9	3.2	9.6	2.8	8.4	1.8	5.3	
$t_{PZH}^{(1)}$	DIR	A	29.2		18.1		16.4		12.8		ns
$t_{PZL}^{(1)}$			32.2		18.9		17.2		13.3		
$t_{PZH}^{(1)}$	DIR	B	21.9		14.4		12.3		10.9		ns
$t_{PZL}^{(1)}$			21		15.6		13.5		12.7		

(1) The enable time is a calculated value, derived using the formula shown in the [Enable Times](#) section.

**SN74LVC1T45**

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**7.8 Switching Characteristics ( $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$ )**

 over recommended operating free-air temperature range,  $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$  (see [Figure 9](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	2.1	15.5	1.4	8	0.7	5.8	0.7	4.4	ns
$t_{PHL}$			2	12.6	1.3	7	0.8	5	0.7	4	
$t_{PLH}$	B	A	1.7	8.3	1.3	6.4	0.7	5.8	0.6	5.4	ns
$t_{PHL}$			1.8	7.1	1.3	5.4	0.8	5	0.7	4.5	
$t_{PHZ}$	DIR	A	2.9	7.3	3	7.3	2.8	7.3	3.4	7.3	ns
$t_{PLZ}$			1.8	5.6	1.6	5.6	2.2	5.7	2.2	5.7	
$t_{PHZ}$	DIR	B	5.4	20.5	3.9	10.1	2.9	8.8	2.4	6.8	ns
$t_{PLZ}$			3.3	14.5	2.9	7.8	2.4	7.1	1.7	4.9	
$t_{PZH}^{(1)}$	DIR	A		22.8		14.2		12.9		10.3	ns
$t_{PZL}^{(1)}$				27.6		15.5		13.8		11.3	
$t_{PZH}^{(1)}$	DIR	B		21.1		13.6		11.5		10.1	ns
$t_{PZL}^{(1)}$				19.9		14.3		12.3		11.3	

 (1) The enable time is a calculated value, derived using the formula shown in the [Enable Times](#) section.

**7.9 Switching Characteristics ( $V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$ )**

 over recommended operating free-air temperature range,  $V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$  (see [Figure 9](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	1.9	15.1	1	7.5	0.6	5.4	0.5	3.9	ns
$t_{PHL}$			1.8	12.2	0.9	6.2	0.7	4.5	0.5	3.5	
$t_{PLH}$	B	A	1.4	7.2	1	5.1	0.7	4.4	0.5	3.9	ns
$t_{PHL}$			1.7	7	0.9	4.6	0.7	4	0.5	3.5	
$t_{PHZ}$	DIR	A	2.1	5.4	2.2	5.4	2.2	5.5	2.2	5.4	ns
$t_{PLZ}$			0.9	3.8	1	3.8	1	3.7	0.9	3.7	
$t_{PHZ}$	DIR	B	4.8	20.2	2.5	9.8	1	8.5	2.5	6.5	ns
$t_{PLZ}$			4.2	14.8	2.5	7.4	2.5	7	1.6	4.5	
$t_{PZH}^{(1)}$	DIR	A		22		12.5		11.4		8.4	ns
$t_{PZL}^{(1)}$				27.2		14.4		12.5		10	
$t_{PZH}^{(1)}$	DIR	B		18.9		11.3		9.1		7.6	ns
$t_{PZL}^{(1)}$				17.6		11.6		10		8.6	

 (1) The enable time is a calculated value, derived using the formula shown in the [Enable Times](#) section.

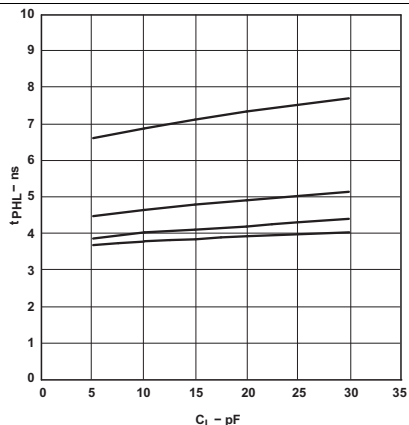
**7.10 Operating Characteristics**
 $T_A = 25^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS	$V_{CCA} =$ $V_{CCB} = 1.8\text{ V}$	$V_{CCA} =$ $V_{CCB} = 2.5\text{ V}$	$V_{CCA} =$ $V_{CCB} = 3.3\text{ V}$	$V_{CCA} =$ $V_{CCB} = 5\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	
$C_{pdA}^{(1)}$	A-port input, B-port output	$C_L = 0\text{ pF}$ , $f = 10\text{ MHz}$ , $t_r = t_f = 1\text{ ns}$	3	4	4	4	pF
	B-port input, A-port output		18	19	20	21	
$C_{pdB}^{(1)}$	A-port input, B-port output	$C_L = 0\text{ pF}$ , $f = 10\text{ MHz}$ , $t_r = t_f = 1\text{ ns}$	18	19	20	21	pF
	B-port input, A-port output		3	4	4	4	

(1) Power dissipation capacitance per transceiver

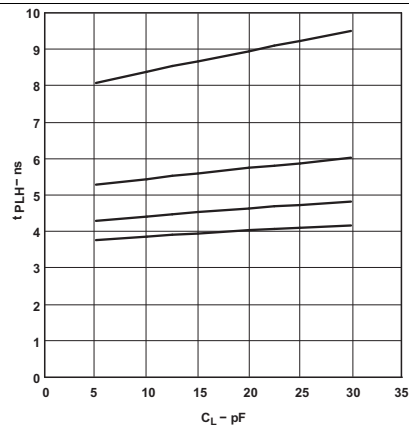


## 7.11 Typical Characteristics



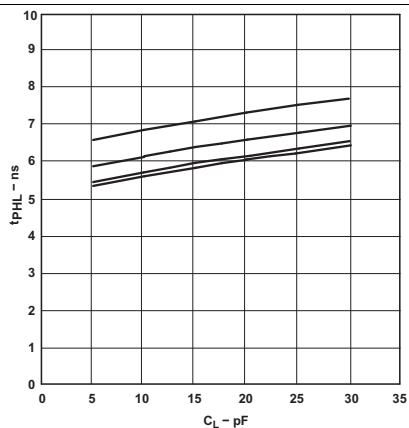
$T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 1.8\text{ V}$

**Figure 1. Typical Propagation Delay (A to B) vs Load Capacitance**



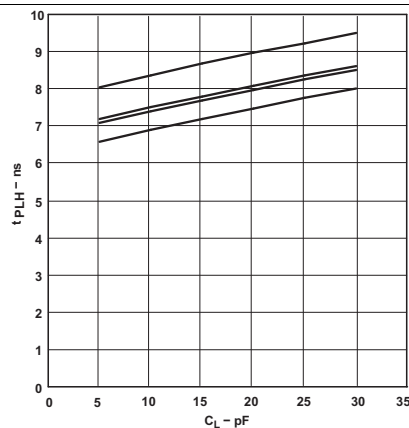
$T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 1.8\text{ V}$

**Figure 2. Typical Propagation Delay (B to A) vs Load Capacitance**



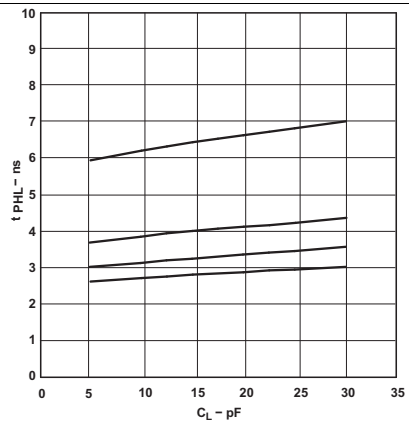
$T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 2.5\text{ V}$

**Figure 3. Typical Propagation Delay (A to B) vs Load Capacitance**



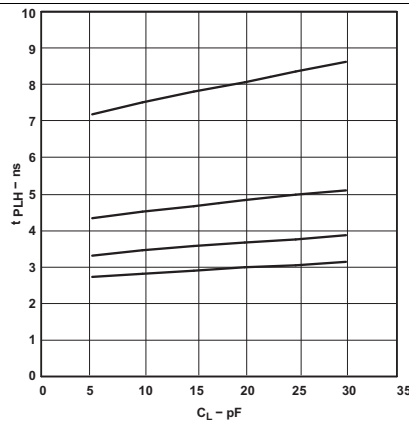
$T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 2.5\text{ V}$

**Figure 4. Typical Propagation Delay (B to A) vs Load Capacitance**



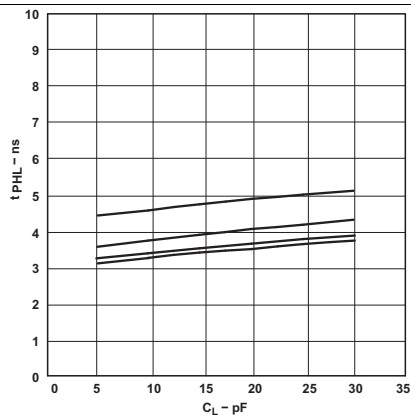
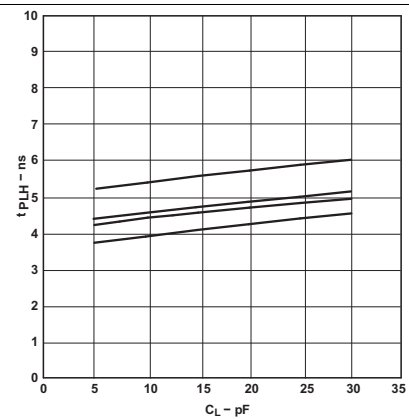
$T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 3.3\text{ V}$

**Figure 5. Typical Propagation Delay (A to B) vs Load Capacitance**

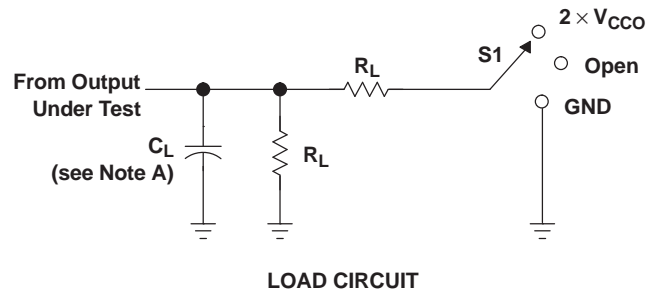


$T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 3.3\text{ V}$

**Figure 6. Typical Propagation Delay (B to A) vs Load Capacitance**

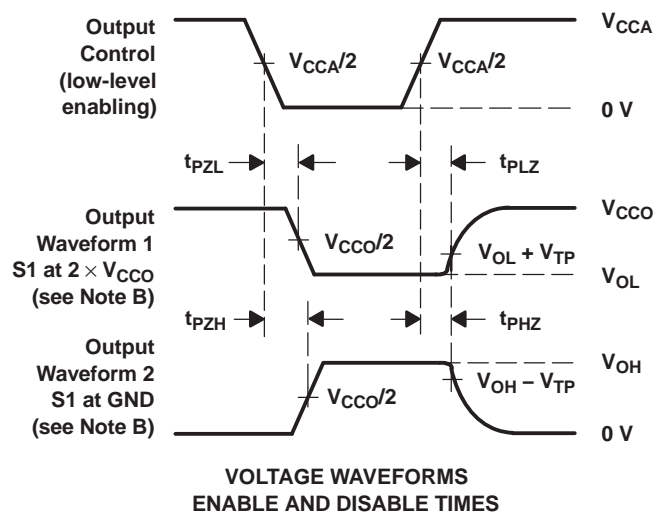
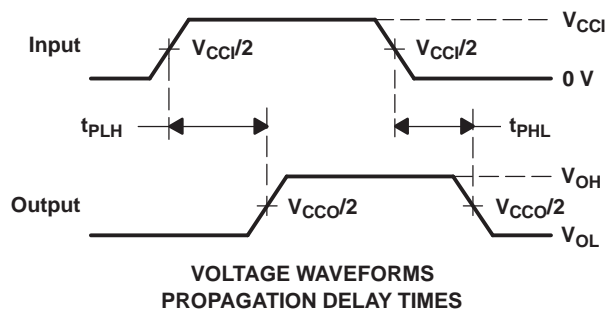
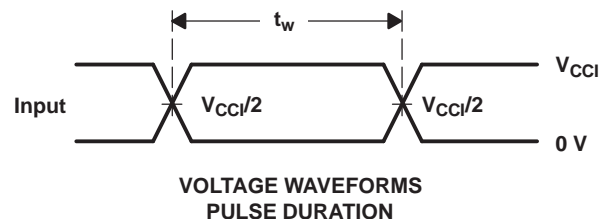
**Typical Characteristics (continued)**

 $T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 5\text{ V}$ 
**Figure 7. Typical Propagation Delay (A to B) vs Load Capacitance**

 $T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 5\text{ V}$ 
**Figure 8. Typical Propagation Delay (B to A) vs Load Capacitance**

## 8 Parameter Measurement Information



$V_{CCO}$	$C_L$	$R_L$	$V_{TP}$
$1.8\text{ V} \pm 0.15\text{ V}$	15 pF	2 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	15 pF	2 k $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	15 pF	2 k $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	15 pF	2 k $\Omega$	0.3 V

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CCO}$
$t_{PHZ}/t_{PZH}$	GND



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $dv/dt \geq 1\text{ V/ns}$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H.  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
  - I.  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.
  - J. All parameters and waveforms are not applicable to all devices.

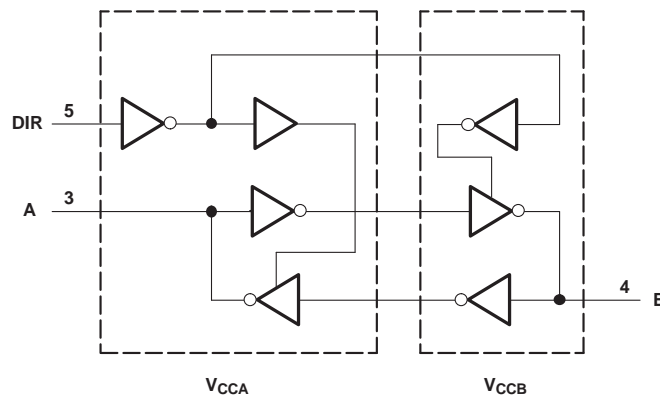
Figure 9. Load Circuit and Voltage Waveforms

## 9 Detailed Description

### 9.1 Overview

The SN74LVC1T45 is a single-bit, dual-supply, noninverting voltage level transceiver. Pin A and that direction control pin (DIR) are supported by  $V_{CCA}$  and pin B is supported by  $V_{CCB}$ . The A port is able to accept I/O voltages ranging from 1.65 V to 5.5 V, while the B port can accept I/O voltages from 1.65 V to 5.5 V. The high on the DIR allows data transmissions from A to B and a low on the DIR allows data transmissions from B to A.

### 9.2 Functional Block Diagram



**Figure 10. Logic Diagram (Positive Logic)**

### 9.3 Feature Description

#### 9.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range

Both  $V_{CCA}$  and  $V_{CCB}$  can be supplied at any voltage between 1.65 V and 5.5 V, making the device suitable for translating between any of the voltage nodes (1.8-V, 2.5-V, 3.3-V, and 5-V).

#### 9.3.2 Support High Speed Translation

The SN74LVC1T45 device supports high data rate applications. The translated signal data rate can be up to 420 Mbps when the signal is translated from 3.3 V to 5 V.

#### 9.3.3 $I_{off}$ Supports Partial Power-Down Mode Operation

$I_{off}$  prevents backflow current by disabling I/O output circuits when device is in partial-power-down mode.

### 9.4 Device Functional Modes

**Table 1. Function Table<sup>(1)</sup>**

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

## 10 Applications and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

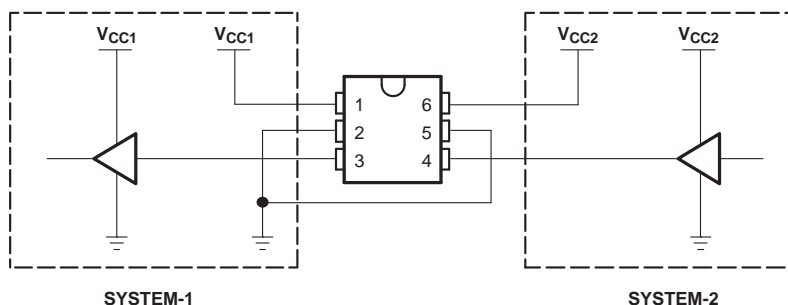
### 10.1 Application Information

The SN74LVC1T45 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The maximum data rate can be up to 420 Mbps when device translates signals from 3.3 V to 5 V.

### 10.2 Typical Application

#### 10.2.1 Unidirectional Logic Level-Shifting Application

Figure 11 shows an example of the SN74LVC1T45 being used in a unidirectional logic level-shifting application.



**Figure 11. Unidirectional Logic Level-Shifting Application**

##### 10.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 2.

**Table 2. Design Parameters**

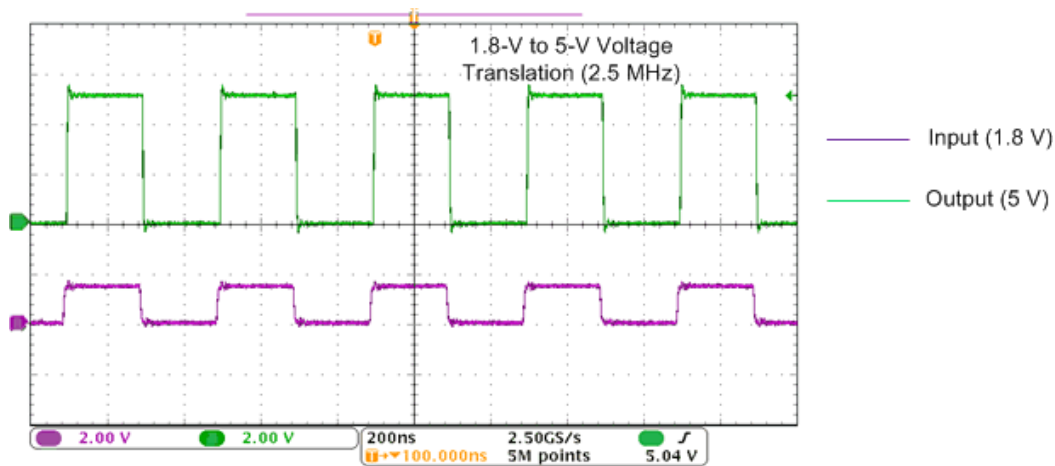
DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.65 V to 5.5 V
Output voltage range	1.65 V to 5.5 V

##### 10.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74LVC1T45 device to determine the input voltage range. For a valid logic high the value must exceed the  $V_{IH}$  of the input port. For a valid logic low the value must be less than the  $V_{IL}$  of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74LVC1T45 device is driving to determine the output voltage range.

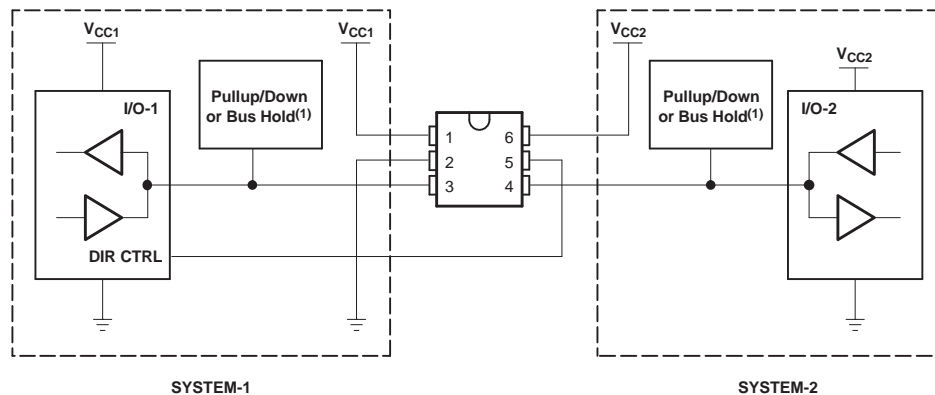
### 10.2.1.3 Application Curve



**Figure 12. Translation Up (1.8 V to 5 V) at 2.5 MHz**

### 10.2.2 Bidirectional Logic Level-Shifting Application

Figure 13 shows the SN74LVC1T45 being used in a bidirectional logic level-shifting application. Because the SN74LVC1T45 does not have an output-enable ( $\overline{OE}$ ) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.



**Figure 13. Bidirectional Logic Level-Shifting Application**

#### 10.2.2.1 Design Requirements

See [Design Requirements](#).

#### 10.2.2.2 Detailed Design Procedure

Table 3 shows data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

**Table 3. SYSTEM-1 and SYSTEM-2 Data Transmission**

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	Out	In	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on pullup or pulldown. <sup>(1)</sup>
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pullup or pulldown. <sup>(1)</sup>
4	L	Out	In	SYSTEM-2 data to SYSTEM-1

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, that is, both pullup or both pulldown.

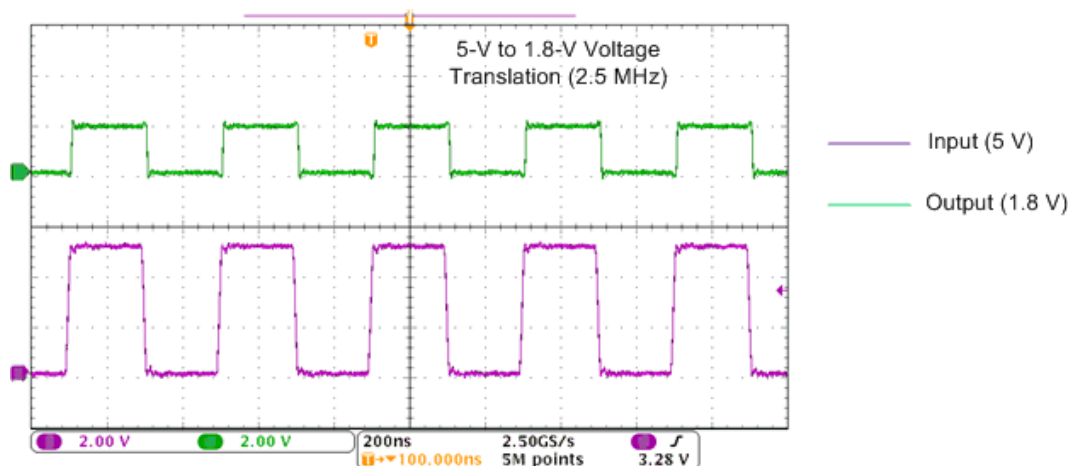
### 10.2.2.2.1 Enable Times

Calculate the enable times for the SN74LVC1T45 using the following formulas:

- $t_{PZH} \text{ (DIR to A)} = t_{PLZ} \text{ (DIR to B)} + t_{PLH} \text{ (B to A)}$
- $t_{PZL} \text{ (DIR to A)} = t_{PHZ} \text{ (DIR to B)} + t_{PHL} \text{ (B to A)}$
- $t_{PZH} \text{ (DIR to B)} = t_{PLZ} \text{ (DIR to A)} + t_{PLH} \text{ (A to B)}$
- $t_{PZL} \text{ (DIR to B)} = t_{PHZ} \text{ (DIR to A)} + t_{PHL} \text{ (A to B)}$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74LVC1T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

### 10.2.2.3 Application Curve



**Figure 14. Translation Down (5V to 1.8 V) at 2.5 MHz**

## 11 Power Supply Recommendations

The SN74LVC1T45 device uses two separate configurable power-supply rails,  $V_{CCA}$  and  $V_{CCB}$ .  $V_{CCA}$  accepts any supply voltage from 1.65 V to 5.5 V and  $V_{CCB}$  accepts any supply voltage from 1.65 V to 5.5 V. The A port and B port are designed to track  $V_{CCA}$  and  $V_{CCB}$ , respectively allowing for low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V and 5-V voltage nodes.

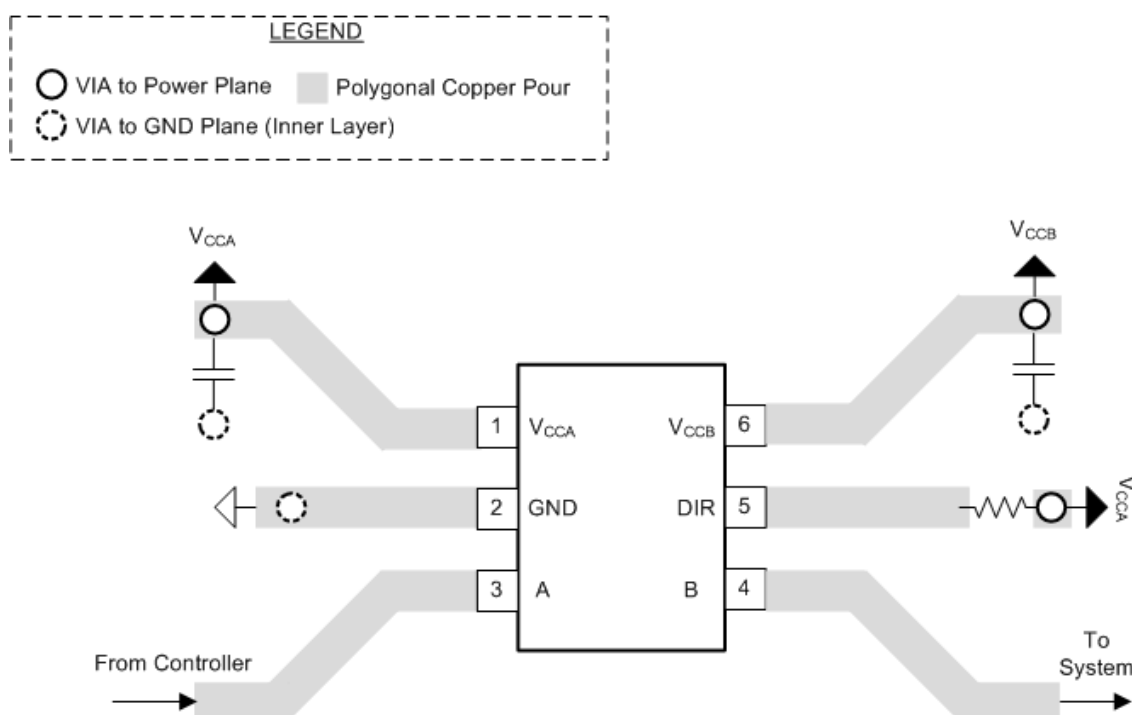
## 12 Layout

### 12.1 Layout Guidelines

To ensure reliability of the device, the following common printed-circuit board layout guidelines are recommended:

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depends on the system requirements

### 12.2 Layout Example



**Figure 15. Layout Example**



## 13 Device and Documentation Support

### 13.1 Documentation Support

#### 13.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#), SCBA004

### 13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.4 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 13.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1T45DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT15 ~ CT1F ~ CT1R)	<a href="#">Samples</a>
SN74LVC1T45DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT15 ~ CT1F ~ CT1R)	<a href="#">Samples</a>
SN74LVC1T45DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT15 ~ CT1F ~ CT1R)	<a href="#">Samples</a>
SN74LVC1T45DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT15 ~ CT1F ~ CT1R)	<a href="#">Samples</a>
SN74LVC1T45DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT15 ~ CT1F ~ CT1R)	<a href="#">Samples</a>
SN74LVC1T45DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5 ~ TAF ~ TAR)	<a href="#">Samples</a>
SN74LVC1T45DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5 ~ TAF ~ TAR)	<a href="#">Samples</a>
SN74LVC1T45DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5 ~ TAF ~ TAR)	<a href="#">Samples</a>
SN74LVC1T45DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5 ~ TAF ~ TAR)	<a href="#">Samples</a>
SN74LVC1T45DCKTE4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5 ~ TAF ~ TAR)	<a href="#">Samples</a>
SN74LVC1T45DCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5 ~ TAF ~ TAR)	<a href="#">Samples</a>
SN74LVC1T45DPKR	ACTIVE	USON	DPK	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TA7	<a href="#">Samples</a>
SN74LVC1T45DRLR	ACTIVE	SOT-OTHER	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA7 ~ TAR)	<a href="#">Samples</a>
SN74LVC1T45DRLRG4	ACTIVE	SOT-OTHER	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA7 ~ TAR)	<a href="#">Samples</a>
SN74LVC1T45YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TA2 ~ TA7 ~ TAN)	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

---

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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#### **OTHER QUALIFIED VERSIONS OF SN74LVC1T45 :**

● Automotive: [SN74LVC1T45-Q1](#)

● Enhanced Product: [SN74LVC1T45-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- 
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1T45DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1T45DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1T45DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1T45DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1T45DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74LVC1T45DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1T45DCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74LVC1T45DCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1T45DPKR	USON	DPK	6	5000	180.0	9.5	1.75	1.75	0.7	4.0	8.0	Q2
SN74LVC1T45DRLR	SOT-OTHER	DRL	6	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74LVC1T45DRLR	SOT-OTHER	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1T45YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

## TAPE AND REEL BOX DIMENSIONS

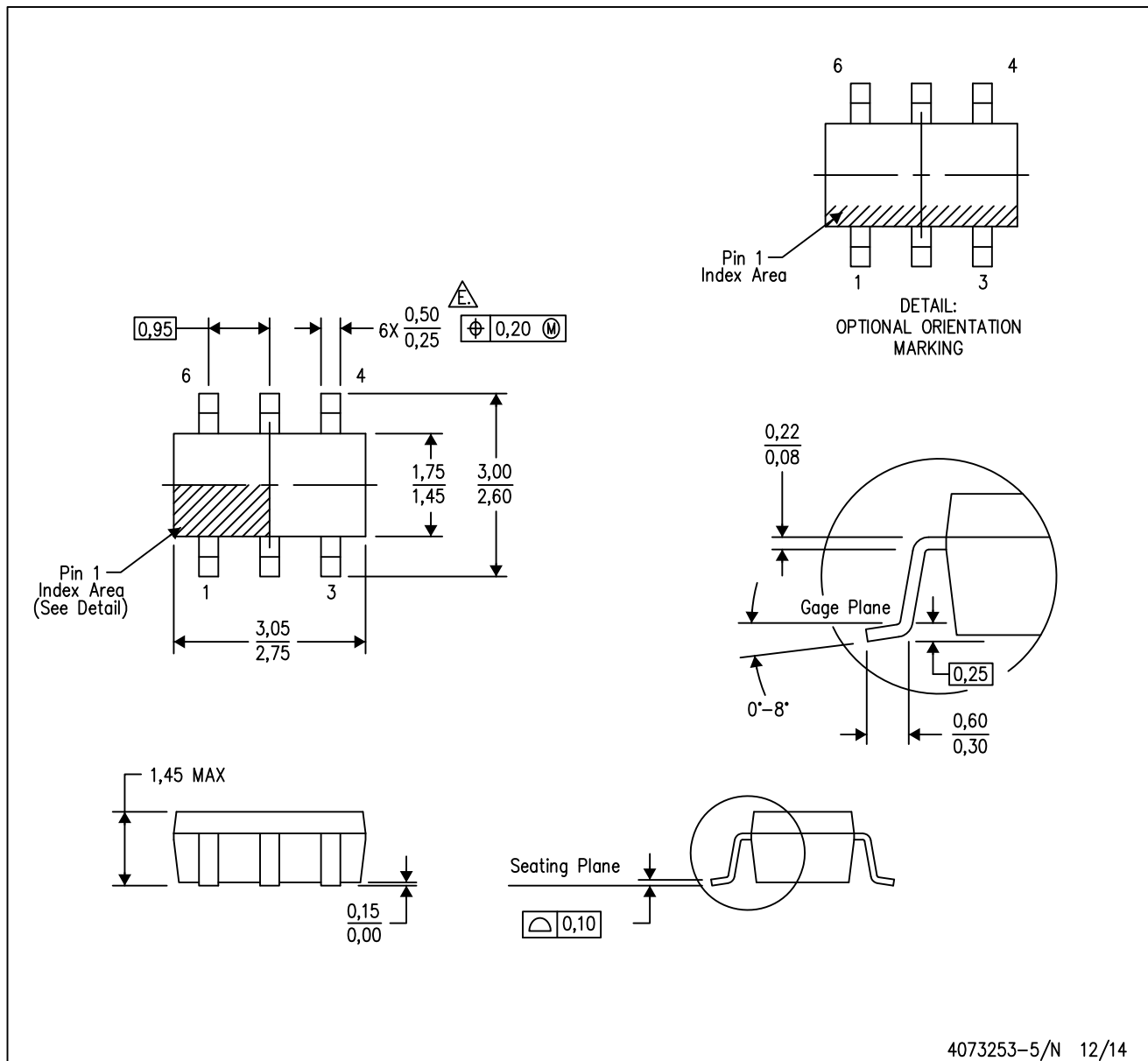


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1T45DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC1T45DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74LVC1T45DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74LVC1T45DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
SN74LVC1T45DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74LVC1T45DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1T45DCKT	SC70	DCK	6	250	202.0	201.0	28.0
SN74LVC1T45DCKT	SC70	DCK	6	250	180.0	180.0	18.0
SN74LVC1T45DPKR	USON	DPK	6	5000	184.0	184.0	19.0
SN74LVC1T45DRLR	SOT-OTHER	DRL	6	4000	184.0	184.0	19.0
SN74LVC1T45DRLR	SOT-OTHER	DRL	6	4000	202.0	201.0	28.0
SN74LVC1T45YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE

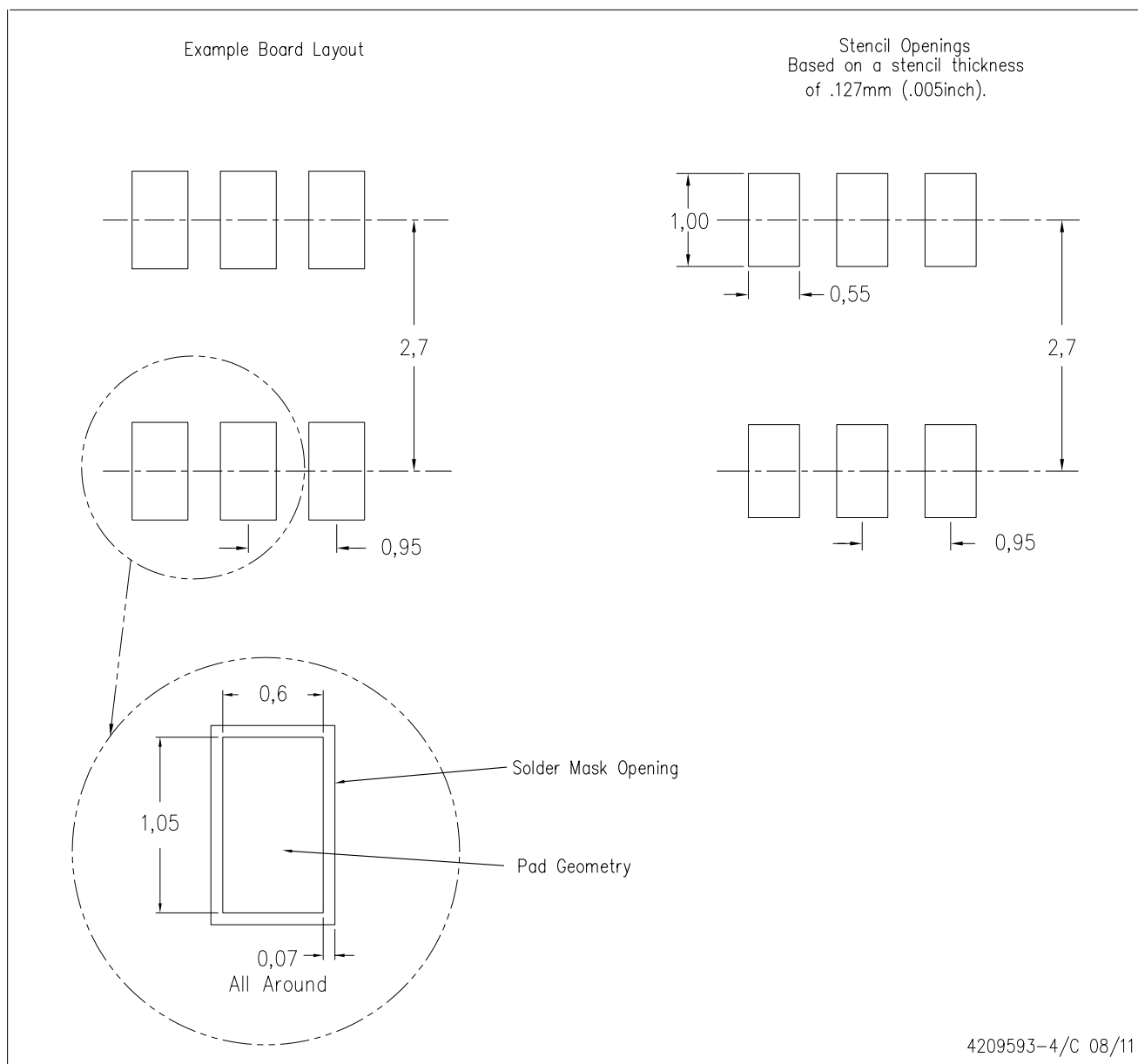


4073253-5/N 12/14

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
  - E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



## DCK (R-PDSO-G6)

## PLASTIC SMALL-OUTLINE PACKAGE



4093553-4/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

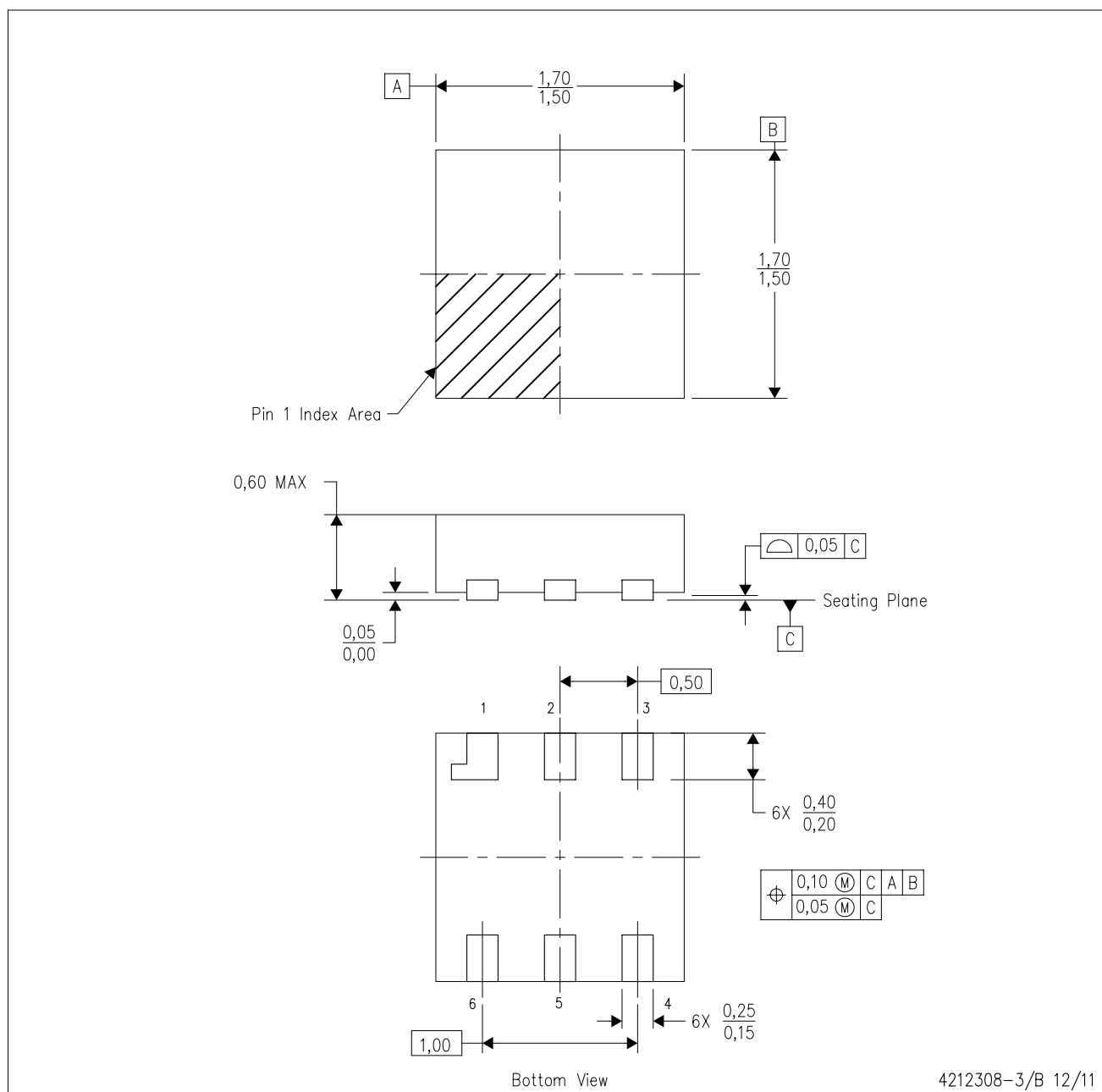
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DPK (S-PUSON-N6)

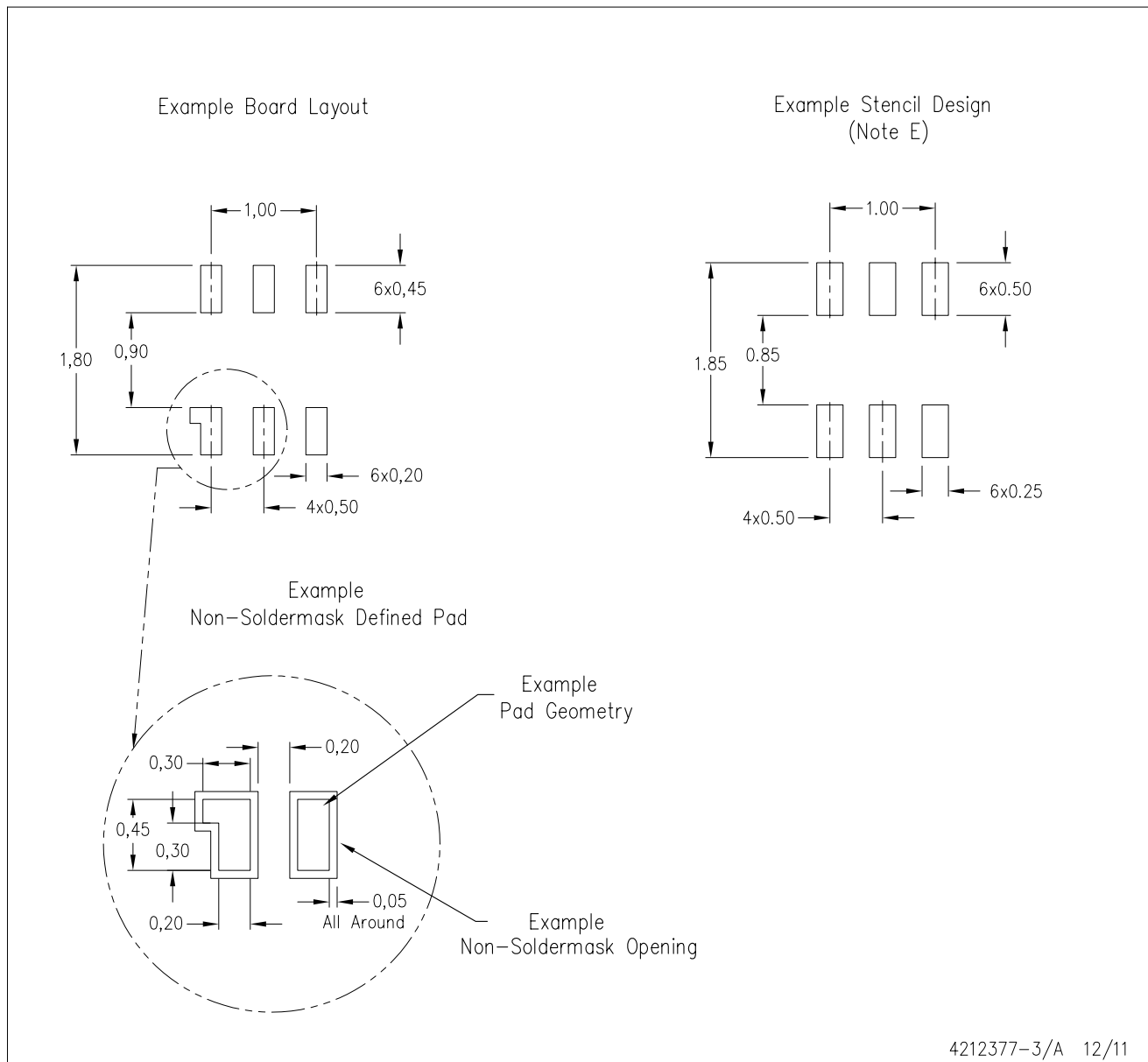
PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.

DPK (S-PUS0N-N6)

PLASTIC SMALL OUTLINE NO-LEAD



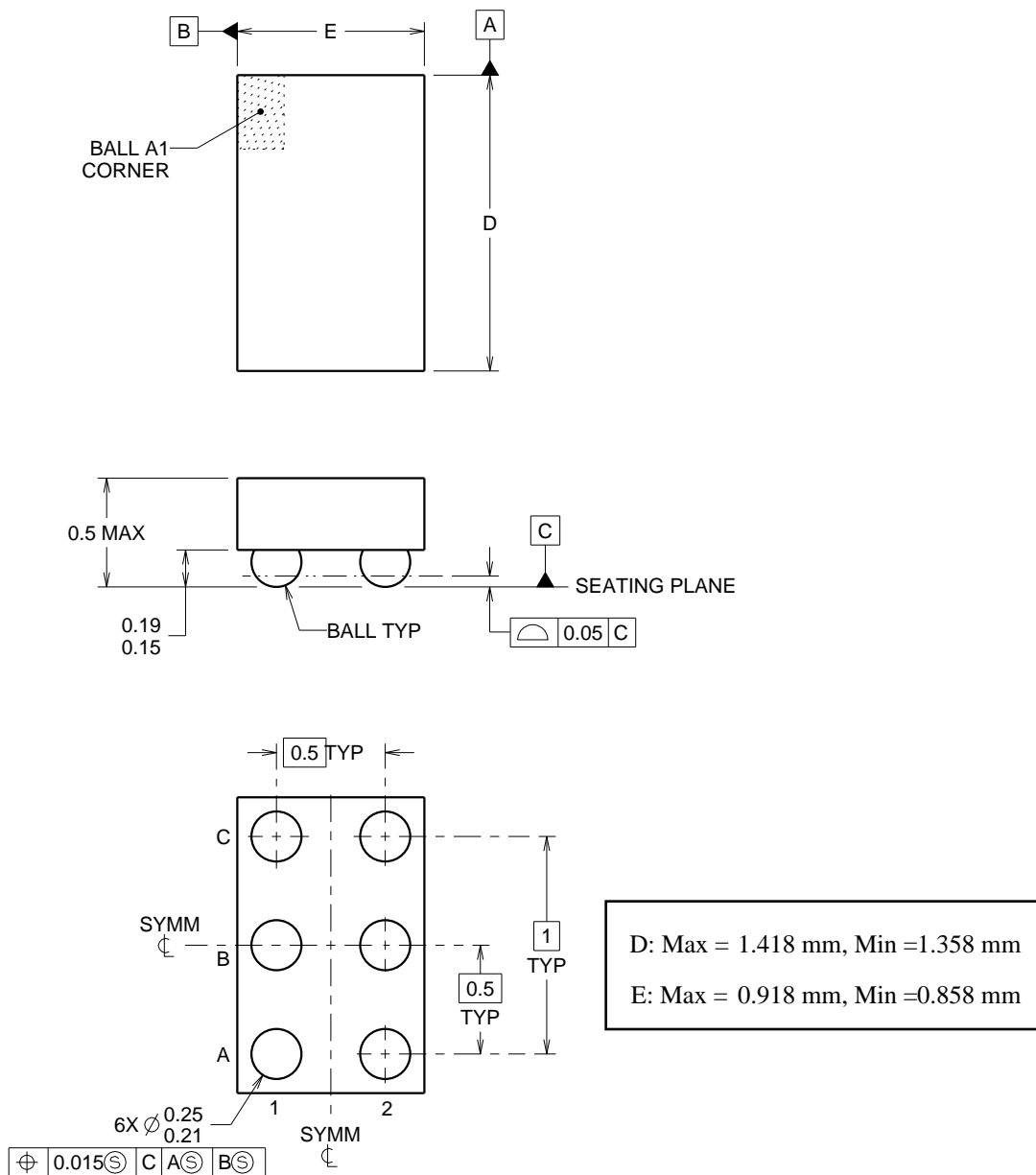
4212377-3/A 12/11

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



## DSBGA - 0.5 mm max height

## DIE SIZE BALL GRID ARRAY



4219524/A 06/2014

NOTES:

NanoFree Is a trademark of Texas Instruments.

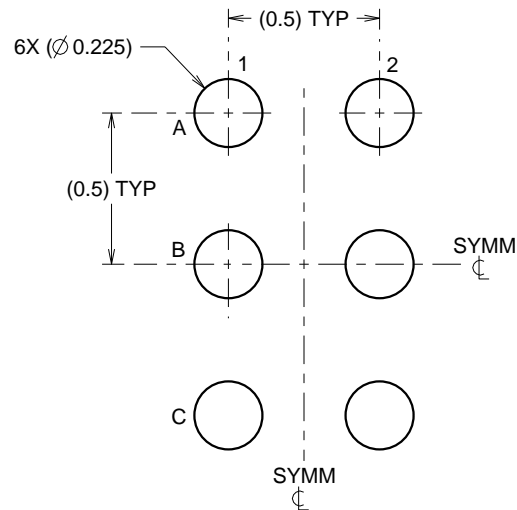
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

# EXAMPLE BOARD LAYOUT

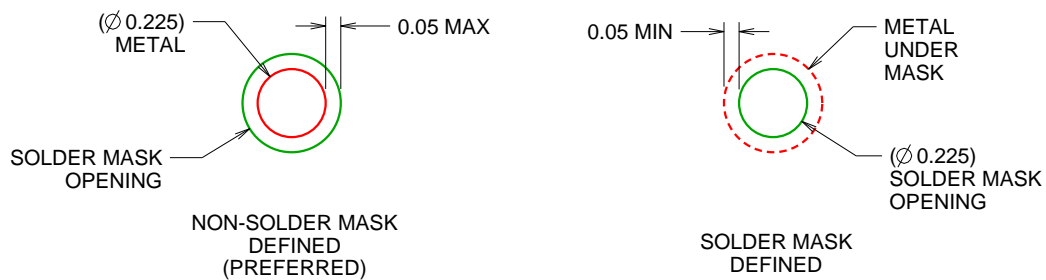
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 ([www.ti.com/lit/sbva017](http://www.ti.com/lit/sbva017)).

## EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



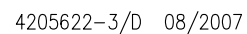
SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4219524/A 06/2014


NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## PLASTIC SMALL OUTLINE



NOTES:

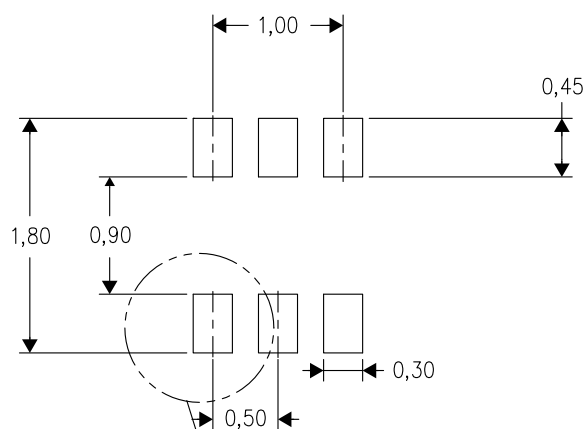
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
-  C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
- D. JEDEC package registration is pending.



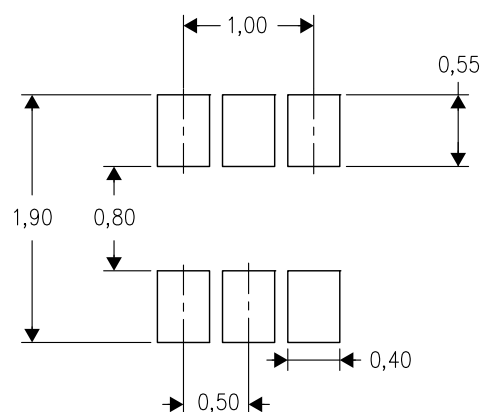
DRL (R-PDSO-N6)

PLASTIC SMALL OUTLINE

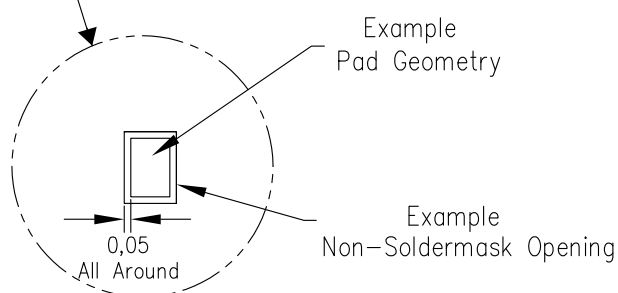
Example Board Layout



Example Stencil Design  
(Note E)



Example  
Non-Soldermask Defined Pad



Example  
Pad Geometry

Example  
Non-Soldermask Opening

4208207-3/E 06/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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